RTG4 Radiation Test Results and Test Plans

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Outline

- Total ionizing dose (TID) effects
  1. TID induced effect at the device level
     a. Floating gate devices
     b. CMOS devices
  2. TID induced effect at the product level
     a. Propagation delay
     b. Power supply current

- Single event effects (SEE)
  1. Single event latchup
  2. Single event upset
     • Flash configuration cell
     • Radiation hardened FF (STMRFF)
     • Fabric SRAMs: LSRAM and µSRAM
  3. MBU and MCU

- Radiation Test plan
Total ionizing dose (TID) effects
TID Testing

- **Facilities**
  - Air Force Research Laboratory (AFRL), NASA Goddard Space Flight Center, Vanderbilt University (VU)

- **Testing condition**
  - Gamma ray and x-ray
  - Dose rate: 5 krad/min and 18 krad/min
  - Dose steps: 25, 50, 100, 150, 200 krad

- **Test parameters**
  1. Propagation Delay
  2. Power Supply Current
RTG4 Flash Configuration Cell

SmartFusion2 : Sense-Switch bit cell

- The data signal doesn’t pass directly through the flash transistor
- RTG4 Push-Pull cell is significantly more radiation tolerant:
  - Radiation induced $V_t$ change in the Nflash and Pflash cells does not result in a change in the switch state (no propagation delay degradation)
- In SmartFusion2 : Propagation delay reaches 10% degradation after 25 krad
  - TID induced charge accumulation in the FG causes the $V_t$ of the switch transistor to change
TID induced effects in the floating gate device

- Radiation induced $V_t$ shift model: $V_T(\gamma) = V_T(\infty) + [V_T(0) - V_T(\infty)] \cdot \text{Exp}(-A \gamma)$

- No S/D leakage current

$\gamma$: total ionizing dose

$V_T(0)$: pre-rad $V_T$

$V_T(\infty)$: saturation $V_T$

$A$: Fitted decay coefficient
TID effect in the CMOS devices

- NMOS devices in programming and signal path
- Hardened high and medium voltage NMOS devices
- No S/D leakage current
TID induced effect in RTG4: Propagation Delay

- Propagation delay measured on an inverter-string design with 7200 stages programmed into the FPGA

SmartFusion2

- 10% degradation after ~25 Krad

RTG4
TID induced effect in RTG4: Core power supply current

- IDD: core power supply current
- 10% increase of the RTG4 power supply current
TID induced effect in RTG4: Power supply current

- IDD: core power supply current
- IDD_PLL: PLL power supply current
- IDDI: I/O bank power supply current
- IPP: Charge pump (programming circuit) power supply current
Single Event Effect Results
Outline

- RTG4 flash-based FPGA overview
- Testing condition and silicon preparation
- SEE Test Results
  - SEE in configuration Flash switch
  - SEL
  - SEU data in RT4G150
    1. Flip-Flop
    2. LSRAM
    3. μSRAM
  - MBU and MCU
- SEU simulation
  - Correlate SRAM data with 3D TCAD simulation
- Reprogramming
- Summary
RTG4 Flash-based FPGA

- RTG4 is a new radiation tolerant flash-based FPGA manufactured in UMC 65 nm technology
- Blocks configured and connected by Flash switches
- Functional Blocks
  - Fabric
    - Logic element (4LUT + carry chain + STMR FF)
    - Math block (DSP)
    - EDAC LSRAM and μSRAM
  - SpaceWire clock
  - SERDES
  - μPROM
  - RT PLLs, oscillators, CCCs
SEE Testing Conditions

- **Lawrence Berkeley National Laboratory (LBNL)**
  - 16 MeV/nucleon cocktail, vacuum chamber
  - LETs Tested: 1.16 to 69.72 MeV.cm²/mg (LET = 90.32 w/ Tilting and Si thickness adjustment)
  - Temperature: Room for SEU, 100 ºC for SEL
  - Bias: Nominal for SEU, Nominal+5% for SEL
  - Tilting -45, 0, +45

- **Texas A&M University (TAMU)**
  - 15 MeV, vacuum chamber for ion penetration
  - LET Tested: 9.8 to 103 MeV.cm²/mg
  - Temperature: Room for SEU, 100 ºC for SEL
  - Bias: Nominal for SEU, Nominal+5% for SEL
  - Tilting -30, 0, +30
Preparation of Silicon

- Need to back-grind Flip-Chip from 675 μm to ~60 μm
- Special Considerations
  - Die size is very large (>2cm x 2cm)
  - Back grind silicon to ensure beam penetration
- Things learned
  - Take it slow when grinding, 6-8 hours per part
  - Use fresh fine diamond coated bits per chip
  - Edge cracks if too much force is applied (100 gr)
  - Thermal relaxation reduces center to edge variance
  - Verification of die thickness is important (SEM)

Measured Die thickness at center and edge. <10μm difference
## Single Event Latchup

<table>
<thead>
<tr>
<th>Temperature</th>
<th>LET (MeV.cm(^2)/mg)</th>
<th>SEL</th>
<th>Fluence (ions/cm(^2))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Room Temp</td>
<td>9.8</td>
<td>0</td>
<td>2.00x10(^7)</td>
</tr>
<tr>
<td></td>
<td>13.74</td>
<td>0</td>
<td>2.00x10(^7)</td>
</tr>
<tr>
<td></td>
<td>26.9</td>
<td>0</td>
<td>6.51x10(^7)</td>
</tr>
<tr>
<td></td>
<td>31.06</td>
<td>0</td>
<td>5.00x10(^7)</td>
</tr>
<tr>
<td></td>
<td>89</td>
<td>0</td>
<td>5.00x10(^6)</td>
</tr>
<tr>
<td></td>
<td>103</td>
<td>0</td>
<td>2.60x10(^7)</td>
</tr>
<tr>
<td>100 °C</td>
<td>58</td>
<td>0</td>
<td>4.00x10(^7)</td>
</tr>
<tr>
<td></td>
<td>89</td>
<td>0</td>
<td>8.94x10(^7)</td>
</tr>
<tr>
<td></td>
<td>103</td>
<td>0</td>
<td>7.58x10(^7)</td>
</tr>
</tbody>
</table>

- Single event latchup testing performed at room temperature and 100 °C, Nominal+5% bias
- No SEL is observed up to LET = 103 MeV.cm\(^2\)/mg @ 100 °C
RTG4 Flash Configuration Cell

- Functionality of the FPGA was **continuously** monitored during radiation exposure.
- No configuration upsets were detected in the 10 parts tested at LBNL and TAMU up to LET = 103 MeV.cm$^2$/mg.
- **RTG4 flash configuration cell is SEU immune.**

<table>
<thead>
<tr>
<th>LET (MeV.cm$^2$/mg)</th>
<th>Configuration Upset</th>
<th>Total fluence (ions/cm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.16 to 103</td>
<td>0</td>
<td>5.02x10$^8$</td>
</tr>
</tbody>
</table>
RTG4 Flash Configuration Cell

- 2 parameters contribute to RTG4 Push-Pull cell SEU immunity
  - Microsemi FPGA flash cells larger than std. flash memory cells
  - Switch transistor in RTG4 Push-Pull data path is indirectly coupled to the floating gate

SmartFusion2 : Sense Switch bit cell

RTG4 : 4T Push-Pull bit cell
Flip-Flop Physical Placement

- **STMRFF**
  - RTG4 features built in STMR into each FF
- **2000x10 FF chains**
  - 400 FF per row x 5 rows = 2000 FF per chain
  - Total of 10 chains, 20000 FFs for statistics
- **Global**
  - Manually placed to identify global upsets in Quadrant, Half, Full Fabric
RTG4 Flip-Flop Cross Section

Error Rates for GEO MIN, 100 mil Al

<table>
<thead>
<tr>
<th>Product</th>
<th>Device</th>
<th>upset/bit-day</th>
</tr>
</thead>
<tbody>
<tr>
<td>SmartFusion2</td>
<td>FF</td>
<td>$1.76 \times 10^{-7}$</td>
</tr>
<tr>
<td>RTG4</td>
<td>STMRFF</td>
<td>$5.01 \times 10^{-12}$</td>
</tr>
</tbody>
</table>
SRAM blocks in RTG4 FPGA fabric

- μSRAM can be used as register file in state machine and μcontroller
- LSRAM can be used as cache memory
- Circuit design and layout techniques are used to mitigate SET affects
  - All registers in the data path employ STMR FF
- Built-in EDAC with SECDED code

<table>
<thead>
<tr>
<th>SRAM</th>
<th>Configuration</th>
<th>#Tx/bit cell</th>
<th>Area (μm²)</th>
<th>size</th>
<th>RT4G150 blocks</th>
</tr>
</thead>
<tbody>
<tr>
<td>μSRAM</td>
<td>2 read port and 1 write port</td>
<td>14</td>
<td>7.74</td>
<td>1.5 Kb</td>
<td>210</td>
</tr>
<tr>
<td>LSRAM</td>
<td>Dual port and two-port</td>
<td>8</td>
<td>4.07</td>
<td>24.5 Kb</td>
<td>209</td>
</tr>
</tbody>
</table>
**µSRAM single bit cross section**

- µSRAM SEU rate = $3.33 \times 10^{-8}$ upset/bit-day for GEO MIN, 100 mil Al
LSRAM single bit cross section

- LSRAM SEU rate $= 4.03 \times 10^{-8}$ upset/bit-day for GEO MIN, 100 mil Al
LSRAM SEU TCAD simulation

- 3D TCAD simulations using RCI tools are performed to compare and calibrate with beam test results.

- The 3D structure includes three LSRAM cell and “source-ties” to account for the SRAM’s neighboring cells:
  - “source-ties” are additional junctions tied to $V_{dd}$ and ground, to accurately simulate charge collection.
  - The dashed lines represent the targeted LSRAM cell boundary.
Correlate Beam Test Data with TCAD

- The simulation results show a good correlation with beam test data at lower LET
  - At higher LETs the simulations deviate from testing data (results under investigation)
- The cross sections only deviate at higher LET and doesn’t affect error rate prediction
  - The LET spectrum in space is dominated by low LET ions
- The upset rates using the simulated cross section and beam test data are very close
  - $4.03 \times 10^{-8}$ upset/bit-day for beam test data
  - $4.67 \times 10^{-8}$ upset/bit-day for the simulations
Mitigation of MBU in RTG4

- MBUs are mitigated by the interleaving of logical bits in the physical memory blocks in RTG4
- In RTG4 logically adjacent bits are separated by 9 physical bits
Fabric SRAM MBU detection

- The post-irradiation state of the SRAMs is compared to the “golden” SRAMs pre-irradiation state
- Readback of the SRAM is executed and processed to determine the number of SBU, MBU and MCU count
- Testing performed at low flux and refresh period is optimized to allow full read of the memory
  - The probability of multiple ion strikes in the time it takes to read the memory is negligible
### MBU and MCU results

<table>
<thead>
<tr>
<th>LET (MeV.cm²/mg)</th>
<th>Total Fluence (ions/cm²)</th>
<th>Flux (ions/cm²/s)</th>
<th>MBU</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.8 to 103</td>
<td>1.72x10⁸</td>
<td>1x10⁴ to 5x10⁴</td>
<td>0</td>
</tr>
</tbody>
</table>

- **Zero** MBU are observed with RTG4 built-in interleaving
- MCU size 2 to 8 are observed but can be corrected with EDAC
## Reprogramming

- Preliminary data shows reprogramming successful up to 106 krad from Heavy-Ion Irradiation

<table>
<thead>
<tr>
<th>DUT Name</th>
<th>Total Dose from Heavy Ion</th>
<th>Reprogram Passed</th>
<th>Functional</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTG4_S07</td>
<td>80 krad</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>RTG4_S08</td>
<td>47 krad</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>RTG4_S09</td>
<td>48 krad</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>RTG4_S10</td>
<td>106 krad</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>
**Summary**

- RTG4 Push-Pull Flash configuration cell is SEU immune
- No SEL observed at 100 °C and LET > 100 MeV.cm²/mg
- SEU Error Rate at Geo Min
  - STMRFF error rate : $5.01 \times 10^{-12}$
  - LSRAM (No EDAC) bit error rate : $4.03 \times 10^{-8}$
  - μSRAM (No EDAC) bit error rate : $3.33 \times 10^{-8}$
- 3D TCAD simulations allow good error rate prediction
- Zero MBU observed for LSRAM or μSRAM
- MCU are observed but can be corrected with EDAC
RTG4 Test Plan
## RTG4 Radiation Test Plan

<table>
<thead>
<tr>
<th>July 1&lt;sup&gt;st&lt;/sup&gt; &amp; Oct 6&lt;sup&gt;th&lt;/sup&gt; SEE@LBNL</th>
<th>Aug 18&lt;sup&gt;th&lt;/sup&gt; TID@NASA</th>
<th>Sept 14&lt;sup&gt;th&lt;/sup&gt; TID@VU</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RT4G150:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>1. SEU</strong></td>
<td><strong>2. Functionality</strong></td>
<td><strong>1. X-ray comparison</strong></td>
</tr>
<tr>
<td>- SRAM with EDAC</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>2. SET</strong></td>
<td><strong>2. Power Supply Current</strong></td>
<td></td>
</tr>
<tr>
<td>- Fabric logic</td>
<td><strong>3. Input Logic Threshold</strong></td>
<td></td>
</tr>
<tr>
<td>- Mathblock</td>
<td>(VIL/VIH)</td>
<td></td>
</tr>
<tr>
<td>- Global clock</td>
<td><strong>4. Output Drive Voltage</strong></td>
<td></td>
</tr>
<tr>
<td>- SpaceWire</td>
<td>(VOL/VOH)</td>
<td></td>
</tr>
<tr>
<td>- MSIO &amp; MSIOD</td>
<td><strong>5. Propagation Delay</strong></td>
<td></td>
</tr>
<tr>
<td><strong>3. SEFI</strong></td>
<td><strong>6. Transition Time</strong></td>
<td></td>
</tr>
<tr>
<td>- SERDES/PCIe</td>
<td><strong>7. Reprogramming</strong></td>
<td></td>
</tr>
<tr>
<td>- PLL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- DDR controller</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>4. Re-programming in beam</strong></td>
<td></td>
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</tr>
</tbody>
</table>

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