Power Matters.™

RTG4 Board Level Considerations

Microsemi Space Forum 2015

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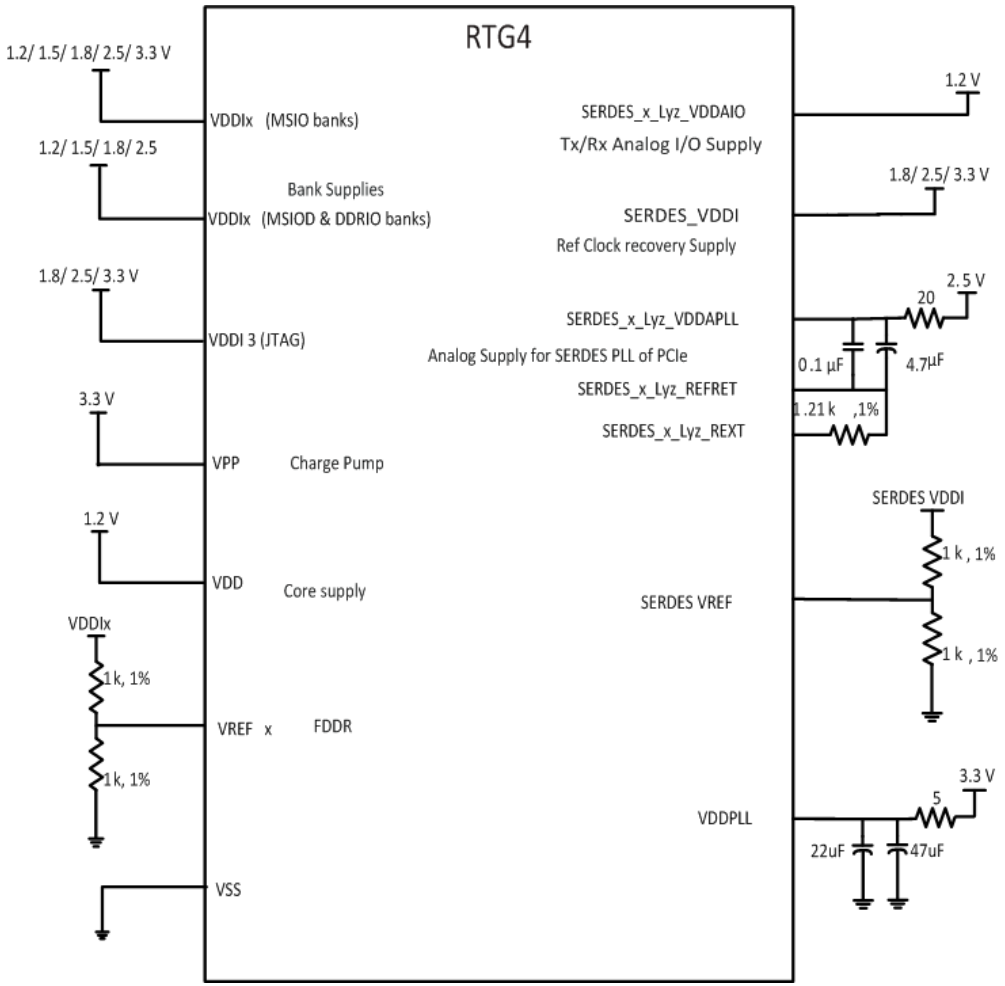
Objectives

- Provide an overview of PCB design considerations for RTG4 designs focusing on:
  - Power Supplies
  - Memory Controller Interfaces
  - SERDES Interfaces

- Highlight information currently available in Microsemi documents

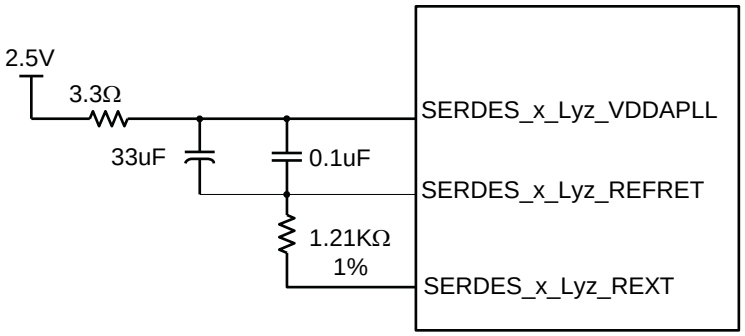
Power Supplies



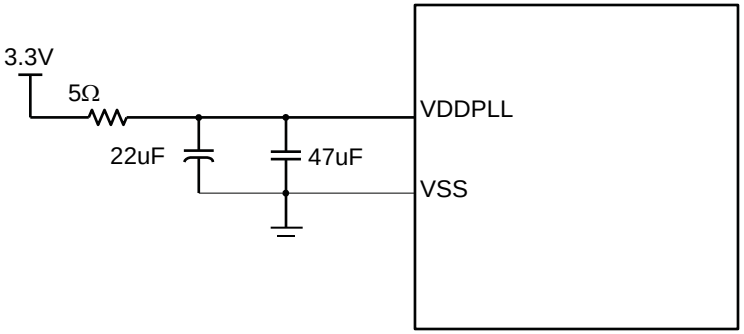
Supply	Voltage	Description
VDD	1.2 V	Core supply voltage
VPP	3.3 V	Power supply for device charge pumps
VDDPLL	3.3 V	Power for eight corner PLLs, PLLs in SERDES PCIe/PCS blocks, and FDDR PLL
VDDIx	1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V	Bank supplies
VREFx	0.5 * VDDIx	FDDR reference voltage
SERDES_x_Lyz_VDDAIO	1.2 V	TX/RX analog I/O voltage for SERDES lanes.
SERDES_x_Lyz_VDDAPLL	2.5 V	Analog power for SERDES TXPLL and CDRPLL
SERDES_VDDI	1.8 V, 2.5 V, or 3.3 V	Power for SERDES reference clock receiver supply.
SERDES_VREF	0.5 * SERDES_VDDI	External differential receiver reference voltage for SERDES Reference Clocks

Analog Supplies

SERDES VDDAPLL Supply



FPGA PLL Supply



- External R-C filters provide filtering to sensitive analog PLL supplies.
- SERDES PLL = 2.5V
  - SERDES TXPLL and CDRPLL supply
  - SERDES Calibration resistor(REXT). 1.21KΩ
    - Impedance calibration (transmit, receive, and receiver equalization)
- FPGA PLLs = 3.3V
- Place all passive components as close to device as possible

Power Supplies Specifications

- Key power supplies must comply to the specifications including operating range, POR trip points, and power supply ramping
- Monotonicity of VDD/VPP/VDDIx is required through its rise time

Preliminary Data

Symbol	Description	Min	Typ	Max	Units
VDD	Core Supply Voltage	1.14	1.2	1.26	V
VPP	Flash operating voltage	3	3.3	3.45	V
VDDt	Power ON Reset Threshold for VDD supply		0.8		V
VPPt	Power ON Reset Threshold for VPP supply		2.6		V
VDDr	VDD Power supply ramp rates (from GND/0V) for all power supplies	0.006		24	mV/µs
Tvddpor	Power Up to Functional time (From VDD/VPP/VDDIx ramp to beginning of device ready		60		ms

Power-up/down Sequence

- There is no power-up/down sequence required for RTG4 if one of the following conditions is met:
  - All PLLs are held in reset until VDDPLL supply reaches its minimum recommended Operating Conditions level (shown below)

Symbol	Parameter	Min	Typ	Max	Units
VDDPLL	Power for eight corner PLLs, PLLs in SERDES PCIe/PCS blocks, and FDDR PLL.	3.15	3.3	3.45	V

  - The device is held in reset by asserting DEVRST_N until VDDPLL supply reaches its minimum recommended level as stated above

- If none of the above conditions is met, VDDPLL must start ramping up and reach its minimum recommend level (as stated above) before VDD, VPP, or VDDIx starts ramping up
  - In other words, VDDPLL must not be the last supply to ramp up, and must reach its minimum recommended level before the last supply starts ramping up

- All I/O banks supplies must be powered for the RTG4 to power up
  - You can bring up the I/O banks in any order and before or after the core voltage

Power Supply Decoupling Capacitors

- To reduce any potential fluctuation on the power supply lines, proper on-board power supply decoupling caps is required
  - Keep decoupling caps close to pin (use 402's where possible on underside of device BGA)
  - Distribute overall decoupling capacitance around the device perimeter
  - Use blind vias to remove crosstalk risk and cap surface mount area
  - Use larger power vias to reduce inductance- especially for high layer count boards.

- PME (Precious Metal Electrode) decoupling caps within the package enhance overall PCB decoupling

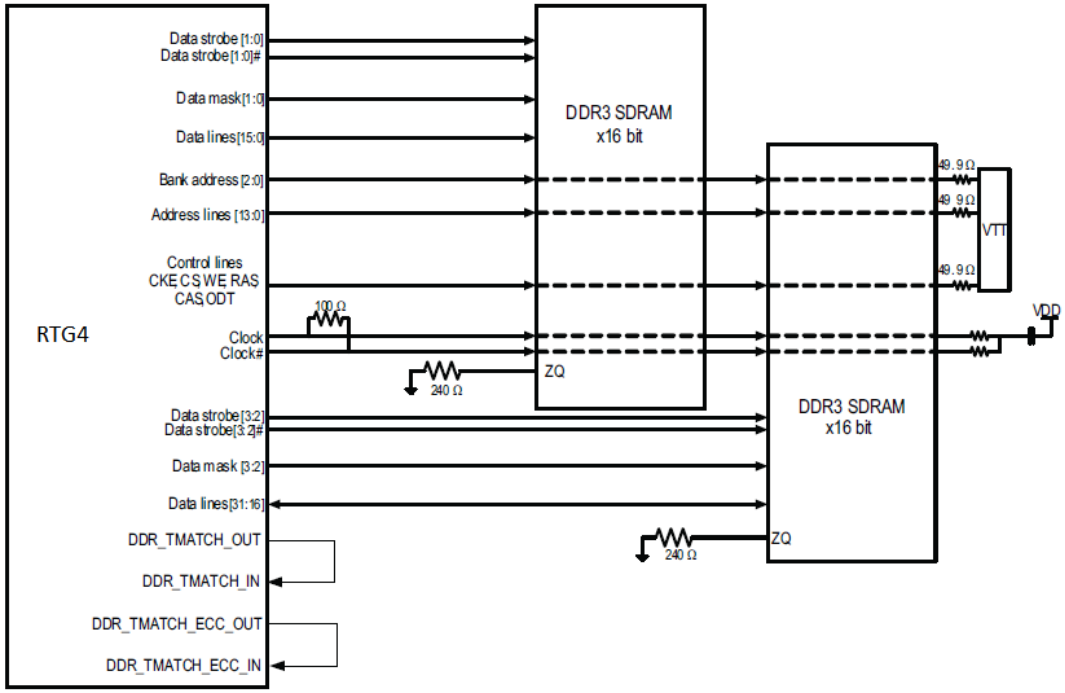
Pin Name	Internal PME capacitance available for LG/CG1657 package
VDD	0.18uF/6.3V
VDDI0	0.18uF/6.3V
VDDI1	0.18uF/6.3V
VDDI2	0.18uF/6.3V
VDDI4	0.18uF/6.3V
VDDI5	0.18uF/6.3V
VDDI6	0.18uF/6.3V
VDDI7	0.18uF/6.3V
VDDI8	0.18uF/6.3V
VDDI9	0.18uF/6.3V
VDDPLL	0.8uF/6.3V

Radiation Tolerant Power Supplies

- Microsemi provides many Radiation-Tolerant components that can be used with RTG4 PCB designs
- Engineers should consider the following when selecting power supply components
  - Calculate required power of the RTG4 device
    - Power Calculator spreadsheet
    - SmartPower tool in Libero SoC
  - Select an appropriate Radiation-Tolerant regulator that can supply the required power and meet all the unique power requirements of the FPGA, using either of the below:
    - Radiation-Tolerant Linear-Regulator (Microsemi)
    - Radiation-Tolerant Switching regulator (Microsemi)

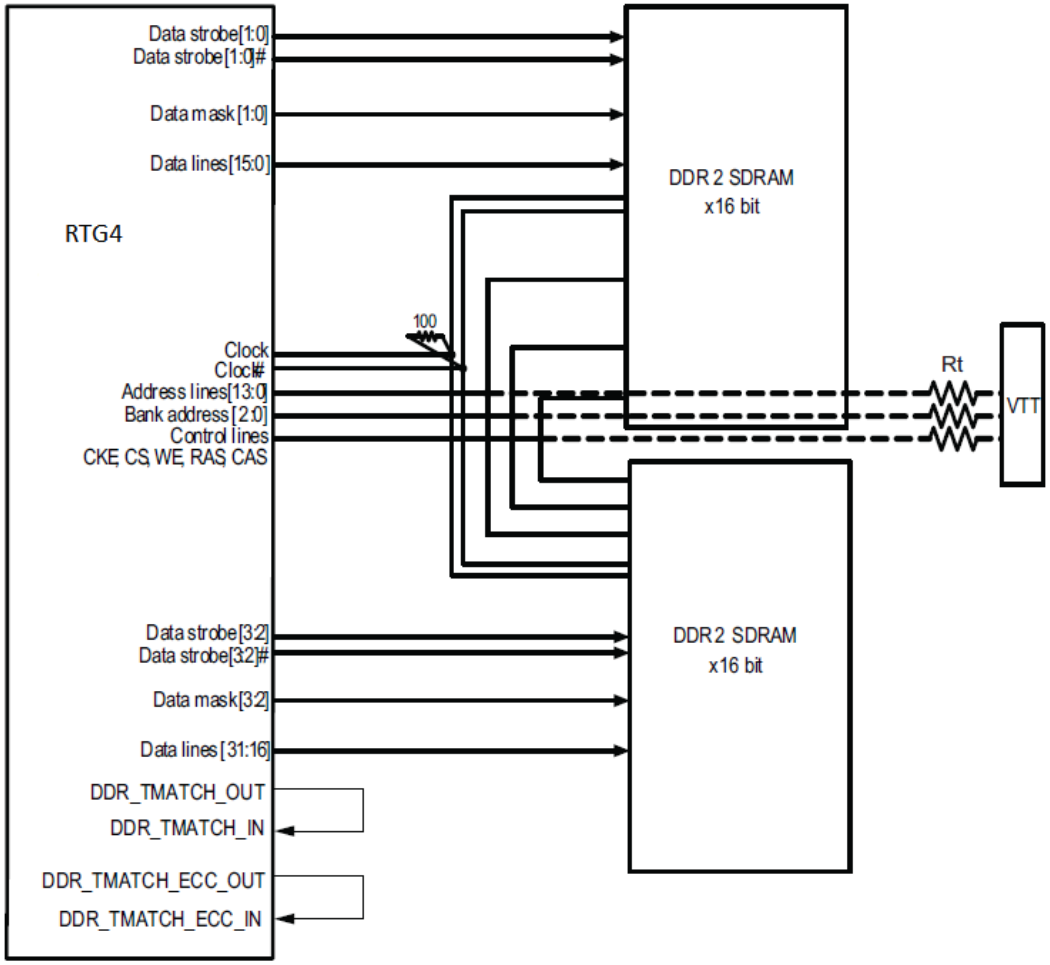
DDR3 Memory Interface

- DDR3 Characteristics
  - SSTL15 interface
  - RTG4 On-Die termination
  - RTG4 IMP_CALIB resistor
    - 240Ω
  - CMD/ADDR require external termination to VTT(0.75V)
  - CLK_P/CLK_N requires differential resistor at memory clk input
  - Match ADDR/CMD/CTRL to CLK
  - Tightly match DQ/DM/DQS delays
  - TMATCH DQS compensation



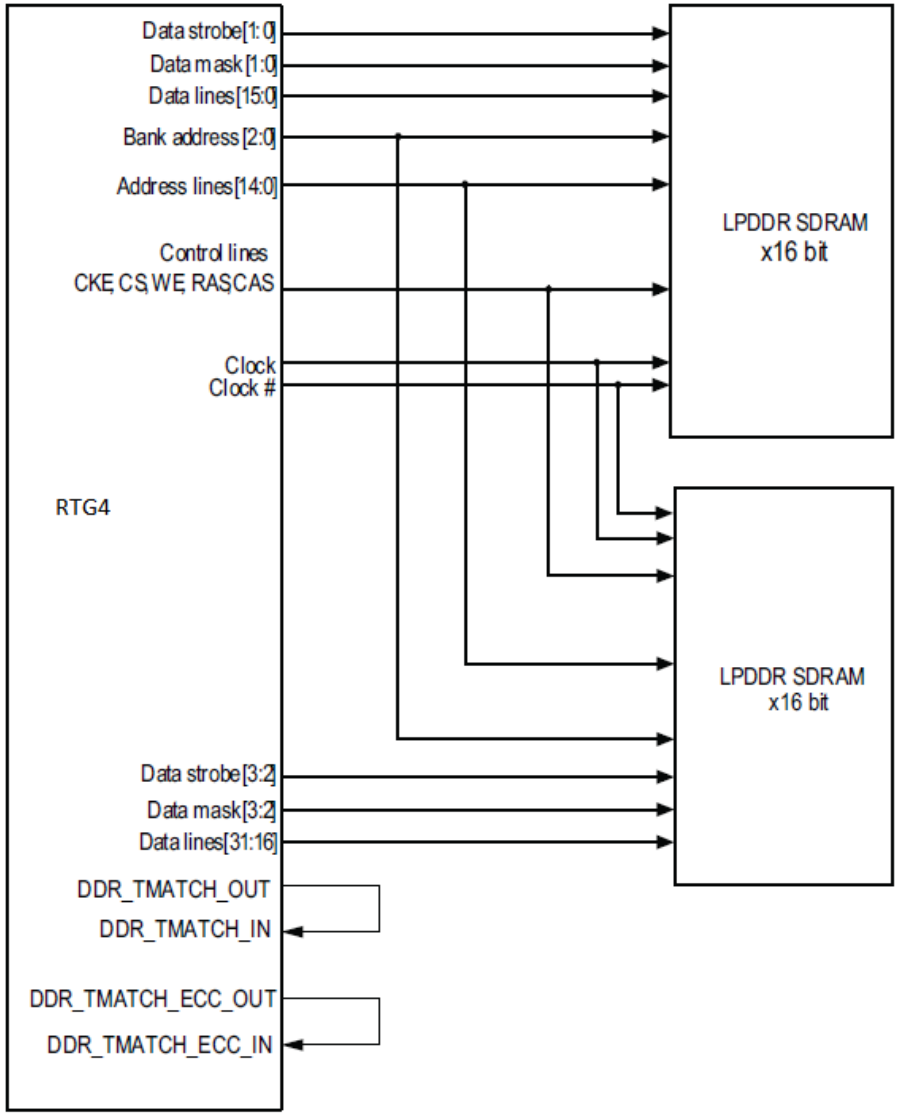
DDR2 Memory Interface

- DDR2 Characteristics
  - SSTL18
  - RTG4 On-Die termination
  - RTG4 IMP_CALIB resistor
    - 150Ω
  - CMD/ADDR require external termination to VTT(0.9V)
  - CLK_P/CLK_N requires differential resistor at memory clk input
  - Match ADDR/CMD/CTRL to CLK
  - Tightly matched DQ/DM/DQS delays
  - Loosely match DQS to CLK
  - TMATCH DQS compensation



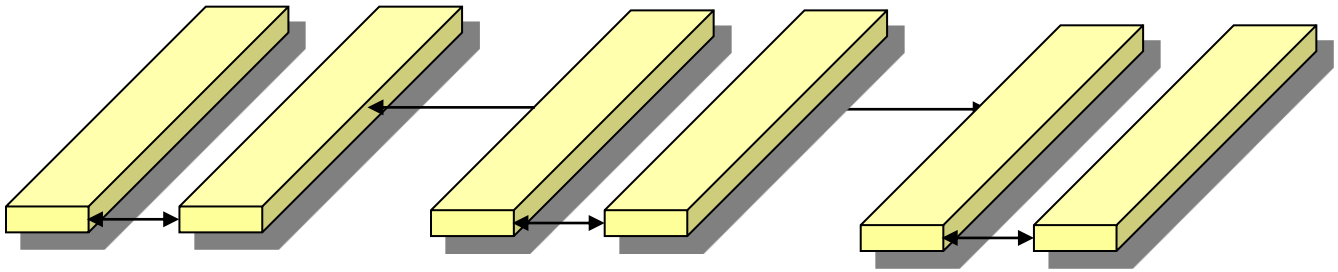
LPDDR Memory Interface

- LPDDR Characteristics
  - LVCMOS18
  - Match ADDR/CMD/CTRL to CLK
  - Tightly matched DQ/DM/DQS
  - Loosely match DQS to CLK
  - TMATCH DQS compensation

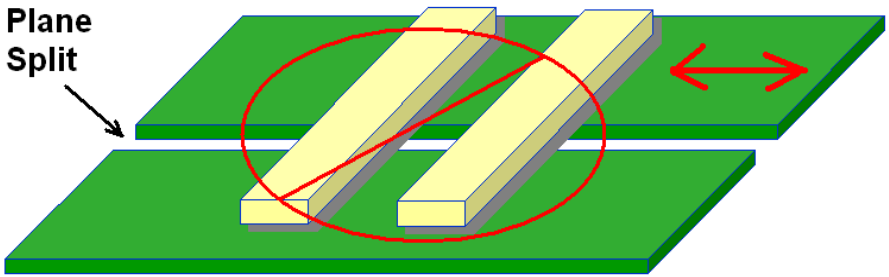


SERDES Routing

- Proper differential pair routing is needed for proper common-mode rejection and noise immunity
  - Pair-to-pair spacing is 2X greater than trace-to-trace spacing

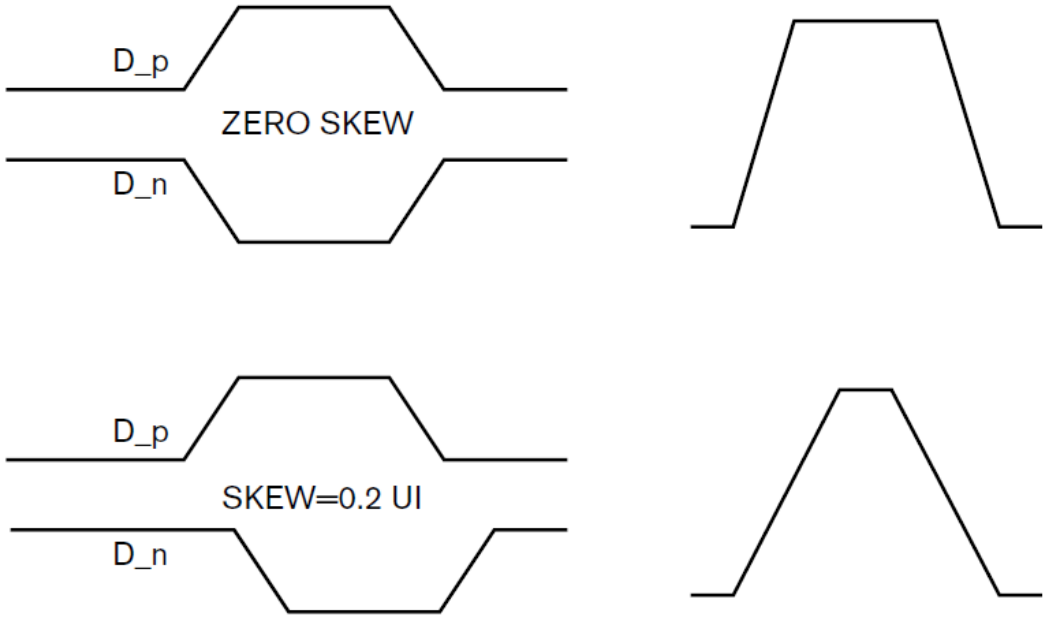


- Avoid Routing Discontinuities:
  - No Plane Split Crossing
  - Do not route High-Speed signals close to the edge of a plane



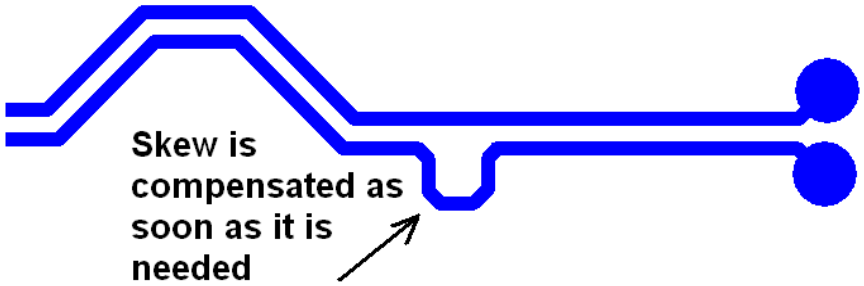
SERDES Differential Skew

- "Differential skew" refers to the time difference between the two single-ended signals in a differential pair (LANE)
- Skew limits the bandwidth, adds data-dependent jitter, and limits the possibility of properly equalizing lanes



SERDES Skew Matching

- P & N trace skew matching “meandering” is used to balance the skew of the pair, it should be distributed throughout the trace length

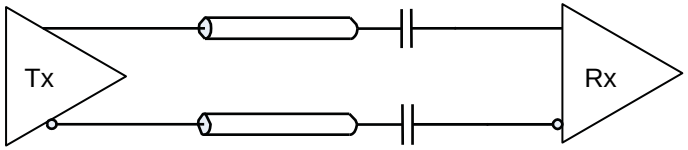


Immediately compensating will result in better skew distribution

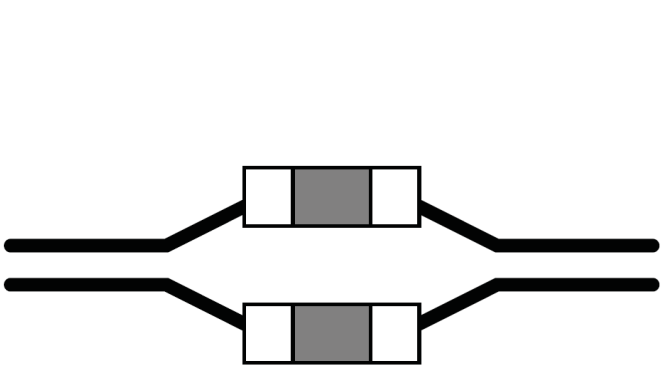
- Keep traces matched throughout routing, not at the end

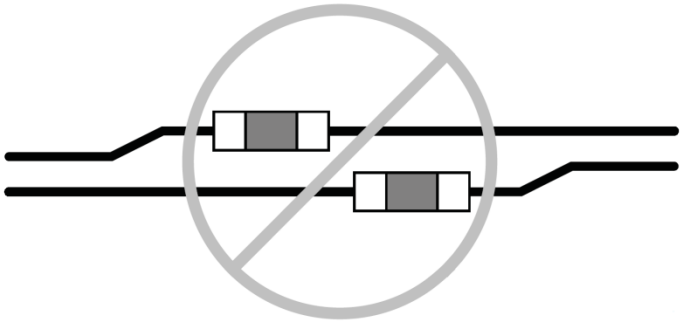
AC-Coupling

- RTG4 requires AC-Coupling for all SERDES applications including PCI Express for link detection
- AC-coupling provides common-mode independence



- Use symmetrical routing and placement for best performance.



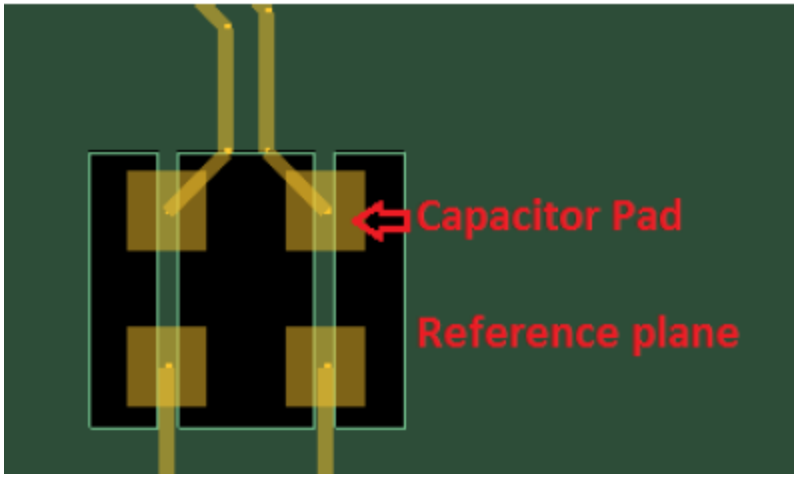


Creates wider trace spacing resulting in more discontinuity

AC-Coupling

- Minimize reflections from the mounting structures with cut-outs in the reference plane

- Clearing of the reference plane underneath the ac-coupling cap produces less discontinuities of the routing path



SpaceWire: ES/MS to PROTO/Flight Silicon

- RTG4 ES device supports 12 SpaceWire ports
  - RTG4 ES Dev board supports **12** SpaceWire ports
- The SpaceWire package pin assignment will be updated in the next silicon revision for PROTO and flight units to support **16** SpaceWire ports
  - RTG4 Production Dev board will support 13 SpaceWire ports
- Going from the current silicon revision to the next silicon revision, refer to the pin mapping of the device on the Dev board

  SpaceWire Pin Mapping from RTG4 ES/MS Silicon to PROTO/Flight Silicon for RTG4 Development Kit

CG1657 Package Pins

- Two devices are available in Libero SoC Software
  - RT4G150_ES CG1657
  - RT4G150 (production) CG1657

- Software generated package pins for RT4G150_ES are not compatible with pins generated for RT4G150 device
  - Due to SpaceWire enhancements

- The following pin mapping tables are provided to help you start designing your board

  SpaceWire Pin Mapping from RTG4 ES/MS Silicon to PROTO/Flight Silicon

  SpaceWire Pin Mapping from RTG4 ES/MS Silicon to PROTO/Flight Silicon for RTG4 Development Kit

Take-Aways

- Understand key points of the RTG4 power supplies and requirements
- Recognize the different PCB topologies and features for the memory controllers available with the RTG4
- Awareness of SERDES layout methods needed for PCB first-time success

Appendix

Name	Operating Voltage	Description
VDD	1.2 V	DC core supply voltage. Must always power this pin.
VPP	3.3 V	Power supply for charge pumps (for normal operation and programming). Must always power this pin.
VDDIx where x is the bank number	1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V	I/O bank supplies for MSIO, MSIOD and DDRIO banks. For MSIO banks: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V For MSIOD banks: 1.2 V, 1.5 V, 1.8 V, 2.5 V For DDRIO banks: 1.2 V, 1.5 V, 1.8 V, 2.5 V For JTAG bank: 1.8 V, 2.5 V, or 3.3 V To power-up the device, all I/O banks must be powered (to exit from power-on-reset state). There is no power-up sequence requirement between VDDI, VPP, and VDD supplies.
VDDPLL	3.3 V	Power for Eight corner PLLs, PLLs in SERDES PCIe/PCS blocks, and FDDR PLL. When in use, the supply must be connected to a common PLL supply (3.3 V) of the corresponding PLL return path (VSS) on-board through an RC filter. When not in use, the supply must be directly connected to 3.3 V (without the filter circuit).
VREF0 VERF9	0.5 * VDDI	Reference voltage for FDDR signals. Reference voltages must be powered with the appropriate bank supplies through voltage divider circuitry. If I/O banks are used as single-ended I/Os (and FDDR functionalities are not used), VREF0, VREF9 can be left floating (DNC).
SERDES_x_Lyz_VDDAIO where, • x refers to 1, 2, 3, 4, PCIE_0 or PCIE_5 • yz refers to lanes 0 and 1, or lanes 2 and 3	1.2 V	TX/RX analog I/O voltage for SERDES lanes. Low voltage power for Lane-y and Lane-z of SERDES_x. If SERDES is not used, it must be connected to 1.2 V
SERDES_x_Lyz_VDDAPLL where, • x refers to 1, 2, 3, 4, PCIE_0 or PCIE_5 • yz refers to lanes 0 and 1, or lanes 2 and 3	2.5 V	Analog power for SERDES lanes. If SERDES is used, all SERDES PLL pins must be connected to the appropriate supply (2.5 V) of the corresponding return path on-board (SERDES_x_Lyz_REFRET) through an RC filter. If SERDES is not used, they must connect directly to 2.5 V without the RC filter circuit.
SERDES_x_Lyz_REFRET where, • x refers to 1, 2, 3, 4, PCIE_0 or PCIE_5 • yz refers to lanes 0 and 1, or lanes 2 and 3	—	Local on-chip ground return path for SERDES lanes. If SERDES is not used, it must be grounded (VSS).
SERDES_x_Lyz_REXT where, • x refers to 1, 2, 3, 4, PCIE_0 or PCIE_5 • yz refers to lanes 0 and 1, or lanes 2 and 3	—	External reference resistor (1.21 kΩ) connected to calibrate TX/RX termination value. Each SERDES_x consists of two REXT signals—one for Lane0 and Lane1, and another for Lane2 and Lane3. If the SERDES is not used, it must remain floating (DNC).
SERDES_VDDI	1.8 V, 2.5 V, or 3.3 V	Power for SERDES reference clock receiver supply. The supply voltage depends on SERDES reference clock source. Must always power this pin.
SERDES_VREF	0.5 * SERDES_VDDI	External differential receiver reference voltage for SERDES Reference Clocks. Reference voltage must be powered with the SERDES_VDDI supply through voltage divider circuitry. If SERDES reference clock uses an I/O reference standard such as SSTL, HSTL on the board, SERDES_VREF must be connected to SERDES_VDDI through a voltage divider circuit. If SERDES is not used or SERDES reference clock uses a non reference standard such as LVDS, LVCMOS, and LVTTL on the board, SERDES_VREF must be connected to Ground through a 1 k–10 kΩ resistor.
VSS	Ground	Ground pad for core and I/Os. Always connect to ground.

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