Power Matters.™

RTG4 Packaging Technology

Microsemi Space Forum 2015

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Microsemi SPACE FORUM

Agenda

- Microsemi Flip-Chip Ceramic Column Grid (CCGA) for Space
  - Packaging road map
  - RTG4-CCGA1657 package construction for hermetically seal with Space application features
  - Package qualification plan and status
  - Package design to meet electrical performance
  - Thermal management in Space
- Summary

- Support Document and Data: CCGA (ceramic column grid array) package as the platform for Space

Hi-Rel Ceramic Packaging Roadmap

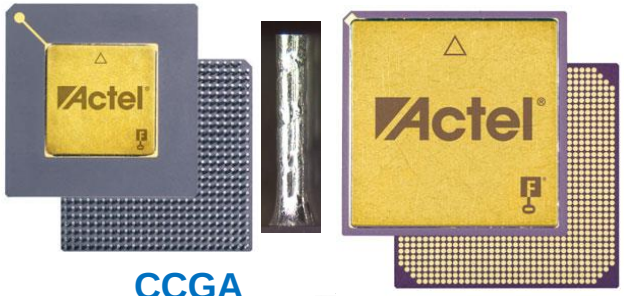
Mature Packages

2008 to 2010

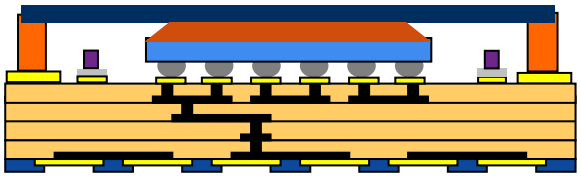
Future Packages

2013 to 20xx

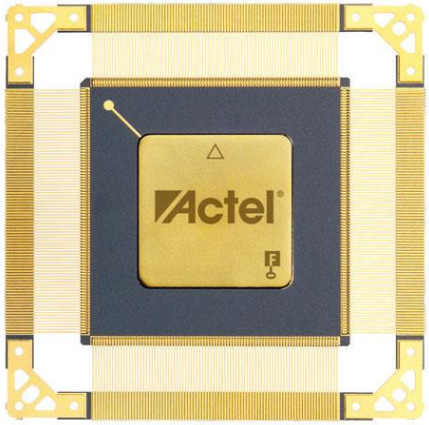
PGA
132 – 391 Pins



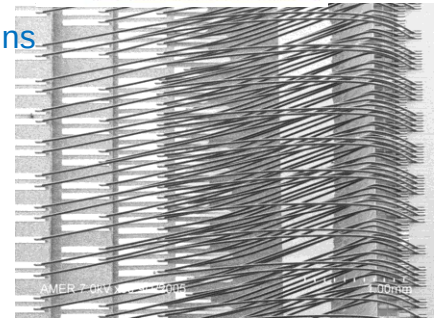
CCGA
624 – 1272 Columns

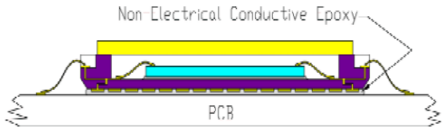


Hermetically seal Flip-Chip CCGA
1432 to 2000+ Columns



CQFP
84 – 352 Leads

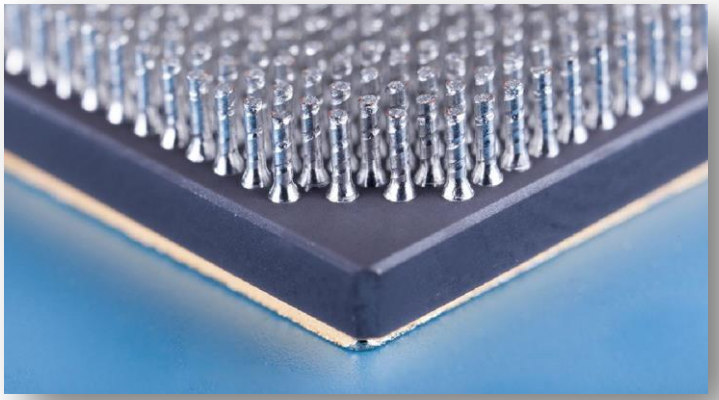




CC256
Chip Carrier

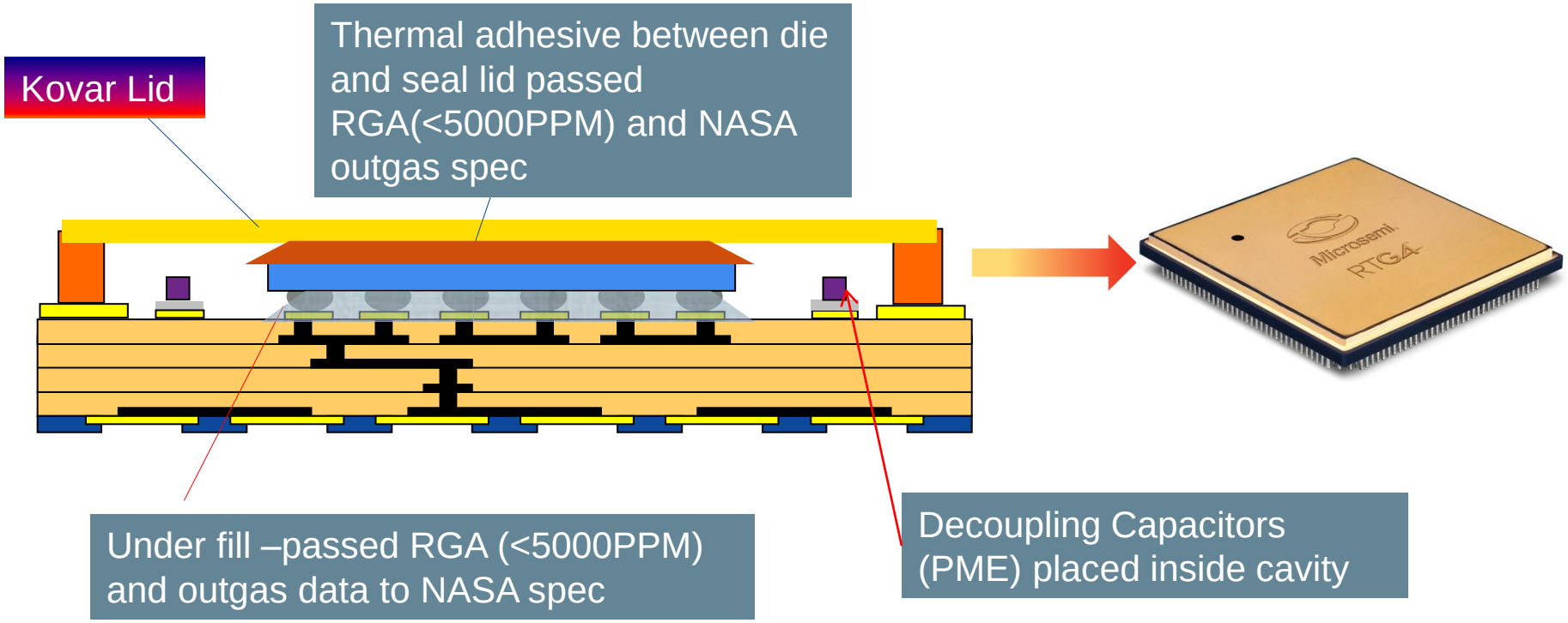
RTG4 Packaging Overview

- Hermetically sealed, ceramic packages
  - Embedded decoupling capacitors
    - Flight models will have Precious Metal Electrode (PME) capacitors
  - Column Grid Array, Ball Grid Array, Land Grid Array



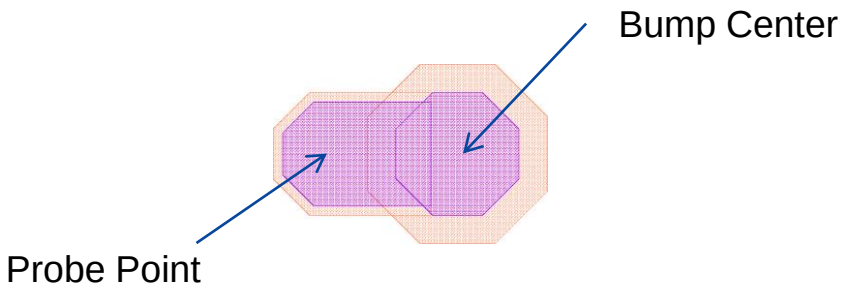
Microsemi Approach: Flip-Chip Ceramic Package Hermetically Lid Seal and Target to V Flow

- Package size: 42.5x42.5mm, 1.0mm pitch, 1657 column pins, 20+ ceramic layers, with hermetically seam seal.
- Target to meet class V (hermetically seal), better than Class Y (non-hermetic)



Detail Of BOM of Production Package

- **Silicon Die**
  - 205 um minimum bump pitch
  - Eutectic solder bump, plated.
  - UBM: TiW 1000A/Cu 2000A, Ni 2um
  - 100 +/-15um um bump height
  - With separated pads for wafer probing



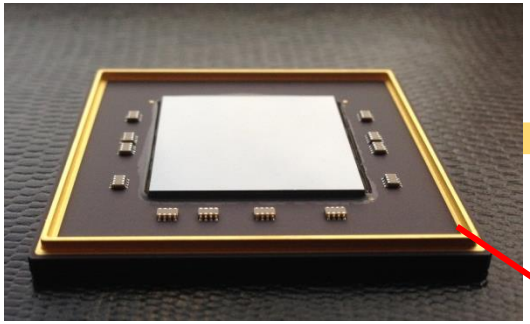
- **Ceramic Package**
  - Use the same ceramic material and metal trace as other older devices such as CQ packages
  - 42.5 mm X 42.5 mm, 1.0 mm Column Pitch
  - 90 um bump pad with Ni and gold plating
  - 0.8 mm Solder Land Pad
  - 1657 Solder Columns, 0.51 mm Ø,
  - Six-Sigma 80/20 Cu wrap column pin, same as other older devices like CG624
- **Capacitors**
  - PME--- Precious Metal Electrode, meet MIL-PRF-THIN Space Grade “T”
- **Daisy Chain Package: available**
  - Almost the same as production package except with 1 layer added for creating the chain for board level testing
  - Initial offering has BME IDC decoupling capacitors, but will phase in with PME capacitors later

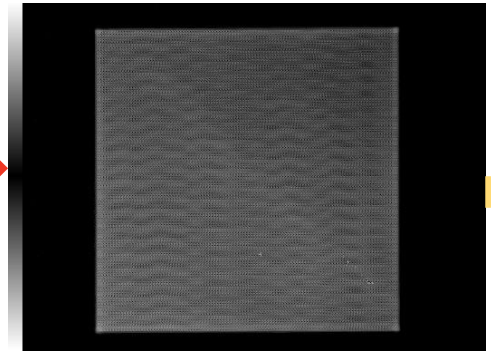
Production Screen Flow and Group B, D

- **Production Screen Flow:**
  - Screen to B and V flow per MIL-PRF-38535 latest version—expect to fully comply
    - Over 1000 parts have been assembled, and no issues so far
  - Group B and D—expect to meet all requirements
- **PIDTP (Package Integrity Demonstrated Test Plan)**
  - In process
  - Expect to meet most of the requirements with some exceptions in TM5011 regarding underfill material
    - But we will comply with all screen requirements (screen flow, group B and D) even certain steps in TM 5011 can not be obtained due to material suppliers are not able to provide data (note: JEDEC committees acknowledge TM5011 need to modify from last JEDEC meeting in Savannah May 2015)
- **Package decoupling capacitors**
  - PME-- Precious Metal Electrode
  - Full complied with MIL-PRF-123 and MIL-PRF-THIN “T” grade (currently working version of spec)
  - Using PME would eliminate concerns about the long term reliability of package decoupling capacitors such as BME (base metal electrode)

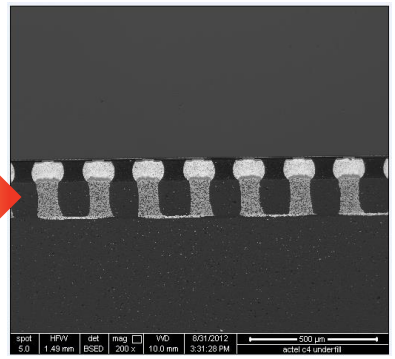
Key Assembly Process Steps Data

- **Underfill—no void**





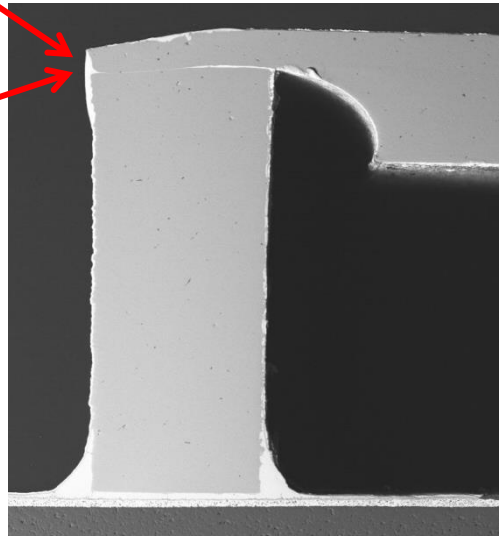
CSAM checking flip-chip under-fill



Cross section of C4 flip-chip bumps

- **Hermetically Lid Seal**

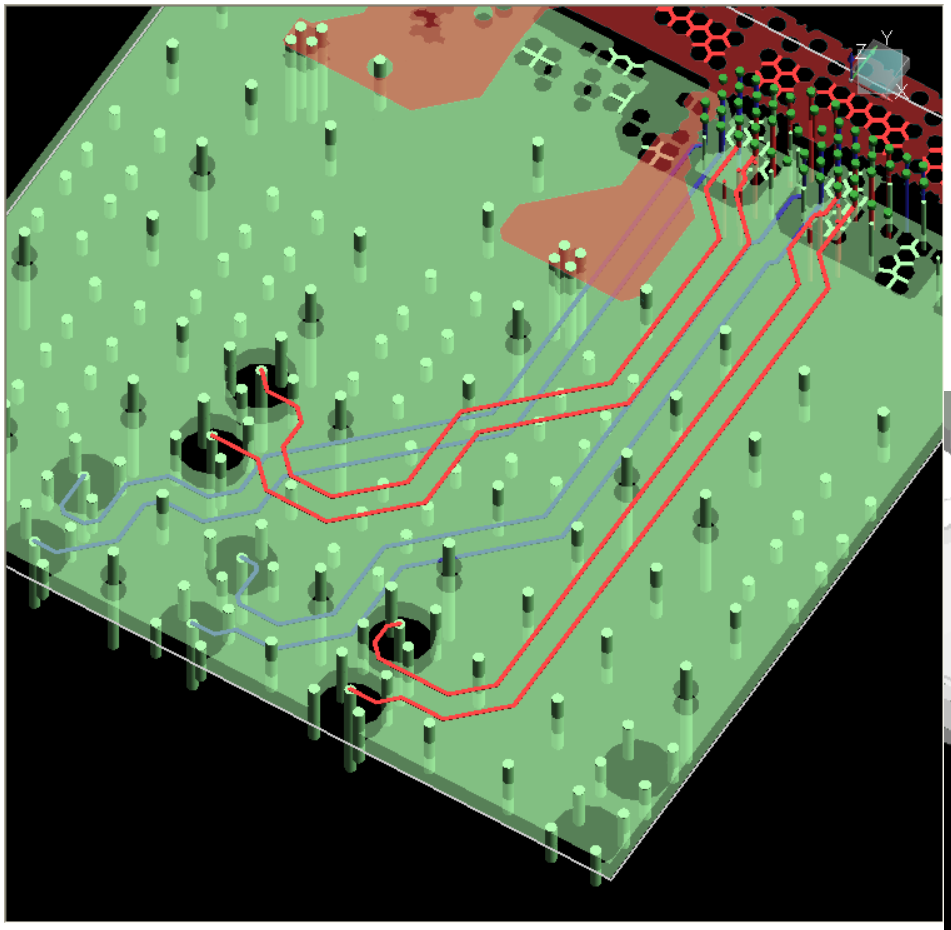
Assembled unit with seam seal Kovar lid

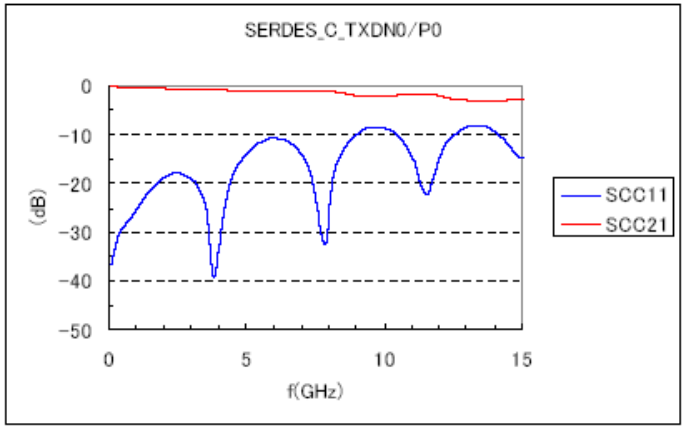


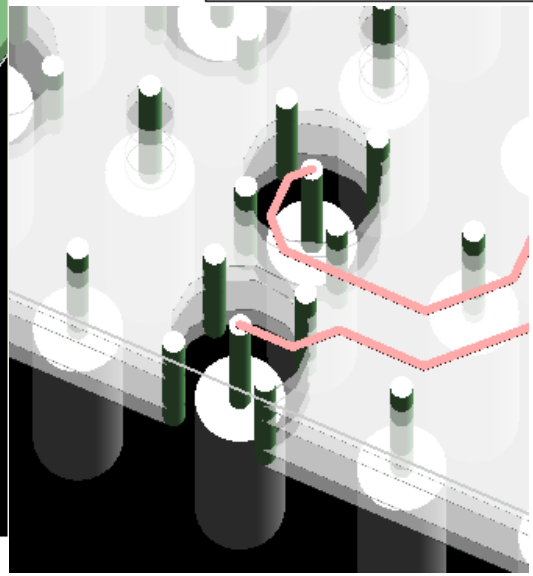
Cross section of lid seal

Package Design Aspect: SerDes RX and TX Design

- Co-axial ground via placement for all Rx and TX pairs
- Opening of the ground plane is optimized to reduce capacitance
- All Rx and Tx signals sandwiched between ground planes





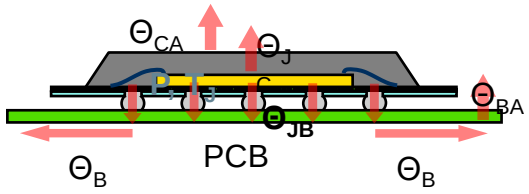


Thermal Management of Components in Space

- A cooling plate is normally attached between two boards within a system (box)
- Prefer no cooling plate attached to the top lid of the flip-chip CCGA (concerns on component reliability from vibration during launch stage)
- Since there is no air in space (vacuum condition), most of the heat from the junction can only be dissipated through the board
- The package's thermal resistance from junction-to-board (θ_{JB}) is the thermal parameter we can use to estimate the maximum power the product can handle

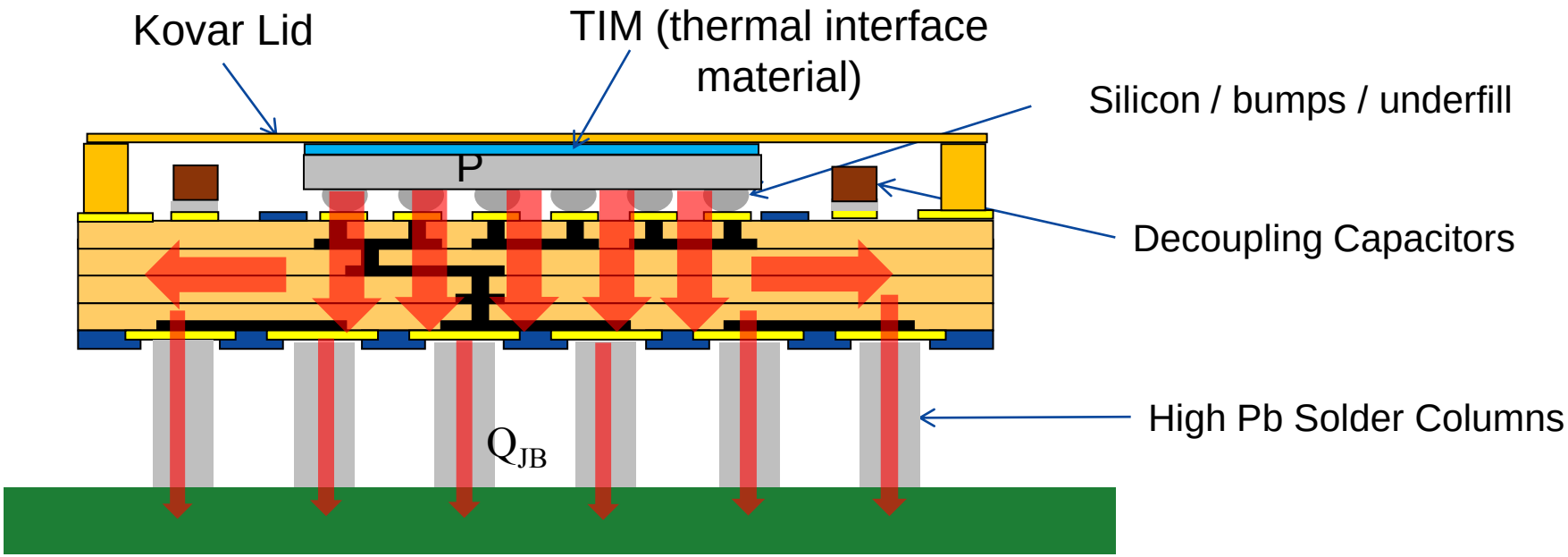
Heat Flow in Vacuum – Junction to Board

- Heat flow in a vacuum condition is through radiation and conduction which is from the die surface to the package, to the solder columns, to the PCB



Typical heat flow in air environment

$$\Theta_{JB} = (T_J - T_B) / Q_{JB} = 2.49\ ^{O}C/W \quad \ldots P = Q_{JB}$$



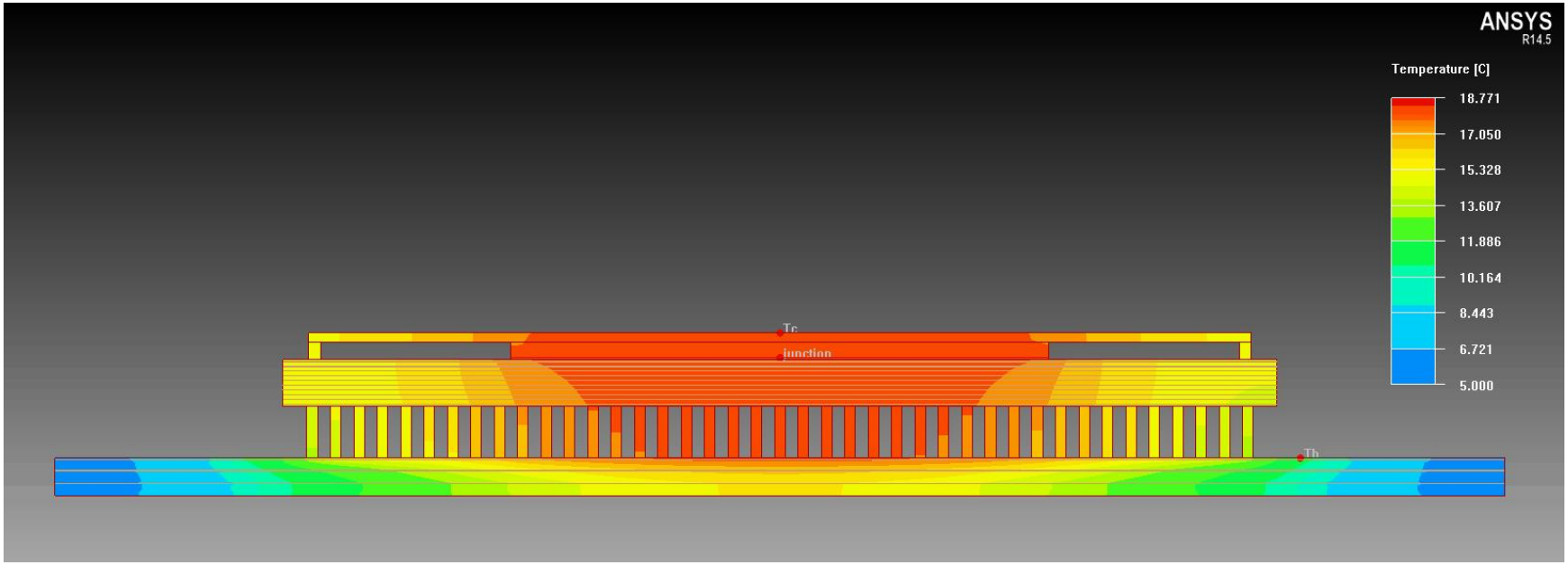
PCB Temperature @ 60 ^{O}C– 70 ^{O}C– 80 ^{O}C

RT4G150-CG1657 Thermal Resistance

Thermal resistance from junction-to-board

Simulation setup:

- An isothermal ring cold plate is placed around the edge of the PCB acting as the boundary condition.
- A temperature point monitor (*T_brd*) is placed on the board 1.0 mm from the package.
- Simulation is set to conduction heat transfer to ensure that all heat will be flowing through the bottom of the package.
- **Thermal resistance from junction-to-board = 2.49 C/W.**



Power Estimated Calculation For RTG4-CG1657 Package

- Estimate Θ_{JB} = 2.49 ^{O}C/W for CG1657

Θ_{JB} (^{O}C/W)	T_J (^{O}C)	T_B (^{O}C)	P (W)
2.49	125	60	26.1
2.49	115	60	22.1
2.49	105	60	18.1
2.49	95	60	14.1

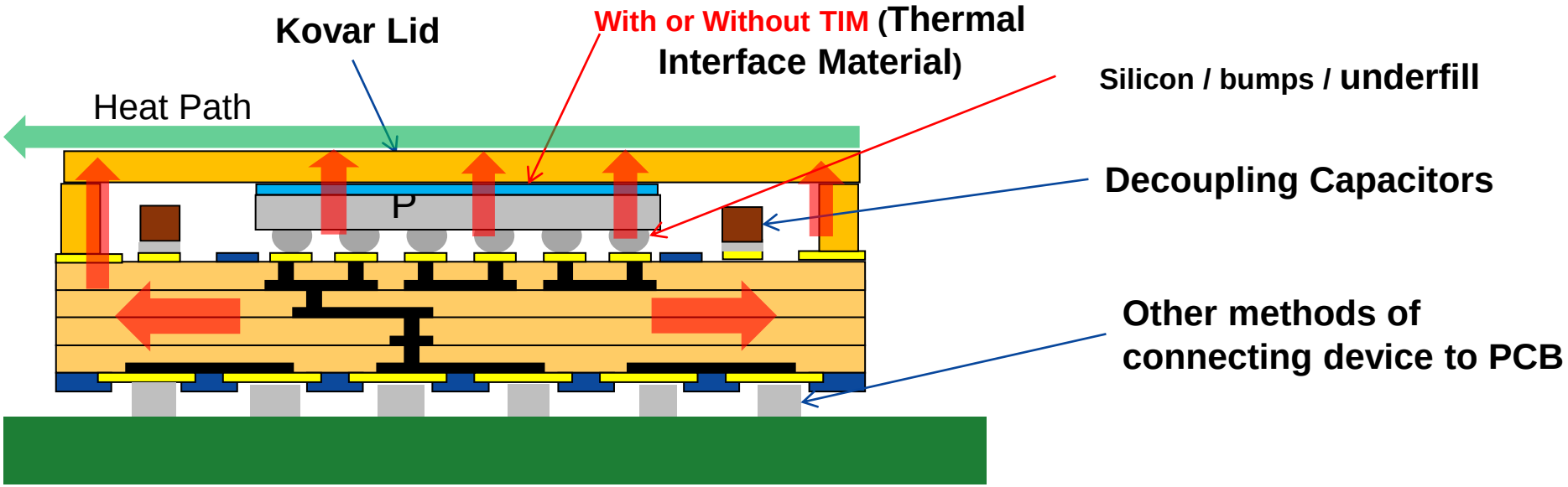
Θ_{JB} (^{O}C/W)	T_J (^{O}C)	T_B (^{O}C)	P (W)
2.49	125	70	22.1
2.49	115	70	18.1
2.49	105	70	14.1
2.49	95	70	10.0

Θ_{JB} (^{O}C/W)	T_J (^{O}C)	T_B (^{O}C)	P (W)
2.49	125	80	18.1
2.49	115	80	14.1
2.49	105	80	10.0
2.49	95	80	6.0

- T_B is the temperature measured by a thermocouple, placed 1.0 mm away from the package edge
- Typical design power: in 10W to 12W range

Potential Other Methods: Heat Flow in Vacuum – Junction to Case

- Heat path from the top of the lid as shown below. However, there will be some heat goes through the bottom of the package to PCB



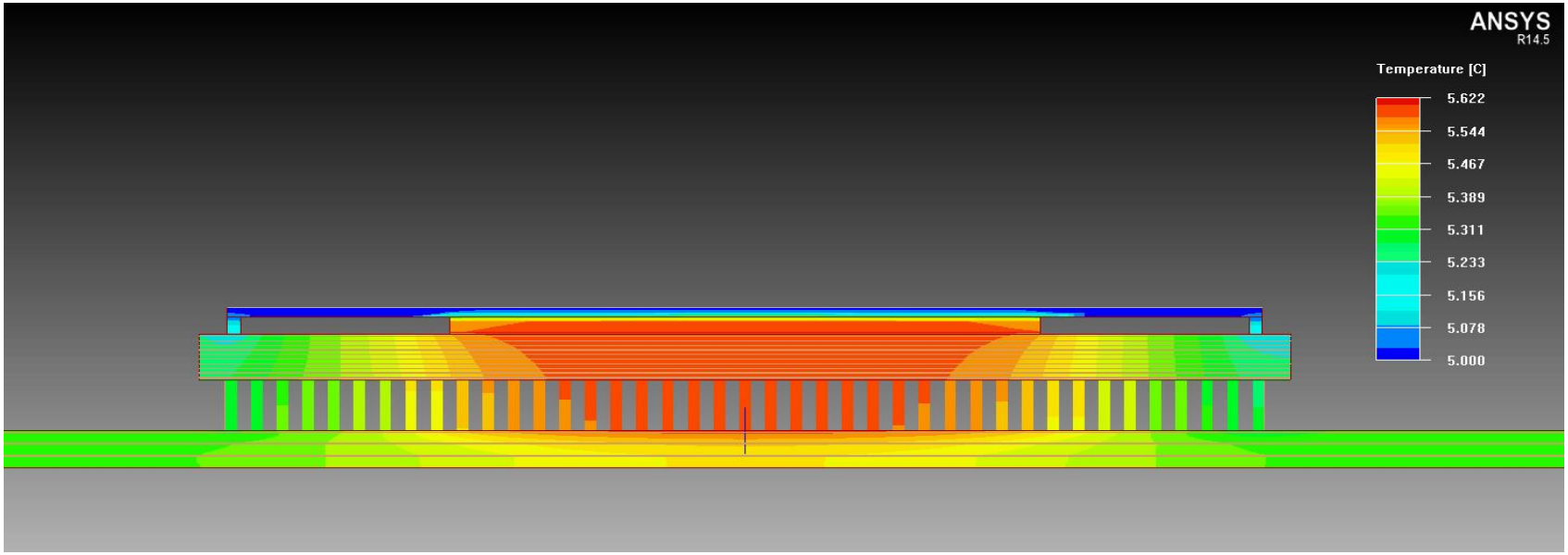
PCB Temperature @ 60 ^{O}C– 70 ^{O}C – 80 ^{O}C

RT4G150-CG1657 Thermal Resistance

Thermal resistance from junction-to-case (with TIM)

Simulation setup:

- An isothermal cold plate is placed at the top of the package lid acting as a boundary condition.
- A temperature point monitor (*T_case*) is placed on the top center of the package lid.
- Simulation is set to conduction heat transfer to ensure that all heat will be flowing through the package lid.
- **Thermal resistance from junction-to-case = 0.21 C/W.**

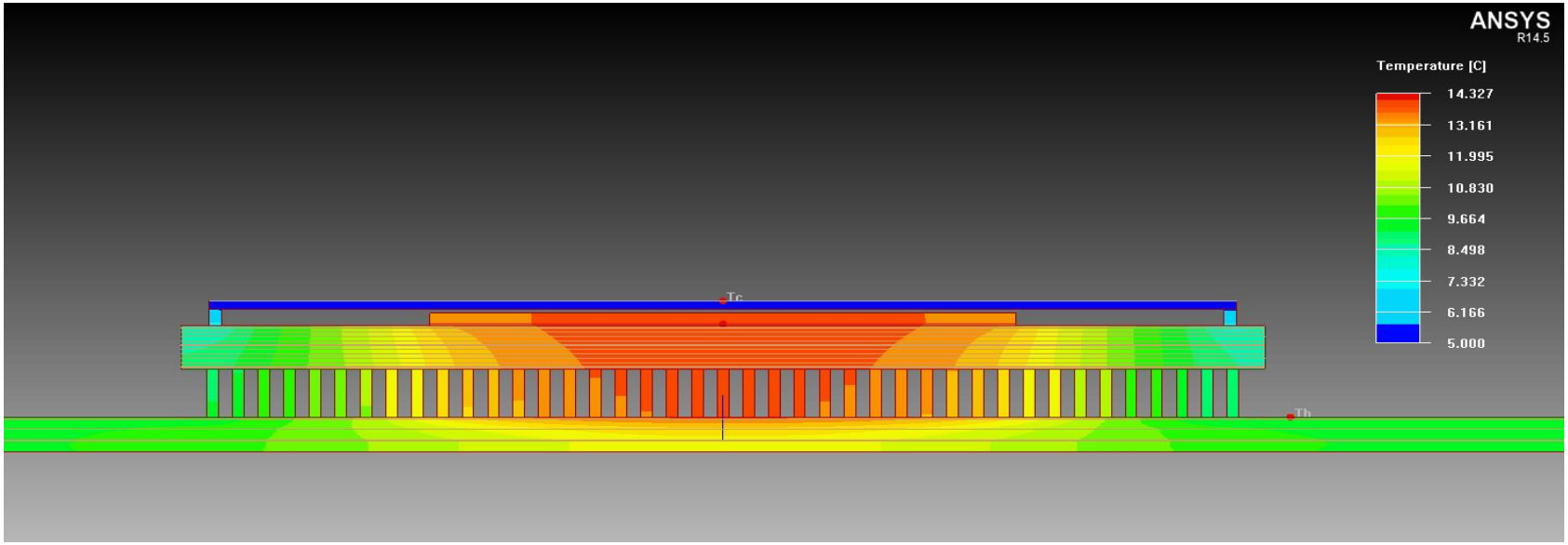


RT4G150-CG1657 Thermal Resistance

Thermal resistance from junction-to-case (without TIM)

Simulation setup:

- An isothermal cold plate is placed at the top of the package lid acting as a boundary condition.
- A temperature point monitor (*T_case*) is placed on the top center of the package lid.
- Simulation is set to conduction heat transfer to ensure that all heat will be flowing through the package lid.
- **Thermal resistance from junction-to-case = 3.12 C/W.**



Potential Other Methods: Heat Flow in Vacuum – Junction to Case

- Heat flow in a vacuum condition is through radiation and conduction which is from the die surface to the silicon, to the heatsink (Kovar Lid in this case)
- With TIM material attached to the lid:

$$\Theta_{JC} = (T_J - T_C) / Q_{JC} = 0.21\ ^{O}C/W \ \ldots P = Q_{JC}$$

- Without TIM material attached to the lid:

$$\Theta_{JC} = (T_J - T_C) / Q_{JC} = 3.12\ ^{O}C/W \ \ldots P = Q_{JC}$$

  - In both configurations, end users can attach some type of cooling plate on the top of the lid and connect it to a cooling system
  - Thermal dissipation from the system level needs to consider partial heat will pass through the bottom of the package then through the column pins, or the land pads through connectors for LGA configuration

Summary

- CCGA (column grid array package) continues to be the platform for the new generation RT device for Space
- Key Features of RTG4-CG1657 Package
  - PME package capacitor—fully meet MIL-PRF-123 and MIL-PRF-THIN “T” grade
  - Ceramic material (same material as CQ packages and other CCGA)—reliable
  - Hermetical seam seal between Kovar seal ring to Kovar lid—reliable
  - Capable of meeting MIL-PRF-38535 Class V (not just Y)
  - Eutectic solder bump as interconnect technology—mature process and reliable
  - Stable assembly processes
- Target for fully MIL-PRF-38535 Class V flow qualification
- Package design optimizing performance and minimizing noise
- Heat dissipation in Space has been considered during design phase
- Daisy chain packages are available for end customers to optimize board level assembly as well as board level reliability test

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Support Data for CCGA (Ceramic Column Grid Array) for Space Applications

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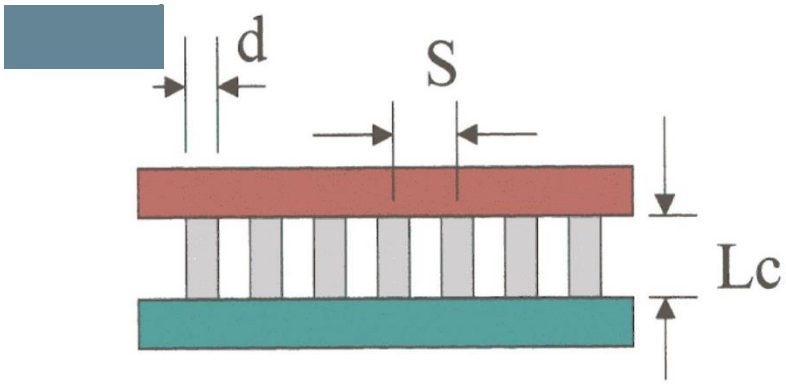
Packaging Platform for Space-Column Grid Array Solution



ΔT_1 = temperature change of board

ΔT_2 = temperature change of component

α_1 = CTE of the board

α_2 = CTE of the component

S = distance from neutral point (DNP)

E = modulus of elasticity of column

d = diameter of column

L = standoff height of column

$$\sigma_{max} \approx \frac{1.5 \cdot (\alpha_1 \cdot \Delta T_1 - \alpha_2 \cdot \Delta T_2)(S \cdot E \cdot d)}{L^2}$$

Solder Columns Configurations

- Three basic types of solder columns
  - Wire column
    - High-lead wire with Sn63-Pb37 fillets
  - Solder column interposer
    - High-lead solder held in array with additional ceramic substrate
  - Reinforced solder column
    - High-lead wire core with spiral wrapped copper ribbon attached with Sn63-Pb37 fillets

Note: Reinforced columns show a significant performance advantage in comparison to other types of solder columns. See board level testing data result

High-lead solid wire core
---Sn20-Pb80 or Sn15-Pb85
Tin plated copper ribbon
Hot solder coating
---Sn63-Pb37

Board Level Reliability Comparison

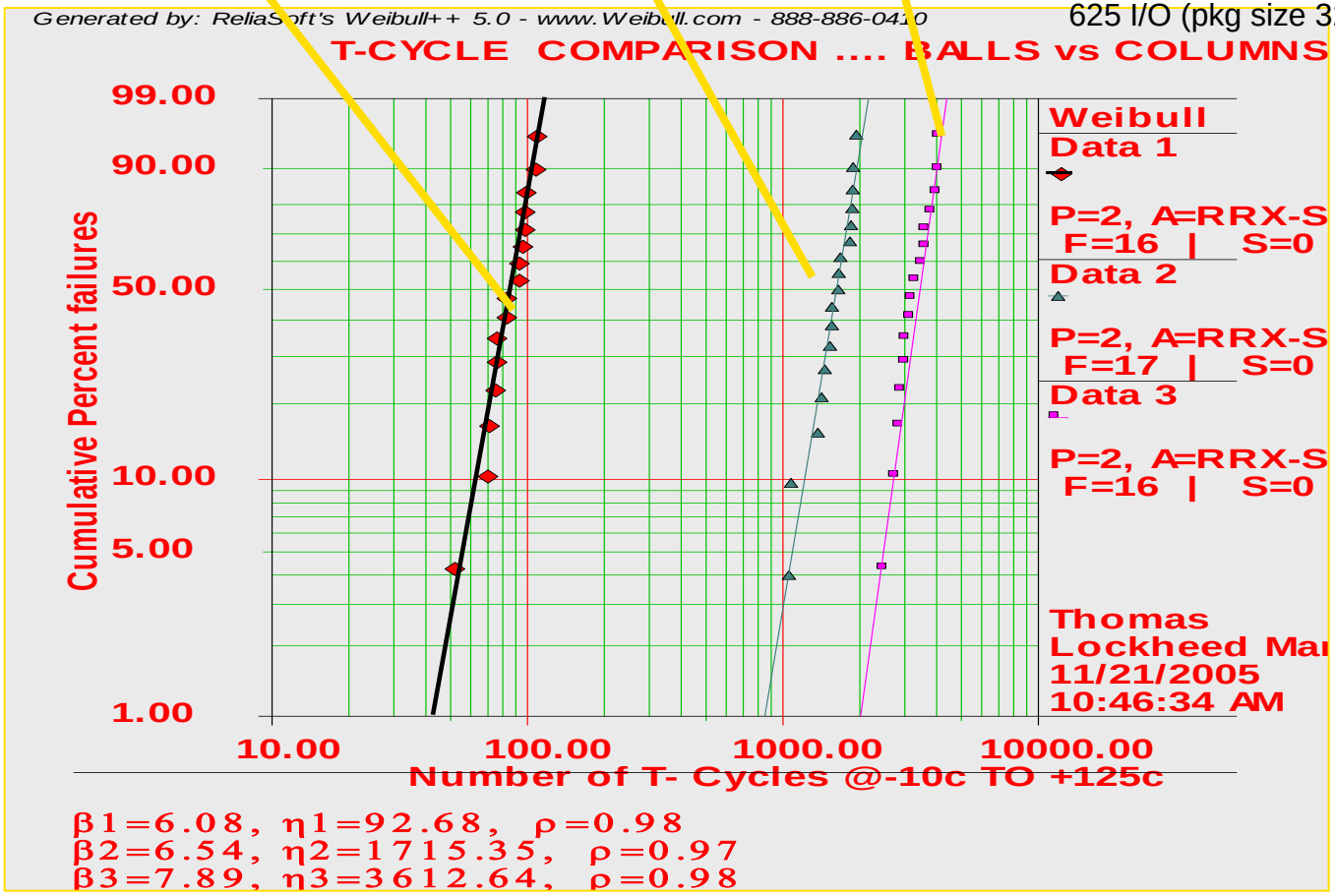
Reinforced Columns

BGA

Wire Columns

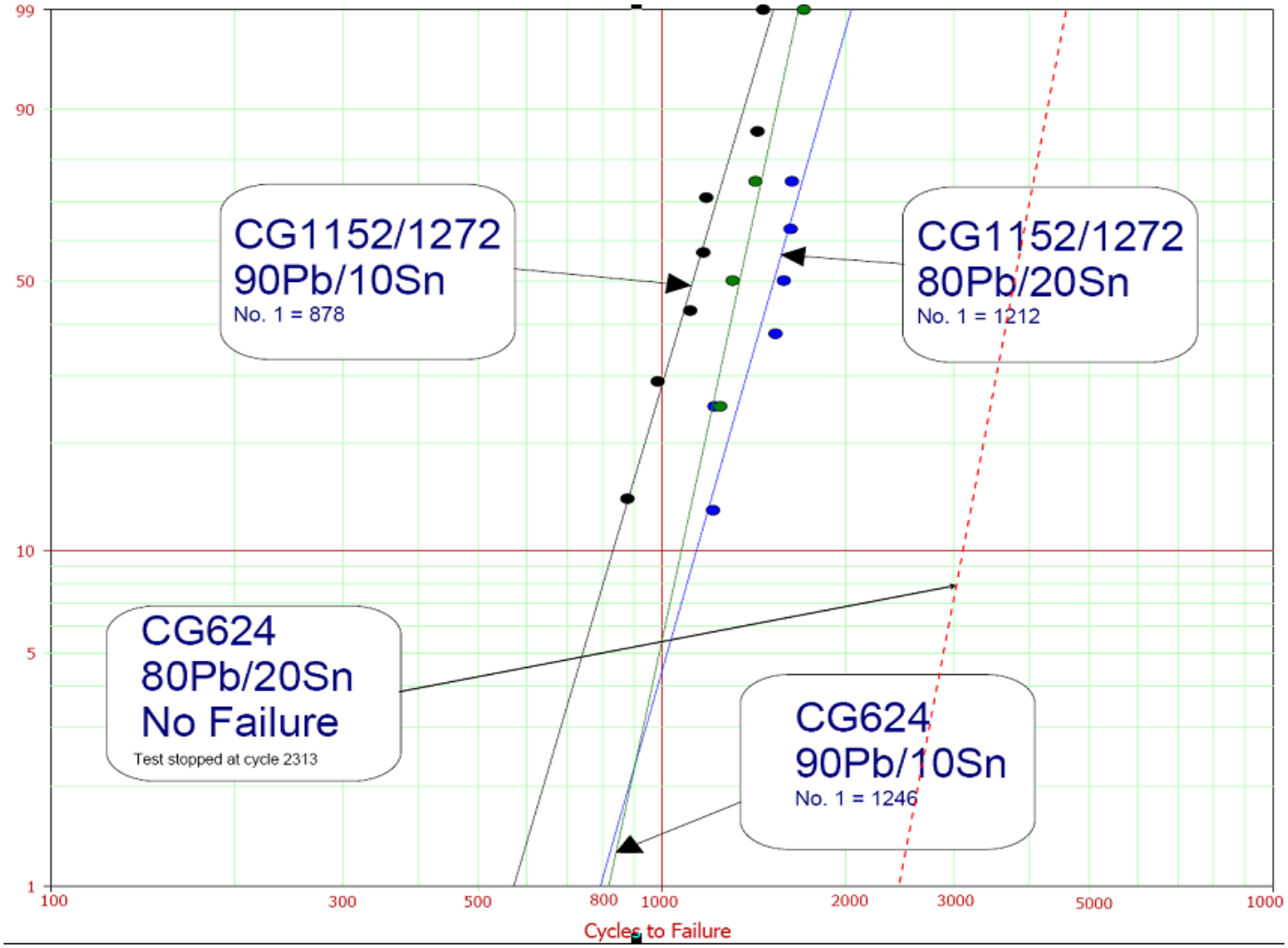
Results (from Six-Sigma)

All parts ceramic with 1.27mm pitch
625 I/O (pkg size 32mm)



Board level Testing (-55C° to 105 C°) on Microsemi Current CCGAs

Lognormal Probability Distribution of Cumulative Fails vs. Temperature Cycles



Lognormal Probability of Cumulative Fails vs. thermal cycles----up to 2313 cycles

Coffin Mason Relation

Lognormal Probability Distribution of Cumulative Fails vs. Temperature Cycles

$$\text{A. F.} = (\Delta T_t * DNP_t / \Delta T_f * DNP_f)^{1.9} \times (F_f/F_t)^{1/3} \exp\left[1414\,(1/T_{maxf} - 1/T_{maxt})\right]$$

Where :
N_f = Field Cycles
N_t = Test Cycles
ΔT_t Test Cycle Temperature Range
ΔT_f = Field Cycle Temperature Range
DNP_t = Test Distance to Neutral Point
DNP_f = Field Distance to Neutral Point
F_f = Field Cycle Frequency
F_t = Test Cycle Frequency
T_{maxf} = Maximum Field Temperature
T_{maxt} = Maximum Field Temperature

Test Conditions :

Temp. Range
-55 105

160 = ΔT_T, ΔTemp for Test

12 = F_T, cycles / day for Test

378 = T_{MaxT}, Max Temp for Test

*21.5mm = DNP for Test for CG624***
22.6mm =DNP for Test for CG1152
22.7mm =DNP for test for CG1272

** Note:

Distance of corner pin to the center point of the package (neutral point)

Used to related temperature cycle result to field condition

CCGA Field Life Projection for Typical Satellite Applications

Based on Temperature cycling Data—for 80Pb/20Sn re-enforce column

	Field Cycles (CPD)	Field Temp Range	Field Delta Temp	DNP (mm)	Field Max Temp (C)	N.01 Test Cycles	Acceleration Factor	Projected Cycles	YEARS OF LIFE
CG624	18	20 to 45	25.00	21.5	45.0	2,313	78.88	182,445.8	27.8
CG1152	18	20 to 45	25.00	22.6	45.0	1,212	78.88	95,600.7	14.6
CG1272	18	20 to 45	25.00	22.7	45.0	1,534	78.88	120,999.5	18.4
CG624	12	70 to 85	15.00	21.5	85.0	2,313	110.67	255,970.0	58.4
CG1152	12	70 to 85	15.00	22.6	85.0	1,212	110.67	134,126.9	30.6
CG1272	12	70 to 85	15.00	22.7	85.0	1,534	110.67	169,761.3	38.8

Why Hermetic Package?

Space Challenges for Complex Non-hermetic Packages

- **Vacuum:**
  - Outgassing, offgassing, property deterioration
- **Foreign Object Debris (FOD)**
  - From the package threat to the system, or a threat to the package
- **Shock and vibration**
  - During launch, deployments and operation
- **Thermal cycling**
  - Usually small range; high number of cycles in Low Earth Orbit (LEO)
- **Thermal management**
  - Only conduction and radiation transfer heat
- **Thousands of interconnects**
  - Opportunities for opens, intermittent - possibly latent
- **Low volume assembly**
  - Limited automation, lots of rework
- **Long life**
  - Costs for space are high, make the most of the investment
- **Novel hardware**
  - Lots of "one offs"
- **Rigorous test and inspection**
  - To try to find the latent threats to reliability

ONE STRIKE AND YOU'RE OUT!

Note: this slide is from July 2011 JC13 meeting on Non-hermetic for Space

Hermetic Package Ensure Reliability for Space

Hermeticity

- NASA prefers hermetic packages for critical applications
- Hermeticity is measureable, assuring package integrity
- Only 3 tests provide assurance for hermetic package integrity:
  - Hermeticity – nothing bad can get in
  - Residual or Internal gas analysis – nothing bad is inside
  - Particle Impact Noise Detection – no FOD inside
- NON-HERMETIC PACKAGE INTEGRITY IS HARD TO ASSESS - NO 3 BASIC TESTS
- Non-hermetic packages expose materials' interfaces that are locked away in hermetic ones

Note: this slide is from July 2011 JC13 meeting on Non-hermetic for Space

Summary of CCGA as Platform for Space

- Extended qualification data on wire bond version of CCGA (ceramic column grid array)
- Successful introduction of CCGA, and widely adapted by end customers for Space applications. Various flight programs have been used or in the planning stage to use CCGA packages
- Building on the current successful introduction of CCGA for Space, Microsemi is taking on to introduce flip-chip CCGA for Space

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