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### **RTG4 Software Features**

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#### Agenda

- Design Considerations
- Design Software Options
- System Controller Suspend Mode
- SPI Slave Programming
- Programming Options
- Package Pins Changes
- Conclusion



#### **Design Considerations – RAM EDAC**

- RAM blocks have built in EDAC (SECDED)
  - SECDED is single error correct, double error detect
  - Optional at word widths 18 bits and higher. Not available at smaller word widths
  - Scrubbing is not built in to the RAM EDAC. Use Microsemi IP (CoreEDAC) or build your own in fabric
- EDAC has flags that shows single correction has happened or double detection has happened
- Software provides GUI Configurators for the LSRAM and uSRAM blocks
- To access the built in EDAC features, use the RAM Configurator instead of RAM inference through Synthesis
- If EDAC is not needed, RAM inference is supported and available with Synplify synthesis tools



## **Design Considerations - SERDES**

- SERDES Configurator and automatic configuration initialization
- Two type of SERDES blocks
  - Support for PCIe, EPCS, and XAUI
  - Support for EPCS, XAUI (no PCIe support)
- Configurators in Catalog reflect the different SERDES blocks types

Catalog		
SER	DES 🔍 🗸	Simulation Mode
Name	A	Version
▲ Perip	herals	
RT	G4 High Speed Serial Interface - EPCS and XAUI - with initialization	1.0.102
RT	G4 High Speed Serial Interface - PCIe, EPCS and XAUI - with initializati	1.0.102
Documer User's Guid	itation: je	
Descripti High Speed	on: J Serial Interface - EPCS and XAUI - with built-in initialization	

- SERDES configurator has built-in automatic initialization mechanism
  - Initialization is generated automatically based on the user selected configuration



## **Design Considerations - FDDR**

- FDDR Configurator and automatic configuration initialization
- Two FDDR blocks (East FDDR and West FDDR)
- FDDR configurator accessed from Catalog and location selection is made in the Configurator GUI

Catalog		Eabric External Memory DDR Controller Configurator
FDDR 🔍 🗸 🗸	Simula:	
Name	Version	
Memory & Controllers		Import Configuration Export Configuration Restore Defaults
RTG4 DDR Memory Controller with initialization	1.0.102	General Memory Initialization Memory Timing
Documentation: User's Guide		Identification     O West FDDR     O West FDDR
Description: RTG4 DDR Memory Controller		

- FDDR configurator has built-in automatic initialization mechanism
  - Initialization is generated automatically based on the user selected configuration



# **Design Considerations - SpaceWire**

CCC/PLL Configurator and hardened SpaceWire RX Clock/Data Recovery



- Each CCC has a built in SpaceWire Clock/Data Recovery circuit
- SpaceWire interface used for command-and-control and data
  - Data and Strobe are XORed to recover SpaceWire clock
  - Hardwired and SET protected
  - Delay compensation option is available in IO block to align data and SpaceWire clock
  - 16 SpaceWire Clock/Data Recovery circuits on each RTG4





## **Design Considerations - CCC**

CCC/PLL configurator accessed from Catalog

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SpaceWire options are part of the CCC Configurator

Catalog		- • • • · · · ·
CCC 🔄 🗸 🖝 Simulation Mode	Basic Advanced PLLOptions	
Name Version  Clock & Management  RTG4 Clock Conditioning Circuit (CCC) 1.1.206	/i     REFCLX     Actual data is shown in blue.     Exact Value       Dedicated Input Pad 0 ~     /i     0.000     100     MHz       CCC Internal ~     /i     PBCLK     0.step(c) ~     RX0 Clock Recovery ~     +	LOCK 1 Y0 3.454 ns 2 GLO GLO_YO_EN
Documentation: <u>User's Guide</u> Description: "RTG4 Clock Conditioning Circuit (CCC)"	FPGA Fabric Input 0  CX0  FPGA Fabric Input 0  CX1  FPGA Fabric Input 1  CX1  FPGA Fabric Input 2  FPGA Fabric Inp	□ Y1 3.461ns ☑ Q.1 Q.1_Y1_PN
Dedicated Input Pad 0 CLK_PAD0 Dedicated Input Pad 1 CLK_PAD1 MHz MHz MHz MHz	CLX2     MH2       FPGA Fabric Input 3     MH2       Dedicated Input Pad 0     0.00 deg (0.00 m)       UC Configure as differential     100       CLX PADD M     100       Dedicated Input Pad 1     MH2       CLX Configure as differential     100       CLX Configure as differential     100       October 2     MH2	E 72 G.2_Y2_EN
Dedicated Input Pad 2 Configure as differential CLK_PAD2 50 MHz Dedicated Input Pad 3 Configure as differential CLK_PAD3 MHz	Configure as differential CK_PA02 Configure as differential CK_PA03 Configure as differential CK_PA03 Configure as differential CK_PA03 CAK_PA01 C CK_PA01 C CK_PA01 C CK_PA00 C CK_PA00 C CK_PA00 C CK_PA00 C CK_PA00 C CK_PA03 C	(13) (13) (13) (13) (13) (13) (13) (13)
• RX Clock Recovery Block 0             • Strobe               • CLK_PAD1               • CLK_PAD0	Strobe CLK_PAD2 *	, ,
RX Clock Recovery Block 1     Data     CLK_PAD3     CLK_PAD2		

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#### **Design Considerations - uPROM**

- The RTG4 FPGA fabric has one embedded programmable read only memory (uPROM) block (10,400 36-bit words)
  - Used for storing program data such as initialization data for LSRAM and uSRAM blocks
- uPROM Configurator and design flow
  - uPROM configurator accessed from Catalog
  - Create clients based on:
    - Address
    - Number of words
    - Memory file

	<b>4</b> -	Simi	ulation Mode
Name			Version
Memory & Controller	s		
RTG4 uPROM			1.0.101

Add Clients to System	User clients in uPROM	
Usage statistics Available memory(36-bit words): 10400 Used memory(36-bit words): 0 Free memory(36-bit words): 10400	Client Name Start Address 36-bit words	
Used space	Add Data Storage Client	



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#### **Design Considerations - uPROM**

- Update the uPROM content without recompiling or running through the Place & Route flow
  - Only programing file re-generation is required





## **Design Software Options - SET Filter**

- Single Event Transient (SET) Mitigation
  - SW provides a Compile option to enable and disable the SET mitigation in the FPGA fabric
  - When the option is checked, SET filters are turned on globally to help mitigate radiation-induced transients. By default, this box is unchecked
    - Individual block SET Filter control is planned for future versions of the Software
  - The setting is propagated to Verify Timing, Verify Power and Back-annotated Netlist for you to perform Timing/Power Analysis
  - There is 943ps Data Setup Time increase with SET filter ON





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### **Design Software Options - Radiation**

- Option to specify radiation value (in Krad)
  - Valid range is from 0 to 100
- The setting is propagated to Verify Timing, Verify Power and Back-annotated Netlist for you to perform Timing/Power Analysis

Project settings	
Device selection Device settings Design flow Analysis operating conditions Simulation options DO file Waveforms Vsim commands Timescale Simulation libraries RTG4	Selected part <b>RT4G150-CG1657M</b> is defined to use MIL range. You can change the operating conditions for <b>Timing and Power a</b> Temperature range(C) MIL  Core voltage range(V) MIL  MIL
	Range    MIL    MIL    MIL    MIL    MIL    Radiation (krad)    0



#### **Design Software Options - Probes**

- RTG4 has two types of Probes
  - One Live Probes channel
  - One dedicate Live capture interface
    - Ability to capture FF contents at the same time and then read back over time.
  - Reserve your pins for probing if you intend to debug using SmartDebug
  - Use SmartDebug debug tool to access the non-invasive probes within the RTG4 devices
- Check "Reserve pins for probes" option to reserve dedicated probe pins
  - If not reserved, probe pins can be used as regular user I/Os

Project settings           Device select	ion					Managers Jam School 1
Device setting Design flow	js	I/O settings Default I/O techno	ology:	LVCMOS 2.5V		Please use the I/O Editor to change
Analysis oper Simulation of DO file	ating conditions ptions	Reserve pins f	for probes		_ •	individual I/O attributes.
Waveforn Vsim con	าร าmands	📝 Reserve Pins f	for SPI			
Timescal Simulation like	e praries					



#### **System Controller Suspend Mode**

- Use this mode to protect the device from unintended behavior due to single event upset (SEUs) in the System Controller
- The System Controller can be held in Suspend mode after device initialization
  - JTAG interface is disabled when System Controller is in Suspend mode
  - System Controller activate if the device is power-cycled or if a hard reset is applied, but it returns to Suspend mode once power-up is completed.
  - System Controller Suspend mode setting is set during device programming
  - The setting is only accessible through the programming file loaded into the device
- To reprogram or debug the device while in System Controller Suspend mode, drive the TRSTB pin High
  - If the TRSTB pin is Low, all the other JTAG input signals are blocked from activating the System Controller
  - When in space, while operational, the TRSTB pin must be held Low



### **System Controller Suspend Mode**

- Enable System Controller Suspend mode Software Option
  - Option is part of a programming bitstream settings
    - Use this option for ground test of design
- You can also exit System Controller Suspend Mode and enable JTAG interface by driving TRSTB high during device power up

			Programming Bitstream Settings
Tool			
⊳	Create Design		Enable System Controller Suspend mode
⊳	Create Constraints		✓ Disable JTAG interface
⊿	Implement Design		
V	Synthesize		Disable SPI interface
	Verify Post-Synthesis Implementation		Disable Fabric Frase Write Verify
	📸 Compile	N	
	Place and Route		Disable Probe Read/Write
	Edit Constraints		Disable Direct Check
	Verify Post Layout Implementation		
⊳	Edit Design Hardware Configuration		
⊿	Configure Programming Options		Selected settings:
	🙀 Configure User Programming Data		System Centraller System Made is enabled and
	Configure Programming Bitstream Settings		JTAG interface is disabled when TRSTB is low during
	Configure Ontions		device power up. The user can exit System 👘 🗐
	Compute options		Controller Suspend Mode and enable JTAG interface
	Program Design		by ariving TRSTB high during device power up.
$\triangleright$	Debua Desian		
			Reset to default
			Help OK Cancel

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#### **System Controller Suspend Mode**

- A RESET\_STATUS signal can be monitored to confirm the status of the System Controller
- You get access to this signal by instantiating SYSTEM\_RESET\_STATUS macro from Libero SoC Catalog
- RESET\_STATUS output port will go high if the System Controller is in reset
  - System Controller Suspend Mode option enabled in Libero device setting

Catalog				₽×	SD Sd* 🗗 🗙
SYSCT		<b>Q</b> -	Simulation Mode	(i) <del>-</del>	
Name	<u>^</u>		Version		
▲ Macro SY	SCTRL_RESET_S	TATUS	1.0		
					SYSCTRL_RESET_STATUS_0
Vendor: M Library: A Name: SY Version: 1	/licrosemi Actel Macros SCTRL_RESET_ST/ 1.0	ATUS			RESET_STATUS



### **SPI Slave Programming – Reserve SPI Pins**

- Dedicate SPI (Slave only) interface as alternative method for programming
  - The SPI block is part of the System Controller
  - SPI-Slave Libero programming through FP5 will be supported in future SW releases
- If the System Controller is not held in Suspend mode, the dedicated SPI-slave interface can be used for programming functions
  - SPI Slave communicates with a remote device such microprocessor that initiates the download of the programming bit stream to the device
- Reserve Pins for SPI
  - Check this box to reserve (four) pins for SPI functionality in Programming

Project settings	structure production of the same increase the same line in the same in
Device selection Device settings Design flow Analysis operating conditions Simulation options DO file Waveforms Vsim commands Timescale	I/O settings Default I/O technology: LVCMOS 2.5V ▼  Please use the I/O Editor to change individual I/O attributes. ✓ Reserve pins for probes ✓ Reserve Pins for SPI



## **Programming Bitstream Settings**

- Disable SPI interface
  - SPI interface is disabled when TRSTB is low during device power up
  - You can enable SPI interface by driving TRSTB high during device power up.
  - For this option to be available, you must reserve pins for SPI in the project settings of the Libero project (refer to the previous slide)
- Disable JTAG interface
  - Disabled when Enable System Controller Suspend mode is Checked
  - Disabled when TRSTB is low during device power up

Programming Bitstream Settings
Enable System Controller Suspend mode
☑ Disable JTAG interface
☑ Disable SPI interface
✓ Disable Fabric Erase/Write/Verify
✓ Disable Probe Read/Write
☑ Disable Digest Check
Selected settings: - Disable Fabric Erase/Write/Verify, JTAG interface, and SPI interface when TRSTB is low during device power up. The user can enable Fabric Erase/Write/Verify, JTAG interface, and SPI interface by driving TRSTB high during device
Reset to default Help OK Cancel



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# **Programming Bitstream Settings**

- Disable Fabric Erase/Write Verify
  - You can enable Fabric Erase/Write/Verify by driving TRSTB high during device power up
- Disable Probe Read/Write
  - For this option to be available, you must reserve pins for Probe in the project settings of the Libero project (refer to previous slides)
- Disable Digest Check
  - Disables all Fabric reads, such as verify digest, read digest, or reading design or programming information in DEVICE\_INFO when TRSTB is low during device power up.
  - You can enable Digest Check by driving TRSTB high during device power up

Programming Bitstream Settings
Enable System Controller Suspend mode
Disable JTAG interface
Disable SPI interface
Disable Fabric Erase/Write/Verify
Disable Probe Read/Write
🔽 Disable Digest Check
Selected settings: - Disable Fabric Erase/Write/Verify when TRSTB is low during device power up. The user can enable Fabric Erase/Write/Verify by driving TRSTB high during device power up. - Disables Probe Read/Write when TRSTB is low
Reset to default Help OK Cancel



#### **CG1657 Package Pins**

- Two devices are available in Libero SoC Software
  - RT4G150\_ES CG1657
  - RT4G150 (production) CG1657
- Software generated package pins for RT4G150\_ES are not compatible with pins generated for RT4G150 device
  - Due to SpaceWire enhancements
- The following pin mapping tables are provided to help you start designing your board
   <u>SpaceWire Pin Mapping from RTG4 ES/MS Silicon to PROTO/Flight Silicon</u> <u>SpaceWire Pin Mapping from RTG4 ES/MS Silicon to PROTO/Flight Silicon for</u> <u>RTG4 Development Kit</u>



#### Conclusion

- Libero SoC Software provides full design automation from RTL to Debug
  - Includes Synphony, Synplify, Modelsim, Identify
  - With support for other simulation tools
- ECC support through RAM Configurator
- Automatic initialization for SERDES and FDDR based on user configurations
- SpaceWire RX Clock/Data recovery configuration through CCC configurator
- SET Filter On/Off option to help mitigate radiation-induced transients
- System Controller suspend mode to protect the device from unintended behavior due to single event upset (SEUs)
- Enable/disable System Controller Suspend mode using Programming Bitstream settings
- SPI programming alternative option to JTAG programming
- Debug options using Live Probe and Capture
- uPROM Configurator support





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# **Thank You**



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