Power Matters.™

RTG4 Architecture Details

Microsemi Space Forum 2015

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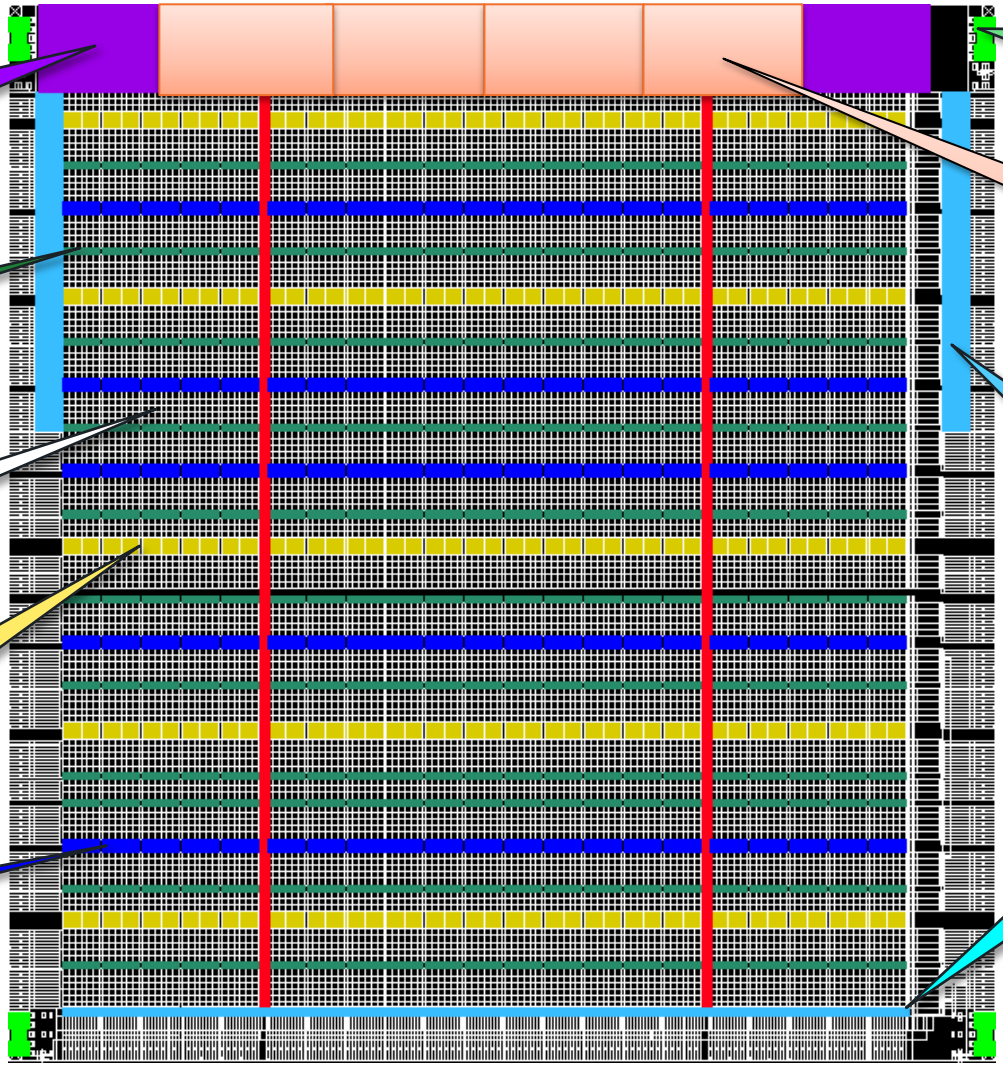
Agenda

- RTG4 Architecture Details
  - FPGA Fabric
  - Embedded Memories
  - DSP Mathblock
  - General Purpose IO
  - Clock Conditioning Circuit (CCC) and PLL
  - SpaceWire Clock Recovery
  - SERDES
  - FDDR Controller
  - System Controller
  - Summary of Radiation-Mitigated Features
- RTG4 Architecture, Performance and Power Comparison
- Conclusion

RTG4 Layout Overview



PCIe SERDES (EPCS, XAUI)

Mathblocks

Logic Cluster

LSRAM (24Kb)

µRAM (1Kb)

PLL and CCC SpaceWire CDR

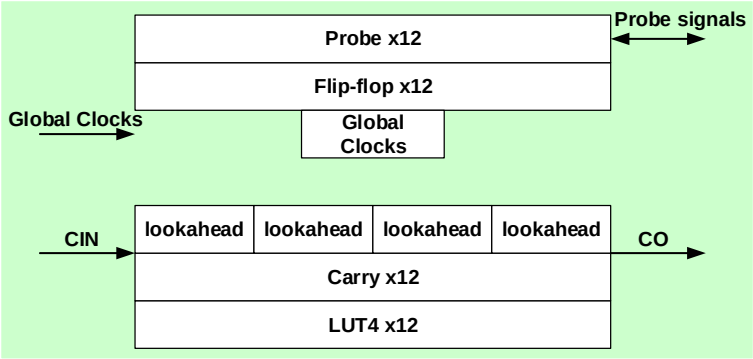
SERDES (EPCS, XAUI)

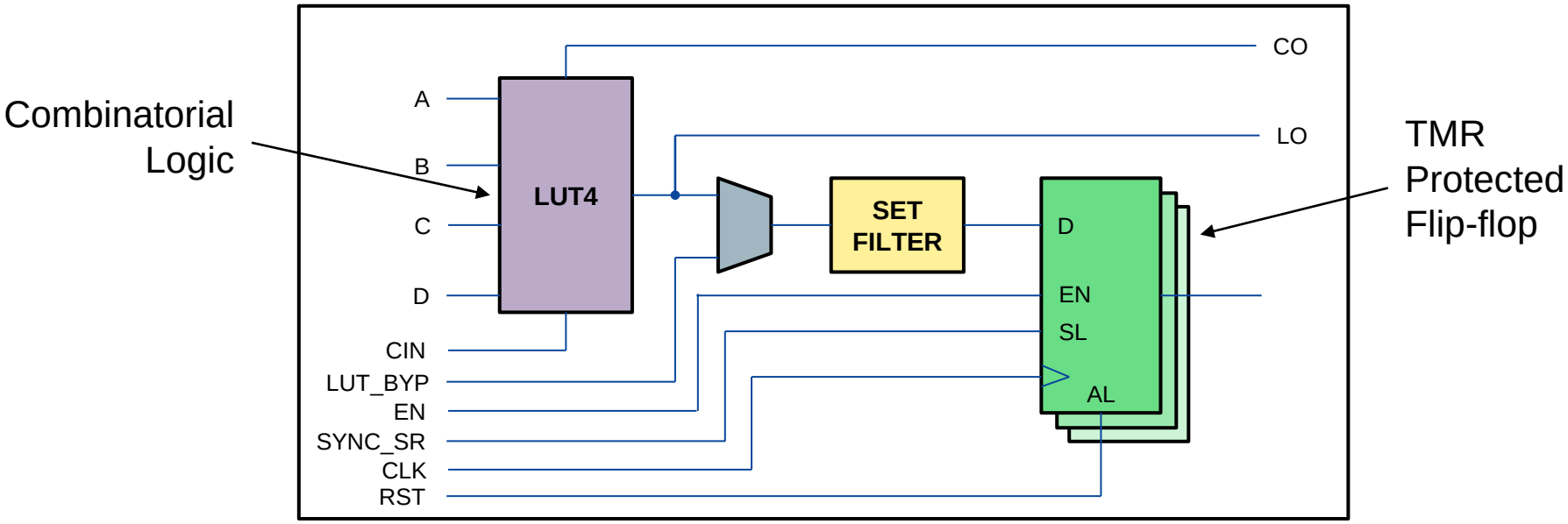
DDR Controller

µPROM

FPGA Fabric: Logic Cluster

- Each Logic Cluster contains 12 Logic Elements
  - 12 TMR Flip-flops with probe logic
  - ⇒ Built-in radiation mitigation
  - ⇒ Capture logic states for debugging purpose
  - 12 LUT4 with fast carry arithmetic logic
  - ⇒ Efficient routing >95% module utilization

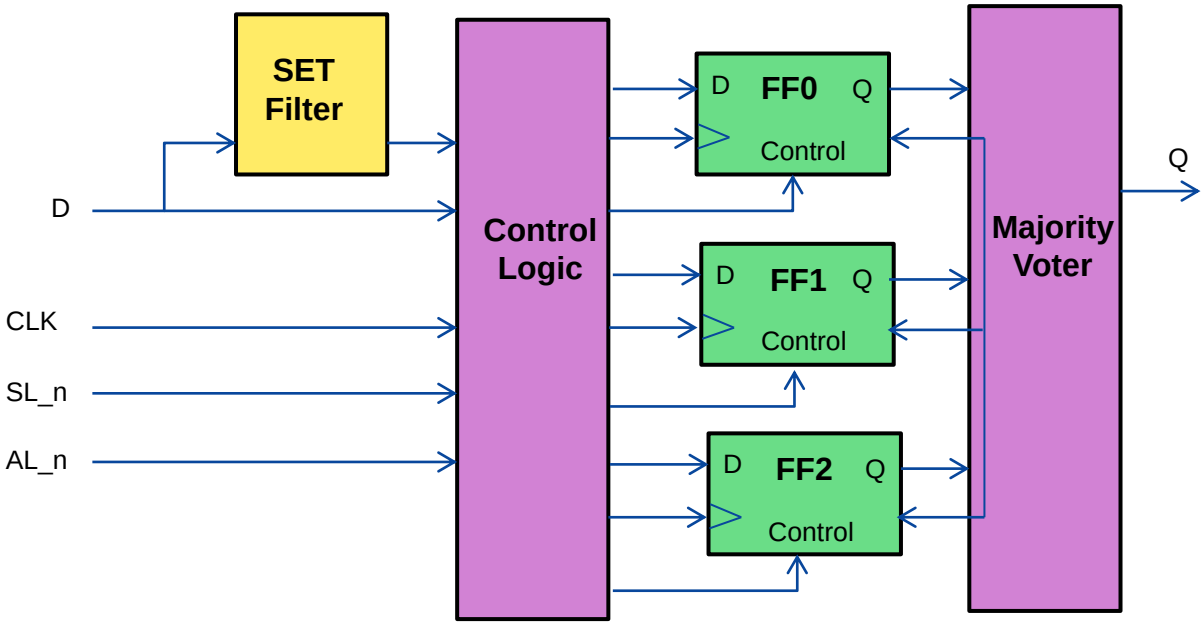




RTG4 Logic Element (LE)

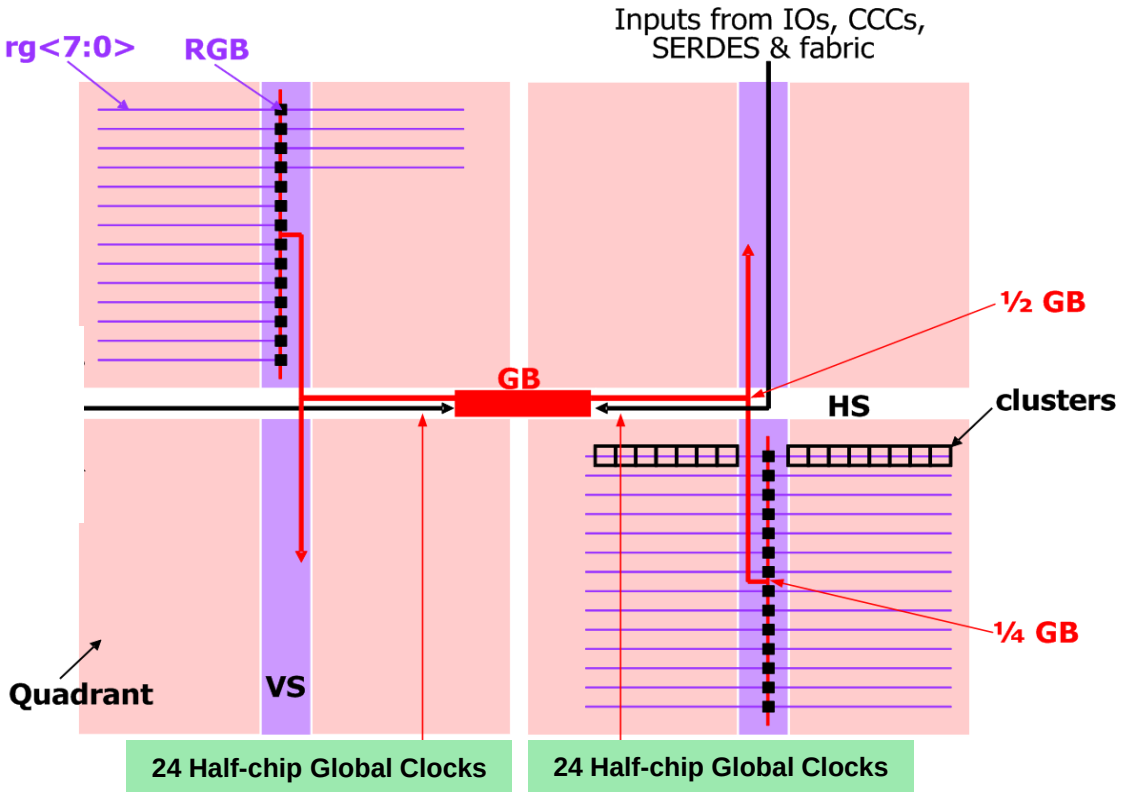
FPGA Fabric: Flip-flops

- Built-in SET filter can eliminate SET glitches up to 600 ps
  - Delay added to data path in SmartTime has been seen to vary from 943 ps to 1.255 ns
- Radiation-hardened Control Logic for clock/reset (synchronous load) and reset/probe (asynchronous load)
- Radiation-hardened asynchronous Majority Voter ensures SEU immunity
- Proprietary triple-module redundancy (TMR) for maximum radiation mitigation while maintaining high performance



Global Clock

- 24 full-chip Global Clocks or 48 half-chip Global Clocks
  - Complete radiation hardening by triple-redundant clock paths
- Global Clocks can come directly from:
  - Output of CCC/PLL
  - Global Buffer (GB)
  - Dedicated Global I/Os



Embedded Memories: SRAM

- Radiation Tolerance:
  - Resistant to multi-bit upset
  - Built-in optional Error Detection and Correction (EDAC) without background scrubbing
  - Shortened Hamming code with single error correct, double error detect (SECDED)

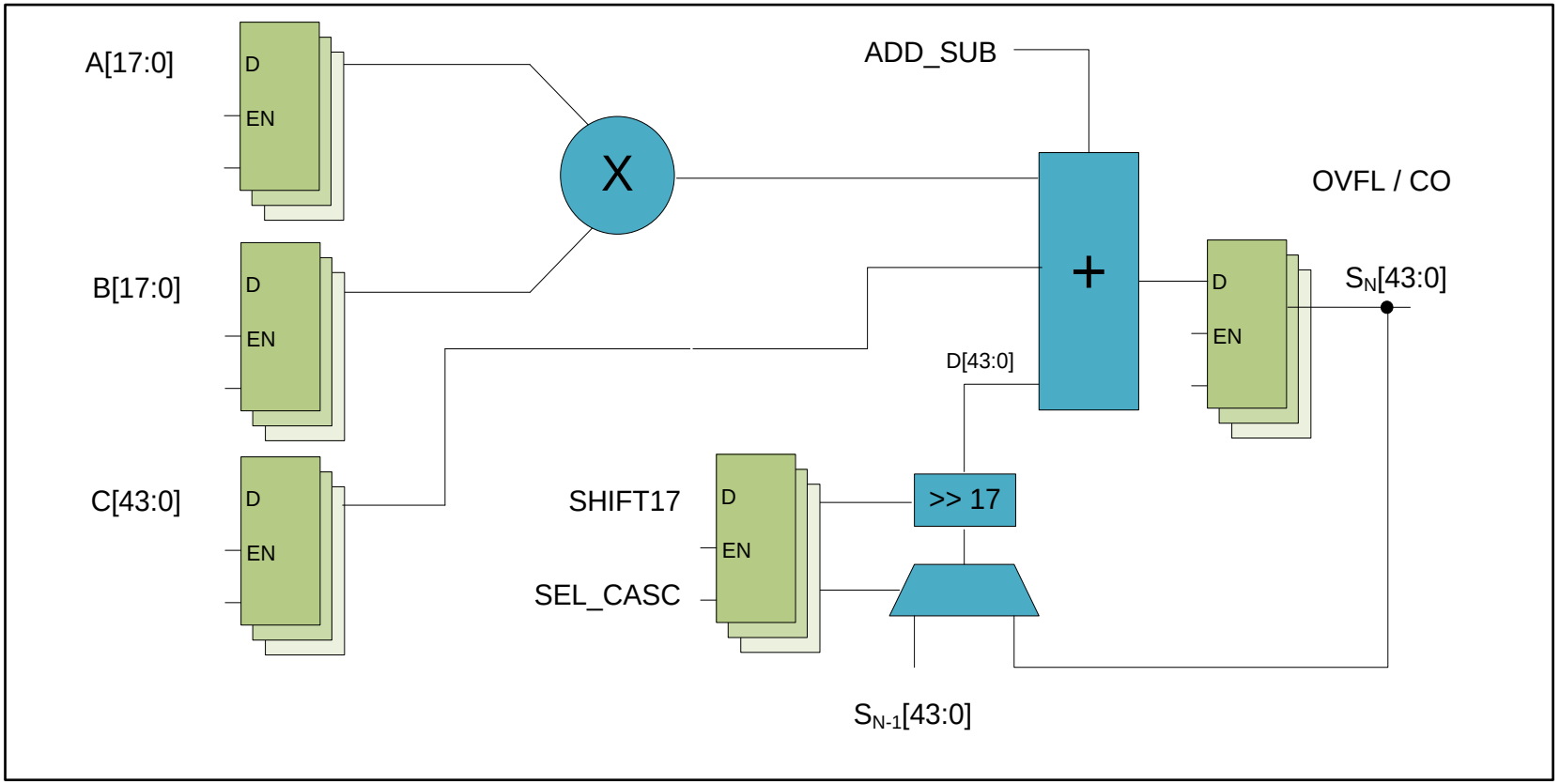
Data Port	Width (bits)	
User data width	18	36
User data width with shortened Hamming code	24	48

- Large SRAM (LSRAM) – Up to 24 Kbit
  - Dual-port and two-port options
  - Supported bit widths: x36, x18, x12 and x9
  - Built-in EDAC available for x36 and x18
- Micro SRAM (uSRAM) – Up to 1.5 Kbit
  - Three-port SRAM
  - Supported bit widths: x18, x12 and x9
  - Built-in EDAC available for x18
- LSRAM and uSRAM contents can be pre-loaded from uPROM at power-on

Embedded Memories: uPROM

- Non-volatile memory based on FPGA configuration cell
  - Configuration upset immune
  - TID >= 100KRad
- Up to 374 Kbits storage for DSP coefficients
- Initialize RAMs and registers from uPROM
  - Power-on initialization
  - Modification of coefficients during normal operation
  - RAM scrubbing
- Read performance of 50 MHz x 32-bits

DSP Mathblock



- 18 x 18 multiplier with advanced accumulate
- High performance for signal processing throughput
- Optional SEU-protected registers on inputs and outputs (including C input)

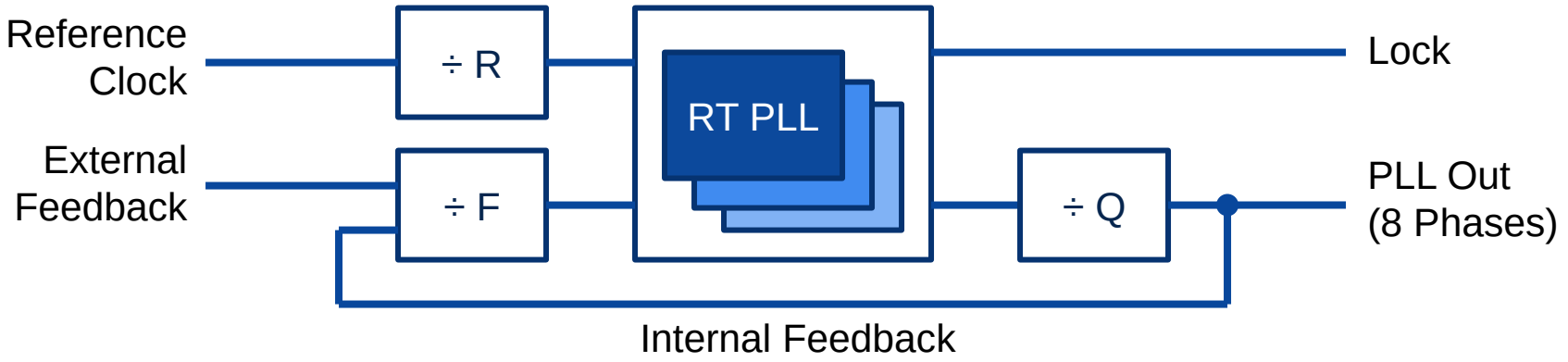
General Purpose IO

- Three IO types: MSIO up to 3.3V, MSIOD and DDRIO up to 2.5V
- Programmable Input Delay available
- Cold Sparing supported with all IO supplies powered while the core supply is tied to ground
- Radiation Tolerance:
  - IO Registers have the same built-in TMR structure as the fabric flip-flops
  - MSIO and MSIOD input buffers are triplicated to be protected from SET

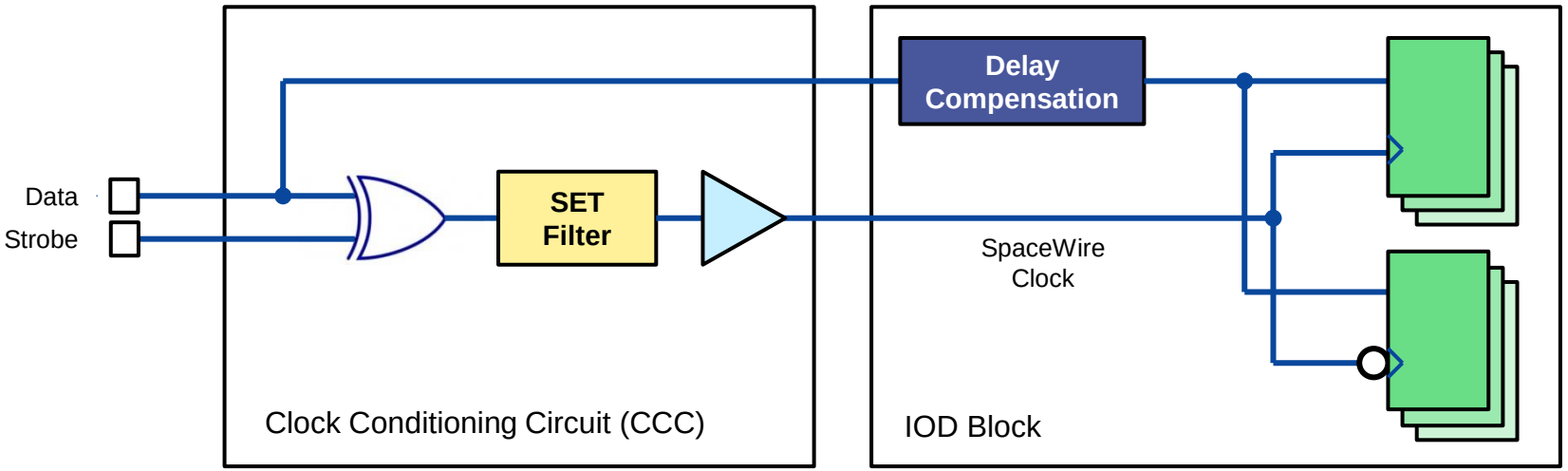
IO Standards		IO Types		
		MSIO (Up to 3.3V)	MSIOD (Up to 2.5V)	DDRIO (Up to 2.5V)
Single-ended	PCI (3.3V)	Yes	No	No
	LVTTL / LVCMOS (3.3V)	Yes	No	No
	LVCMOS (1.2V to 2.5V)	Yes	Yes	Yes
Voltage Reference	HSTL 1.5V (Class I)	Yes	Yes	Yes
	HSTL 1.5V (Class II)	No	No	Yes
	HSTL 1.8V	Yes	Yes	Yes
	SSTL 2.5V (Class I & II)	Yes	Yes	Yes
	SSTL 1.8V (Class I & II)	Yes	Yes	Yes
	SDRAM 3.3V	Yes	No	No
True Differential	LVDS	Yes	Yes	No
	RSDS	Yes	Yes	No
	Mini LVDS	Yes	Yes	No
	LVPECL (input only)	Yes	No	No
	MLVDS	Yes	Yes	No

CCC and PLL

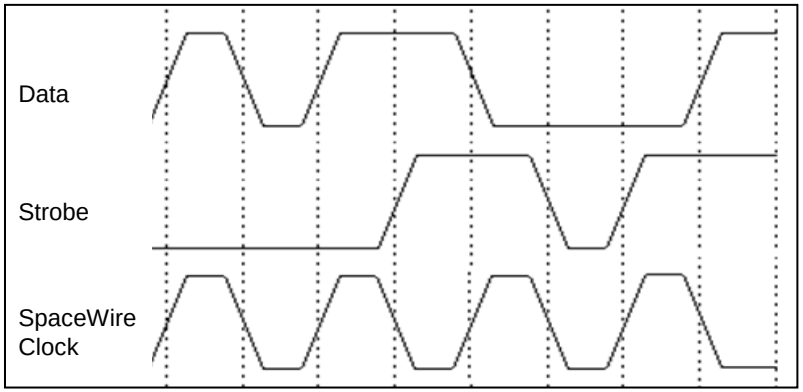
- Radiation-Tolerant PLLs are used in CCC, SERDES and DDR blocks
  - PLL output frequency up to 400 MHz
  - Two CCC/PLL per corner. Two SpaceWire CDR circuits per CCC
- Triple module redundant (TMR) PLL in internal feedback mode
  - Reference clock is fed back to all 3 sub-PLLs independently
  - Sub-PLL is SEL immune
- Single PLL in external feedback mode
  - PLL output travels through clock network and is fed back to PLL
  - Common mode used for clock network delay compensation
  - Only 1 sub-PLL is enabled in this mode
  - Sub-PLL is SEL immune



SpaceWire Clock Recovery



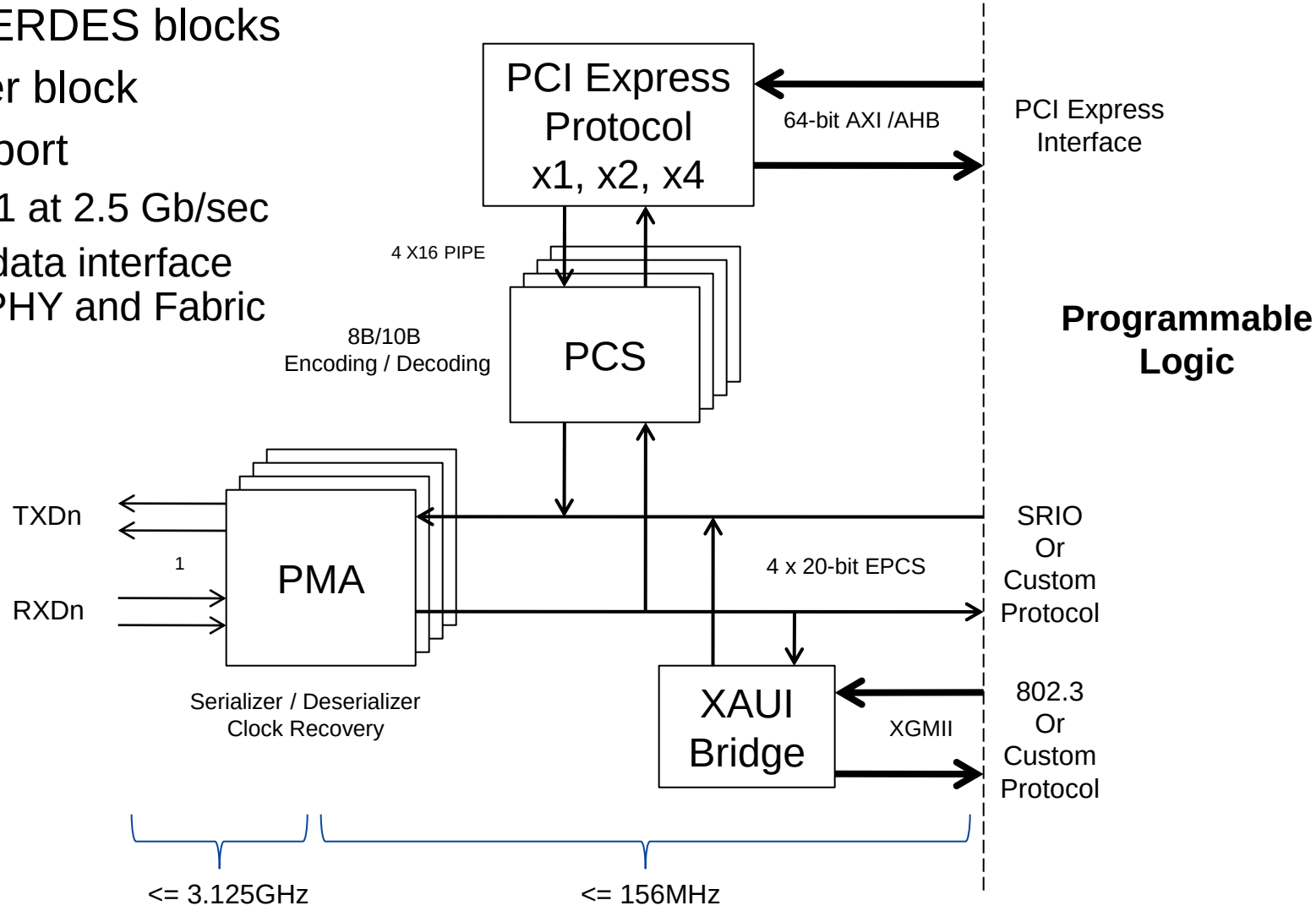
- SpaceWire interface used for command-and-control and data
  - Data and Strobe are XORed to recover SpaceWire clock
  - Hardwired and SET protected
  - Delay compensation available to align data and SpaceWire clock
  - 16 SpaceWire Clock Recovery circuits on each RTG4



Unique Microsemi RTG4 Feature

3.125 Gb/sec SERDES

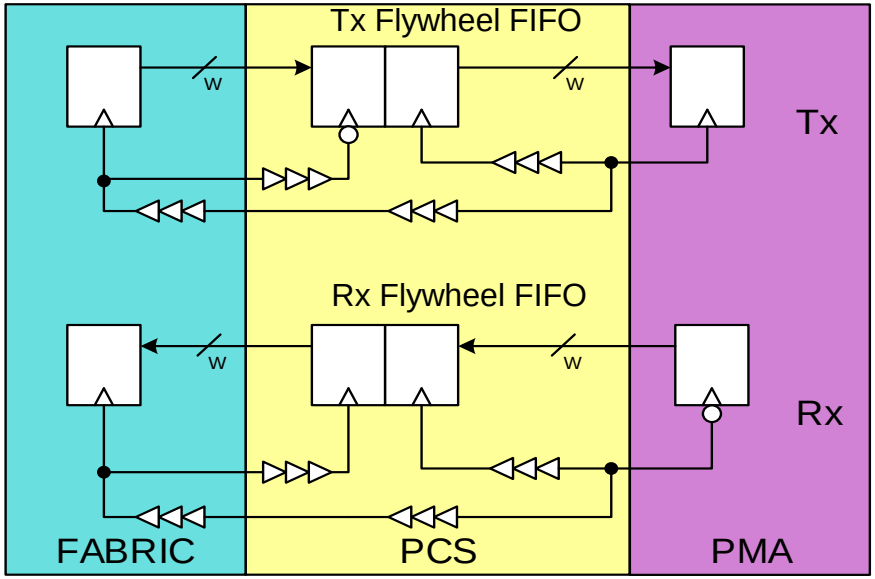
- Up to 6 SERDES blocks
- 4 lanes per block
- PCIe Support
  - PCIe Gen1 at 2.5 Gb/sec
  - AXI/AHB data interface between PHY and Fabric



SERDES (Cont.): EPCS and XAUI

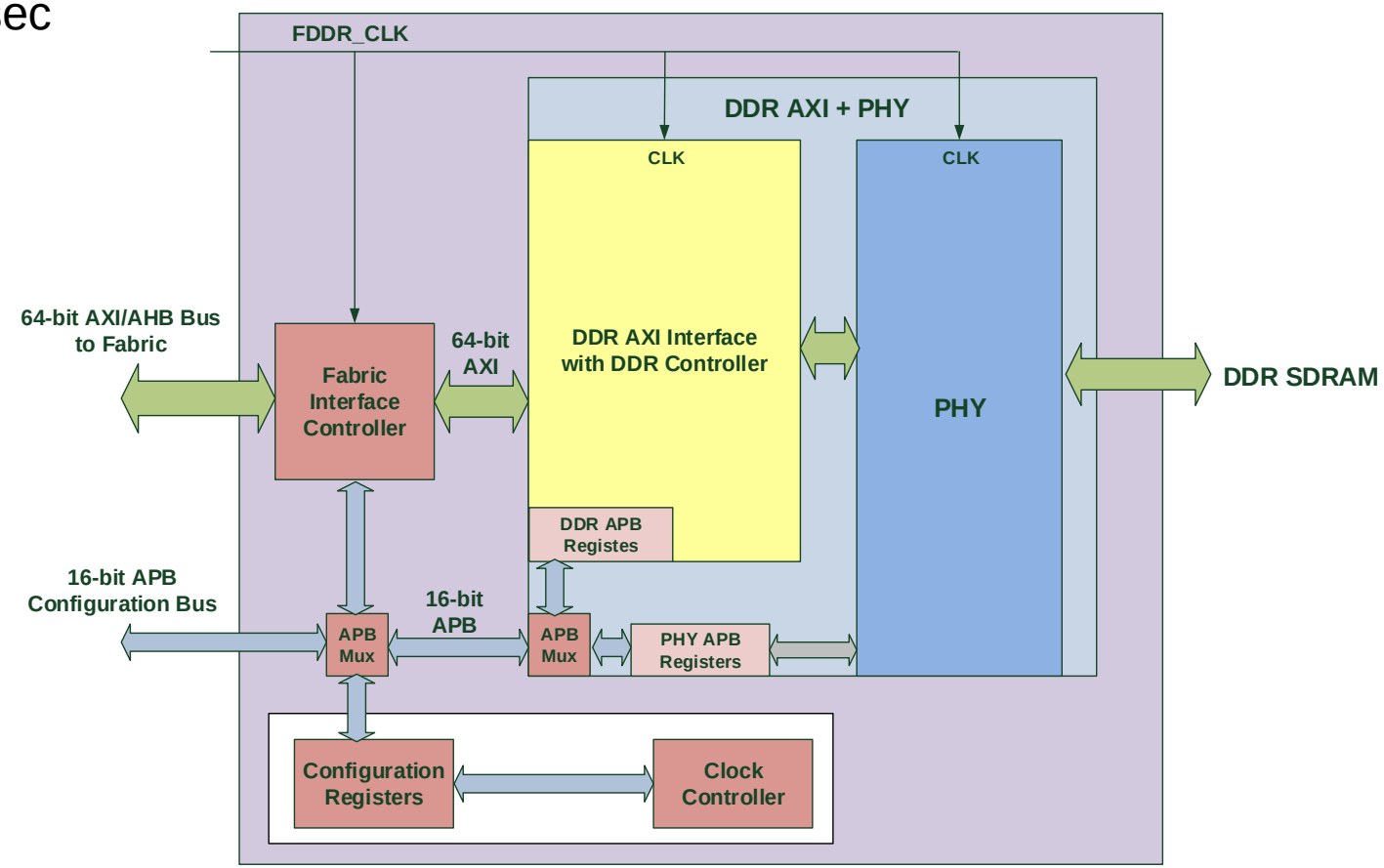
- EPCS and XAUI modes are improved from commercial SERDES (For example: SmartFusion2 and Igloo2)
  - A flywheel FIFO improves read timing to the FPGA fabric and provides clock compensation to transfer Rx data to the Tx clock domain in the FPGA fabric
  - Dedicated routing from SERDES clocks to the global clock network

⇒Efficient routing and high performance up to 3.125 Gb/sec



FDDR Controller

- 2 FDDR Controllers support:
  - DDR2, DDR3 and LPDDR1
  - 8/16/32 bit data bus. Built-in EDAC for x16 and x32
  - Up to 667 Mb/sec



System Controller

- System Controller manage:
  - Programming through JTAG and SPI Slave interface
  - Power-On Reset (POR) Generator

- System Controller Suspend Mode protects device from unintended configuration due to radiation upsets
  - JTAG_TRSTB must be held Low and this mode must be set in Libero SoC software
  - To exit this mode, hold JTAG_TRSTB High and reprogram the device with System Controller Suspend Mode turned off in software

- System Controller Suspend Mode control bit is stored in a flash cell and immune from configuration upset

Summary of Radiation-Mitigated Features

Features	Radiation Mitigation				
	SEL Immune	SEU Immune By Design	SEU Mitigated with Optional EDAC	SET Immune by Design	SET Mitigated with Optional SET Filter
Configuration Flash Memory	YES	YES			
FPGA Fabric					
Combinatorial Logic	YES				YES
Flip-flop	YES	YES			
Global Clock and Reset	YES			YES	
LSRAM and uSRAM					
SRAM Data	YES		YES		
SRAM Control	YES			YES	
DSP Mathblock	YES	YES			YES
MSIO/MSIOD Input Buffer	YES			YES	
PLL/CCC Internal Feedback	YES			YES	
PLL/CCC External Feedback	YES				
SERDES					
SERDES Control (Register Maps)	YES	YES		YES	
FDDR					
FDDR Control (Register Maps)	YES	YES		YES	
50-MHz RC Oscillator	YES			YES	

RTG4 Architecture, Performance and Power Comparison

RTG4 vs. RT/RH SRAM FPGAs

	RT4G150	Xilinx XQR5VFX130 (SIRF)	Xilinx XQR4VSX55	Xilinx XQR4VFX60	Xilinx XQR4VFX140	Xilinx XQR4VLX200	Atmel ATFS450
Non-TMR FF TMR FF	151,824	81,920	55,296 *18,432*	56,880 *18,960*	142,128 *47,476*	200,448 *66,816*	23,104
LUT4 LUT6	151,824	*106,496* 81,920	55,296	56,880	142,128	200,448	46,208
18x18 MAC 24x18 MAC	462	*448* 320	512	128	192	96	None
SRAM (Mbits)	5.2	10.7	5.7	4.1	9.9	6	0.18
SERDES Lanes	24	18	None	None	None	None	None
In-orbit Reconfig	To be tested	Unlimited	Unlimited	Unlimited	Unlimited	Unlimited	Unlimited

- Note that *italic data* were converted to compare with RTG4
- Assumptions:
  - 1 SIRF LUT6 = 1.3 x RTG4 LUT4
  - 1 SIRF Mathblocks = 1.4 x RTG4 Mathblocks

⇒ RTG4 is the largest RT FPGA with the most TMR flip-flops, combinatorial logic and SERDES

RTG4 vs. SIRF

Resources	Microsemi RT4G150	Xilinx V5QV SIRF
LUT4 + TMR FF	**151,824**	
LUT6 + TMR FF	-	81,920
User IO (non-SERDES)	720	836
RAM Mbits	5.2	10.7
UPROM Kbits	**374**	-
18x18 MAC Blocks	462	-
25x18 MAC Blocks	-	320
SERDES lanes	**24**	18
DDR2/3 SDRAM Controller	**2x32**	-
Globals	24	32
PLLs (Rad Tolerant)	**8**	6
SpaceWire CDR Circuits	**16**	-
PCI Express Endpoints	2	3
CG1657	✓	
CG1752		✓

- 46% More Flip-Flops
- 30% More Combinatorial Logic
- 6 More SERDES Lanes
- 16 SpaceWire CDR Circuits

RTG4 vs. SIRF Performance Comparison

- Performance benchmark was done to understand RTG4 performance with respect to SIRF using a wide range of benchmark designs

- Benchmark designs:
  - 106 internal benchmark designs:
    - Standard designs typically used for performance benchmarking, including customer designs, IP cores, and basic functions
    - Advanced designs with high demand on long routing tracks and more complex functions
    - DSP designs optimized for our technology
  - 1 real world design:
    - Channelized application (up to 24 channels) consuming a significant amount of DSP, logic and RAM

Internal Designs: Performance Result

SW Settings	SIRF	RTG4
Design Tool	ISE 13.2	Libero SoC
Synthesis Tool	Synplify	Synplify
Operating Cond.	MIL, Worst voltage	MIL, Worst voltage
Device & Speed	Only 1 device	RT4G150
Speed Grade	Only 1 speed grade	-1
TID (Krad)	0	0
SET Filter Value	~ 2.1 ns	~ 1.255 ns

Geomean	RTG4	SIRF	RTG4 with SET	SIRF with SET
All Designs	1.00	1.02	0.87	0.74
Adv. Designs	1.00	0.56	0.93	0.49
DSP Designs	1.00	0.75	0.85	0.59

⇒RTG4 is 15% faster than SIRF with SET filter

⇒RTG4 is significantly faster than SIRF in Advanced and DSP designs

Real World Design: Performance Result

- Resource utilization:
  - RTG4 could integrate up to 22 channels
  - SIRF only integrated 16 channels and already 99% full
  - The 22-channel design had 22.4% more logic than 16-channel design
    - The 24-channel design did not fit in either part

- Performance:

Clock Domain	RTG4	SIRF	Notes
External Clock (MHz)	150.6	115.2	Long critical net delay 7.6 ns
External System Clock (MHz)	37.1	42.4	
Half Sample Clock (MHz)	168.9	103.5	Long critical net delay 8.2 ns
Global Clock Bus (Mhz)	50.6	52.4	

⇒For large design, RTG4 maintains comparable performance while having more resources

RTG4 vs. SIRF Power Comparison

- Goal to compare RTG4 and SIRF power consumption in a highly utilized design switching at 175 MHz using:
  - RTG4 Power Calculator v2c, available on RTG4 website
  - SIRF Power Calculator v14.3.2, available on Xilinx website
- Use Model in RTG4
  - 70% LUT4, 53% flip-flops
  - 96% LSRAM blocks
  - 100% DSP Mathblocks
  - 18 SERDES lanes, 1 PCIe

Condition	Static 25C	Static 85C	Static 125C	Total 25C	Total 85C	Total 125C
Process	**Typical**	**Typical**	**Typical**	**Typical**	**Typical**	**Typical**
RTG4 (W)	0.14	0.49	1.26	11.416	11.766	12.536
SIRF (W)	1.89	3.932	7.173	12.671	14.712	17.954

⇒RTG4 has lower total power. RTG4 has significant advantage in Static power, while SIRF has lower Dynamic due to 1V core.

Conclusion

- RTG4 comprehensive and robust architecture offers a complete solution for high-speed signal processing applications
- True Radiation-tolerant FPGAs with built-in mitigation throughout the device
- Significant improvement in performance while maintaining low power

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