RTG4 ES Development Kit Release Notes

The RTG4™ ES Development Kit provides space designers and developers with an evaluation and development platform for the latest Radiation-tolerant High-speed Signal Processing FPGAs family, RTG4. The RTG4 ES development board features a RT4G150 Engineering Sample (ES) device in a Ceramic Ball Grid Array (CBGA) package with 1,657 pins. More information can be found at http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/rtg4-development-kit

This Release Notes provides information on unsupported features and known issues which have been identified in the RTG4 ES development board.

1. RTG4 ES development board is intended for hardware functional verification only. It should not be used for space flight applications. It should also not be used for applications or activities which require the quality of space flight parts, such as qualification of space flight hardware.
2. RTG4 ES development board is only tested at room temperature.
3. Support for SpaceWire Clock and Data Recovery Circuits
    a. 12 SpaceWire ports are available in the RTG4 ES development board as RTG4 ES device only supports 12 SpaceWire ports. Note that the 2 ports located at SE0_1 and SE1_1 locations have larger trace strength difference between Data and Strobe signals which may result in higher clock skew. Users are recommended to use available SpaceWire ports other than SE0_1 and SE1_1 for better trace length matching.
    b. The SpaceWire package pin assignment will be updated in the next silicon revision for PROTO and flight units. Note that SpaceWire pins are also used as general-purpose global I/O pins. Even if SpaceWire is not used, some of these general-purpose global I/O pins will be updated in the next silicon revision. Refer to the following spreadsheet for pin mapping of the device on the development board, going from the current silicon revision to the next silicon revision:
    SpaceWire Pin Mapping from RTG4 ES/MS Silicon to PROTO/Flight Silicon for RTG4 Development Kit
    c. The RTG4 ES development board uses RevB version of the board, which schematic already references the next silicon revision pin assignment. Users should continue working with the ES package pin assignment and use the above pin mapping spreadsheet to plan for future designs with the next silicon revision of PROTO and flight units.
4. The following features have not been tested and therefore not supported in the ES version of the development board:
    a. Temperature sensing circuit
    b. SPI flash interfaces
    c. RJ45 interface for 10/100/1000 Ethernet
5. The RTG4 ES development kit and the onboard RTG4 ES device are not tested for radiation performance and should not be used for radiation testing.

For more information on RTG4 ES devices, please refer to RTG4 ES Description and RTG4 ES Silicon Errata