Confidently Deploy Microsemi RTG4 FPGAs in Space-based Systems

A Reliability Overview

WP0194

May 2015

Summary

Designers of space systems can deploy RTG4™ Radiation-Tolerant FPGAs in space with confidence because, for the reasons listed below, the RTG4 family surpasses the key requirements for a reliable space-based integrated circuit.

- There is sufficient proven reliability of the 65nm UMC fabrication process.
- Additional design for reliability steps enhance overall device robustness.
- Qualification tests provide ample data that supports reliability confidence.

Introduction

Electronics systems for space-based deployment face a number of issues that terrestrial electronics systems don't need to contend with. Space presents a radiation environment that is hazardous to integrated circuits. (RTG4 radiation effects are covered in a separate paper, see the list of reference documents in the "Additional Resources" section at the end of this paper). Perhaps the next most obvious requirement for space-based systems is the need for the utmost reliability and long lifetime. After all, it is very difficult to make a service call in space. Additionally, a failure in a space deployed electronics system can have a disastrous impact, over and above the failure of a specific feature. An explosive bolt that fires at the wrong time or a mechanical arm that swings uncontrollably can destroy an entire system and put human life, both in space and on the ground, at risk.

It’s no wonder then that electronic devices used in space systems require the most reliable manufacturing processes possible. The most robust space-based devices use an intrinsically reliable fabrication process and manufacturing steps that are well understood. Perhaps most importantly, components used in space electronics systems are extensively tested and screened for many failure mechanisms.

Microsemi RTG4 FPGAs take this approach:

- Leveraging proven reliability of the 65nm NVM UMC fabrication process used for the SmartFusion®2 SoC FPGA and IGLOO®2 FPGA devices.
- Using additional design for the reliability steps to enhance robustness even more.
- Subjecting RTG4 FPGAs to an extensive battery of qualification steps that demonstrate the ability of the devices to withstand the harsh space environment.

This white paper provides the background information needed by RTG4 designers to deploy RTG4 FPGAs in space-based electronics systems with the highest confidence in mission success.

Key Process Requirements for Reliable Space-based Integrated Circuits

Processes used for manufacturing integrated circuits for space-based deployment share many key reliability requirements with processes used for commercial integrated circuit manufacturing. Additionally, processes that feature non-volatile memory (NVM) elements, for both commercial and space-based devices, have additional requirements related to the reliability of the storage capabilities of the NVM cells. The key requirements for any process must take into account the known failure mechanisms for the process and put in place mitigation techniques that reduce failures to the maximum extent possible. A summary of common failure mechanisms that a reliable process must address is listed below.

Electromigration

Electromigration is the process by which material, for example the aluminum or copper used for conductors in integrated circuits, is transported by the momentum transfer from electrons. If sufficient material is transported, conductivity is reduced and circuit failures can result.

Single vias and 90° bends are two examples where current density in a conductor increases, so modern design rules are modified to mitigate the use of these and similar structures.

Hot Carrier Injection

Hot carrier injection is a phenomenon in electronic devices where a charge carrier (an electron or hole) gains sufficient kinetic energy (becomes 'hot') to break through a potential barrier (is injected across the barrier). If a charge carrier becomes trapped in the gate dielectric of a MOS transistor, it can effect the switching characteristics of the transistor, which can lead to a device failure.

Time Dependent Dielectric Breakdown

Time dependent dielectric breakdown (TDDB) is a phenomenon in MOS transistors where the gate oxide (dielectric) breaks down due to an electric field over a long time period. The breakdown occurs when a conductive path is formed from the gate oxide to the substrate, due to the electron tunneling current created by the electric field. This typically happens when devices operate beyond their specified voltage, creating higher than expected electric fields.

Negative Bias Temperature Instability

Negative bias temperature instability (NBTI) can result when a negative bias is applied between the gate and the source for a prolonged period, creating interface 'traps' that hold charge similar to an HCI effect. NBTI thus increases the threshold voltage and this can result in device failures.

Data Retention

Data retention in NVM cells is a measure of the length of time data or the programmed cell state that is properly maintained. The ability of the contents of any particular cell in an array to return the correct data over a period of time is affected by numerous factors including temperature and voltage, electrostatic environment, exposure to radiation, and cumulative erase cycles. Data retention must meet the device specification or failures may occur.

Endurance

Endurance is the measure of the number of program/erase cycles an NVM cell can be exposed to without impacting the ability to correctly store, retain, or read out correct data. Each program/erase cycle has the potential to create defects in the cell structure which can accumulate over time. Cell endurance must meet the device specification or failures may occur.

Microsemi RTG4 FPGA Manufacturing and Screening Process

Microsemi uses robust manufacturing processes and screening flows to produce devices that customers can deploy with confidence in spaced-based systems. Some of these elements are described in the following sections.

Use of MIL-STD-Based Screening Flows

For RTG4 devices screening flows have been developed based on the requirements of MIL-PRF-38535, following the applicable MIL-STD-883 Class B test methods. This enhances the already robust manufacturing and test methodology used for RTG4 products. (Links for these and other similar documents are provided in the "Additional Resources" section at the end of this white paper).

Microsemi Space FPGA Screening Flows Overview

Microsemi RTG4 devices use a robust screening flow to verify that the devices are fit for deployment in space-based applications. Table 1 on page 4 shows the proposed testing and inspection steps for Microsemi's RTG4 FPGA screening flows.

Microsemi SoC offers three screening flows for RT FPGAs:

1. "B-Flow", which implements MIL-STD-883 Class B screening and is compliant with QML Class Q.
2. "E-Flow", which implements additional tests beyond the requirement of MIL-STD-883 Class B.
3. "V / EV Flow", which is a full QML Class V flow (it is called EV Flow prior to official QML Class V qualification).

The steps in red show the additional steps included in each flow, over and above the flows in the columns to the left. Note that the bond pull test has been omitted from these test flows, as RTG4 uses flip-chip assembly technology and has no wire bonds.

Table 1: **RTG4 FPGA Screening Flows**

Proposed RTG4 Screening Process		
Class Q (B Flow)	**Class Q (E Flow)**	**Class V (EV Flow)**
Wafer Sort	Wafer Sort	Wafer Sort
Package Assembly (B flow)	Package Assembly (E flow)	Package Assembly (EV flow)
Internal Visual (Cond. B)	Internal Visual (Cond. A)	Internal Visual (Cond. A)
—	Pre-Cap Source Inpsection (Cond. A)	Pre-Cap Source Inpsection (Cond. A)
Serialization (RT only)	Serialization	Serialization
Temperature Cycling (10 Cycles)	Temperature Cycling (10 cycles)	Temperature Cycling (10 cycles)
Constant Acceleration	Constant Acceleration	Constant Acceleration
PIND (RT only)	PIND	PIND
Seal (Fine/Gross Leak Test)	Seal (Fine/Gross Leak Test)	Seal (Fine/Gross Leak Test)
—	X-Ray	X-Ray
Binning Circuit	Binning Circuit	Binning Circuit
Comm Temp Test	Comm Temp Test	Comp Temp Test
—	Pre-read and Record +25°C (R&R)	Pre-read and Record 25°C (R&R)
Dynamic Burn-in (160 hours at 125°C)	Dynamic Burn-in (240 hours at 125°C)	Dynamic Burn-in (240 hours at 125°C)
Post-BI-Test +25°C	Post-BI-Test +25°C with R&R	Post-BI-Test 25°C with R&R
—	Static Burn-in (144 hours at 125°C)	Static Burn-in (144 hours at 125°C)
—	Post-BI Test +25°C with R&R	Post-BI Test +25°C with R&R
Final Test -55°C	Final Test -55°C	Final Test -55°C with R&R
Final Test +125°C	Final Test +125°C	Final Test +125°C with R&R
—	Seal (Fine/Gross Leak Test)	Seal (Fine/Gross Leak Test)
100% QA Electrical +25°C	100% QA Electrical +25°C	100% QA Electrical +25°C
Visual Inspection	Visual Inspection	Visual Inspection
Lot Acceptance Tests		
Generic Group B	Lot Specific Group B with RGA	Lot Specific Group B with RGA
Generic Group C	Generic Group C	Wafer Lot Specific Group C (2000 hours HTOL)
Generic Group D	Generic Group D	Generic Group D
Generic Radiation Total Dose Report	Generic Radiation Total Dose Report	Generic Radiation Total Dose Report
—	—	Lot Specific DPA (per Date Code)
—	—	Data Package

Additional RTG4 FPGA Reliability Enhancements

In addition to the standard manufacturing process steps followed for RTG4 devices, Microsemi has also included several additional reliability enhancing steps that build on the already robust manufacturing process. Several design for reliability steps have been taken to further enhance reliability.

Conservative Design Rules for Improved Reliability

One of the areas with the most potential impact on reliability is the selection of design rules for the various elements of the integrated circuit fabrication process. By selecting conservative design rules, many of the common device failure mechanisms associated with device failures can be drastically reduced or eliminated. Some of the conservative design rules implemented in the design of RTG4 FPGAs are described below.

Double Vias

Vias are one of the conductor structures most susceptible to electromigration effects due to the reduction in conductor size. This increases current density and thus increases electromigration effects. By using multiple vias in selected high current conduction paths, current density is reduced. This reduces electromigration effects and increases reliability.

Double Contacts

Contacts on device structures can be a source of increased current density and thus can increase electromigration effects. By doubling selected high current contacts, current density is reduced and thus electromigration effects are also reduced, increasing reliability.

Metal Line Width

Small metal lines can reduce the size of circuit interconnect structures, but if line widths become too narrow current density increases. With increased current density, electromigration effects can increase. Conservative sizing of the width of critical conductors will reduce electromigration and improve reliability.

Metal Track Layout

With careful layout of metal track conductors it is possible to avoid common patterns that can cause reliability concerns. Tracks with bends at 90°, for example, increase current density considerably and can cause electromigration effects. By limiting the angle of track bends, current density is reduced and reliability is improved.

Device Dimensions

The sizing of critical devices can impact the overall die size and thus cost. If devices are too small however, process variations can adversely impact device performance and function. By sizing key devices conservatively, the impact of process variations is reduced and reliability is improved.

Well Taps

If well taps are not spaced correctly, latch-up effects may occur and reduce reliability. RTG4 well taps were spaced conservatively to mitigate latch-up effects and improve reliability.

Choice of materials

By selecting appropriate materials for the fabrication of a device, the reliability of the device can be enhanced. For example, Boron10 was not used in the 65nm process for RTG4 FPGAs, SmartFusion2 SoC FPGAs, and IGLOO2 FPGAs. This reduces a source of high energy particles that can cause reliability issues in integrated circuits.

Comprehensive Testing

Rigorous testing is a critical step in checking the overall reliability of a device, and with the use of hardware test structures and built-in self-test (BIST) procedures, much more robust testing and improved test coverage is possible. BIST hardware elements are used in testing multiple blocks within RTG4 FPGAs such as: memory, programmable logic fabric, and fixed function elements. This increases test coverage and thus improves the rigor of RTG4 reliability testing.

Other test structures are also used to improve the results of reliability testing. For example, an on-chip temperature sensor provides measurements of the junction temperature of a device and is used during RTG4 burn-in and high-temperature operating life (HTOL) tests. The increased accuracy of the on-chip temperature sensor improves the rigor of all high-temperature related tests.

Qualification Testing

Extensive qualification tests have been performed on the SmartFusion2 SoC FPGAs and IGLOO2 FPGAs, which use the same 65nm flash process as RTG4. These tests have all passed and provide significant confidence in the fabrication and manufacturing processes that RTG4 devices also use. Some of these qualification tests are listed below:

- HTOL: High-Temperature Operating Life (JESD22-A108; T_J >= +125°C)
- LTOL: Low-Temperature Operating Life (JESD22-A108; T_J <= -50°C)
- ELFR: Early Life Failure Rate (AEC Q100-008, T_J >= +140°C)
- HTSL: High-Temperature Storage Life (JESD22-A103; T_A >= +150°C)
- NVCE: Non-Volatile Memory Cycling Endurance (JESD22-A117)
- HTDR: Data Retention for NVM High-Temperature (JESD22-A117; T_J = +125°C)
- LTDR: Data Retention for NVM Low-Temperature (JESD22-A117; T_A = +25°C)
- HTR: High-Temperature Data Retention (JESD22-A117; T_A = +250°C)
- LU: Latch-Up (Class I and II JESD78)
- ED: Electrical Parameter Assessment (JESD86)
- ED-HBM: Human Body Model Electrical Discharge (JS-001; T_A = +25°C)
- ESD-CDM: Charged Device Model ESD (JESD22-C101; T_A = +25°C)
- PC: Moisture Sensitivity Level Precondition (JESD22-A113)
- HTSL: High-Temperature Storage Lifetime (JESD22-A103; +150°C & Precond)
- HAST: High-Temperature Humidity (JESD22-A110; 110°C, 85%)
- TC: Temperature Cycling (JESD22-A104; -55°C to +125°C)

The above tests have been selected in order to validate the robustness of the 65nm process used by SmartFusion2 SoC FPGAs and IGLOO2 FPGAs, and which is also used for RTG4 FPGAs. In particular, checks for reliability against the known failure mechanisms for space-based devices are shown in Table 2 on page 7 below.

Table 2: **Reliability Checks**

Failure Mechanism	Reliability Tests
Electromigration	HTOL, HTSL
Hot Carrier Injection	HTOL (PMOS), LTOL (NMOS)
Time Dependent Dielectric Breakdown	HTOL
Negative Bias Temperature Instability	HTOL
NVM Data Retention	HTDR, LTDR (SILC), HTSL, HTR
NVM Endurance	NVCE

Conclusion

RTG4 FPGAs can be deployed in space-based systems with confidence because the RTG4 design and manufacturing process surpasses the key requirements for space-based integrated circuits. RTG4 uses fabrication processes with reliability already proven through an extensive series of qualification tests on commercial products. The additional design for reliability steps included in RTG4 FPGAs further enhance their robustness. Finally, the MIL-PRF-38535 qualification tests used for RTG4 devices cover all space-based device reliability concerns and provide ample data so that the RTG4 devices can be deployed in space-based systems with the utmost confidence.

Additional Resources

Microsemi White Papers, Web Pages and Reports

RTG4 Radiation White Paper

Microsemi Rad Tolerant FPGAs Web Page

SmartFusion2 SoC FPGA Web Page

IGLOO2 Web Page

SmartFusion2 and IGLOO2 Interim Radiation Report

Microsemi SoC Reliability Report- Rev 12

Military Standard Specifications

MIL-STD-883 - Test method standard for microcircuits

MIL-PRF-19500 - Semiconductor Devices, General Specification For

MIL-PRF-38534 - Hybrid Microcircuits, General Specification For

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification For

MIL-STD-1835 - Electronic Component Case Outlines

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