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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0
Updated the demo guide for Libero v11.8 software release changes.

1.2 Revision 3.0
Updated the demo guide for Libero v11.7 software release changes.

1.3 Revision 2.0
The following is a summary of the changes in revision 2.0 of this document.
- Updated the demo guide for Libero v11.6 software release changes.
- Updated the labview runtime installer instruction in the Installing the GUI, page 13.

1.4 Revision 1.0
Revision 1.0 was the first publication of this document.
2 Implementing JESD204B Interface Using SmartFusion2

The demo describes the use of SmartFusion®2 System-on-Chip (SoC) field programmable gate array (FPGA) serializer/de-serializer (SerDes) and JESD204B Tx/Rx IP cores for JESD204B data converter interface. This demo uses the CoreJESD204BTx and CoreJESD204BRx IP cores in a loop-back configuration and operates as a standalone demo for JESD204B data converter interface that can be used with the SmartFusion2 Security Evaluation Kit board. A testbench is also provided to simulate the CoreJESD204BTx/Rx cores. Instructions are provided on how to use the corresponding demo as a reference design for JESD204B applications.

This document is intended for FPGA designers, embedded designers, and system-level designers.

The SmartFusion2 SoC and IGLOO®2 FPGA family devices have embedded high-speed SerDes blocks that can handle data rates from 1 Gbps to 5 Gbps. The SerDes module integrates several functional blocks to support multiple high-speed serial protocols within the FPGA. JESD204B is a high-speed serial interface standard for data converters from the JEDEC committee. It reduces the number of data inputs and outputs between the high-speed data converters and receivers. Microsemi has both JESD204B Rx/Tx IP cores compliant with the JESD204B standards. These cores are easy to integrate with JESD204B based data converters for developing high bandwidth applications such as wireless infrastructure transceivers, software defined radios, medical imaging systems, and radar and secure communications.

The SmartFusion2 and IGLOO2 JESD204B Rx/Tx IP cores support link widths of x1, x2, and x4 up to 3.2 Gbps per lane using subclass 0, 1, and 2. This demo guide describes how to use the SmartFusion2 SerDes blocks, JESD204B Rx/Tx IP cores for interfacing subclass0 JES204B based data converters with the data rates up to 2 Gbps. This demo does not use any analog-to-digital converter (ADC) or digital-to-analog converter (DAC) devices, but operates in a loop-back to provide an example of these IP cores in a working design. This demo design works only on SmartFusion2 devices, not on IGLOO2 devices.

- Refer to the JESD204B standard from JEDEC for information on JESD204B interface.
- Refer to the UG0447: IGLOO2 and SmartFusion2 High Speed Serial Interfaces User Guide for more information on SerDes blocks.

2.1 Design Requirements

The following table lists the hardware, software, and IP requirements for this demo design.

<table>
<thead>
<tr>
<th>Requirements</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Hardware</strong></td>
<td></td>
</tr>
<tr>
<td>SmartFusion2 Security Evaluation Kit</td>
<td>Rev D or later</td>
</tr>
<tr>
<td>– 12 V - 2 A wall mounted power supply</td>
<td></td>
</tr>
<tr>
<td>– FlashPro4 JTAG Programmer</td>
<td></td>
</tr>
<tr>
<td>– USB 2.0 A-male to mini-B for UART</td>
<td></td>
</tr>
<tr>
<td>– 2 SMA to SMA cables¹</td>
<td></td>
</tr>
<tr>
<td>Host PC or Laptop</td>
<td>Any Windows 64-bit</td>
</tr>
<tr>
<td><strong>Software</strong></td>
<td></td>
</tr>
<tr>
<td>Libero® System-on-Chip (SoC)</td>
<td>v11.8</td>
</tr>
<tr>
<td>SoftConsole</td>
<td>v3.4 SP1²</td>
</tr>
<tr>
<td>FlashPro Programming Software</td>
<td>v11.8</td>
</tr>
<tr>
<td>Host PC Drivers for FlashPro5</td>
<td>USB to UART drivers</td>
</tr>
</tbody>
</table>
2.2 Demo Design

The demo design files are available for download from the following path in the Microsemi website:
http://soc.microsemi.com/download/rsc/?f=m2s_dg0611_liberov11p8_df

The demo design files include:
- Libero SoC software project
- STAPL programming file
- Graphical User Interface (GUI)
- Sample programming files
- Labview Runtime Installer

For more information, see the readme.txt file.

The following figure shows the top-level structure of the design files.

**Figure 1 • Top-Level Directory Structure**

```
<download_folder>
  m2s_dg0611_liberov11p8_df
    liberodesign
    gui
    stapl_programming_file
    readme
    Labview Runtime Installer
```
2.2.1 Features

The SmartFusion2 JESD204B demo is a standalone reference design developed for interfacing JESD204B compliant data converters with the SmartFusion2 devices. In this demo design, the SerDes lanes are looped back and the data generator pattern is checked by data checker after traversing through both the JESD204B Tx/Rx IP cores. A user friendly GUI is provided to control and monitor the status signals. The following figure shows the JESD204B demo design block diagram implemented in the SmartFusion2 device.

This reference design describes the following:

- Hardware demonstration by externally looping back the SerDes Tx/Rx lanes externally on SmartFusion2 Security Evaluation Kit
- Simulation by looping back the SerDes Tx/Rx lane internally on a test bench to verify the mode of operation

![Hardware Implementation Block Diagram](image-url)

*Figure 2* • Hardware Implementation Block Diagram
2.2.2 Description

2.2.2.1 Hardware Design

The hardware design for the JESD204B demo implementation includes the following:

- Data Generator
- JESD204BTx IP core
- JESD204BRx IP core
- Data Checker
- SERDESIF
- Control Logic
- MMUART for console communications
- Fabric Interface Controller

Figure 2, page 4 shows the block diagram for the design implementation. Refer to the Block Descriptions, page 5 for more information.

2.2.2.2 Block Descriptions

2.2.2.2.1 Data Generator

The data generator has a PRBS generator and waveform generator. The PRBS generator can generate PRBS9, PRBS15, PRBS23, and PRBS31 patterns. An error insertion mode is also implemented in the PRBS generator, which inserts an error into the PRBS sequence for checking. The waveform generator generates sine wave, saw tooth wave, triangle wave, and square wave. The data generator feeds the 16-bit test pattern to CoreJESD204BTx core for transmitting data for SERDESIF.

2.2.2.2.2 Data Checker

The data checker receives 16-bit data output from the CoreJESD204BRx IP core and checks for the correctness of the received data. It generates both an error count and status signal, which is sent to the GUI for status indication. It only checks the PRBS sequences of the data generator.
2.2.2.2.3 **Core JESD204B Tx**

The CoreJESD204BTx is compatible with the JEDEC JESD204B standard. For this demo design, the IP core is configured, as shown in the following figure.

**Figure 3 • Core JESD204B Tx Configuration**

Refer to the *IP Core Configuration Guide* for more information on settings.
2.2.2.4 Core JESD204B Rx

The Core JESD204B Rx is compatible with the JEDEC JESD204B standard. The IP core is configured, as shown in the following figure.

*Figure 4 • Core JESD204B Rx Configuration*

Refer to the [IP Core Configuration Guide](#) for more information on settings.
2.2.2.2.5 SERDESIF

The SmartFusion2 SoC FPGA high-speed SerDes is a hard IP block on chip that supports the high-speed data rates up to 5 Gbps. The SERDESIF EPCS mode is used for JESD204B providing a data path directly to the PMA.

Refer to UG0447: IGLOO2 and SmartFusion2 High Speed Serial Interfaces User Guide for more information on the SerDes block.

In this demo, the SERDESIF2 block is configured in EPCS mode on lane 2 to interface JESD204B IP cores, with reference clock 100 MHz from fabric to support 2 Gbps data rate. The following figure shows the SerDes block configuration details.

Figure 5 • SERDESIF2 Configuration

Note: The M2S090/M2GL090 and M2S060/M2GL060 devices use the SERDESIF2 module. All the other SmartFusion2 and IGLOO2 devices use the SERDESIF module.

2.2.2.2.6 MSS Block

The microcontroller subsystem (MSS) block sends and receives the data between host PC (GUI interface) and fabric logic. The MMUART interface is used to communicate with the host PC. The FIC_0 interface (APB master) is used to communicate with the fabric user logic.

2.2.2.2.7 TPSRAM IP

TPSRAM IP is an LSRAM module and is used for loading status and data signal, and is configured as follows:

• Status data Buffer (Depth: 1024, Width: 32)
• Output data Buffer (Depth: 1024, Width: 32)
2.2.2.8 Control Logic
The control logic implemented in the fabric consists of an APB slave FSM to communicate with a MSS APB master, and also controls operations such as reading and writing status and output data buffers.

2.3 Simulating the Design
The design is simulated using the provided testbench. The testbench simulates the JESD204B demo design for PRBS pattern and waveform selection.

To run the simulation,

- Double-click Simulate under Verify Pre-Synthesized Design in the Design Flow tab of the Libero project, as shown in the following figure.
- Or right-click and select Simulate to invoke the simulator.

Figure 6 • Simulating the Design

The testbench generates the test selection for the PRBS input (PRBS7, PRBS15, PRBS23, and PRBS31) and sine wave for waveform input. It also monitors the JESD204B output status signals (SYNC_N, ALIGNED, and CGS_ERR) for the verification of JESD204B phases, and PRBS checker output status signals for the correctness of the Input PRBS pattern (PRBS7, PRBS15, PRBS23, and PRBS31).
The simulation ends after executing all the test cases. The status of the test cases is shown in the Modelsim Transcript window, as shown in the following figure.

Figure 7 • Transcript Window
After simulation, the **Simulation Waveform** window is displayed, as shown in the following figure.

*Figure 8* • Simulation Waveform Window
2.4 Setting Up the Demo Design

The following steps describe how to set up the demo design:

1. Connect the FlashPro4 programmer to the FlashPro header on the SmartFusion2 Security Evaluation Kit, as shown in the following figure.
2. Connect the J18 connector and host PC using the mini-B cable.
3. Ensure that the USB to UART bridge drivers are automatically detected (can be verified in the Device Manager).
4. Loop-back the SerDes Lane 2 (TxD2P <-> RxD2P, TxD2N <-> RxD2N) using two SMA-SMA cables, as shown in the following figure.
5. Connect the 12 V power adapter that shipped with the FPGA development board to the power jack J6, and switch on the power supply.

Figure 9 • Hardware Setup

Note: SerDes Lane 1 is looped back from transmit to receive data on the board. If the SMA cables are not available, the user can reconfigure the SERDESIF2 to Lane 1.

2.5 Programming the Device

The following steps describe how to program the device:

1. Download the design files from http://soc.microsemi.com/download/rsc/?f=m2s_dg0611_liberov11p8_df
   The Programming file (STAPL/PDB) is located in the Programming_File folder.
2. Connect the FlashPro4 programmer to the SmartFusion2 Security Evaluation Kit.
3. Connect the jumpers to the SmartFusion2 Security Evaluation Kit board as listed in the following table.

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Pin From</th>
<th>Pin To</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>J3</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J8</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
</tbody>
</table>
CAUTION: Ensure that the power supply switch SW7 is switched OFF while connecting the jumpers to the SmartFusion2 FPGA Security Evaluation Kit.

4. Program the SmartFusion2 device with the downloaded programming file as in step 1 using FlashPro v11.8.

2.6 Installing the GUI

The JESD204B demo is provided with a user friendly GUI that runs on the host PC to communicate using an UART with the SmartFusion2 Security Evaluation Kit.

The following steps describe how to run the installer if the GUI is used for the first time:

1. Download the design files from http://soc.microsemi.com/download/rsc/?f=m2s_dg0611_iberov11p8_df
2. Open and run Labview Runtime Installer > setup.exe before installing JESD204B GUI. Restart host PC if necessary.
3. Open GUI_Installer > Volume > setup.exe.
4. Click Yes for any message from User Account Control. The Destination Directory window is displayed with the default locations, as shown in the following figure.
5. Click Next.

Figure 10 • GUI Set Up Window
6. Follow the instructions in the GUI to start the installation. A progress bar appears, which shows the progress of installation as shown in the following figure.

Figure 11 • GUI Set Up Progress Bar

7. Wait for the installation to complete. After successful installation, the Installation Complete message is displayed.

8. Click Finish.

9. Restart the host PC before using the installed GUI.

2.7 Running the Demo Design

This section describes how to use the GUI for selecting the test patterns and monitoring the loop-back data for the demo design. It provides an interactive GUI for selection of different PRBS test patterns as a demo input, and observes the JESD204B status signals and PRBS status collected from the board. It also shows the output waveform samples collected from the board during waveform selection on the waveform tab.
The following steps describe how to run the demo design:

1. Open **Programs > SF2_JESD204B Demo**.  
The following figure shows the GUI window.

*Figure 12 • SmartFusion2 JESD204B Demo GUI Window*  
![SmartFusion2 JESD204B Demo GUI Window](image)

The drop-down list for ports has the list of serial ports available on the host PC. The working ports are enabled and the unavailable ports are grayed out.

**Note:** The default settings for the design are 115200 baud, no flow control, one stop, and no parity.

2. Select the COM port number that is detected to configure the serial port.
3. Click **Connect** to connect the host PC to the hardware through the selected port, as shown in the following figure.

**Note:** Port numbers may vary. Select the correct port number from the list.

*Figure 13 • Serial Port Configuration*
4. Select the pattern to be transmitted using the **Input selection**. Select one of the patterns in PRBS selection, Select **PRBS 7** as shown in the following figure.

*Figure 14 • PRBS Pattern Selection*

5. Click **START** to start the JESD204B demo. The selected pattern is sent over serial transmit link. The looped back data is received by the receiver and checked for any errors. The status can be monitored using the status signals in the GUI at any time.

**Note:** Select any six signal check boxes on the right side panel to view the status of the signals. If the count is more than six, de-select the selected signals before selecting any new signals.
6. Click **Generate Data Error** and observe error status using GUI. The following figure shows the Host Connection, Link Status, PRBS Status, and Error Count.

*Figure 15 • Data Error Generation*

7. Click **Clear Error** to stop generating the error data **PRBS Status** turns green, and **Error Count** is displayed as 0.
8. Click **Generate Link Error** to generate error in 20 bits SerDes lane. The following figure shows the **Link Status** changed to RED on link error.

**Figure 16 • Data Error Generation**

![Data Error Generation Diagram]

**Note:** Select any six signal check boxes on the right side panel to view the status of the signals. De-select the selected signals before selecting any new signals if the count is more than six. The SYNCH, ALIGNED, CGS_ERR, NIT_ERR, DISP_ERR, and EPCS_RX_VALID signals are enabled during Link Status failure.

9. Click **Clear Error** to stop generating the error data and observe the **Link Status** turn to green.
10. Select **Triangle** as Input selection to change the pattern and view the status link, as shown in the following figure.

*Figure 17 • Waveform Pattern Selection*

The selected pattern is sent over the serial transmit link. It is then received by the receiver. The status can be monitored using **Status Signals** in the GUI.
11. Click the **Waveform** tab to view the **Triangle** waveform received from the JESD204BRx IP core, as shown in the following figure.

**Figure 18 • Waveform Tab**

![Waveform Tab Image](image)

12. Click **Stop**.