ER0196
Errata
SmartFusion2 Device v1.5

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.5

Updated text for item Concurrent access of Cortex-M3 I- and D-busses is not allowed, page 7.

1.2 Revision 1.4

Updated text for item The I/Os state during programming is changed from Z to weak pull-up, page 10.

1.3 Revision 1.3

Added Errata items For S (security) grade devices, user must not enable write protection for Protected 4 K Regions, also known as Special Sectors in the eNVM, page 10 and Users must not set page lock in eNVM0 for the 060 device and eNVM1 for 090/150 devices, page 10.

1.4 Revision 1.2

The following items are added in revision 1.2 of this document:

- Updated Table 2, page 2 to include the M2S010 device in revision 3.
- Added errata items Disable Cortex-M3 when programming eNVM only, page 10 and The I/Os state during programming is changed from Z to weak pull-up, page 10.
- Updated Table 6, page 12 to include the M2S010 (T, TS) device.
- Added solution for item Programming of the eNVM blocks needs to occur independent of the fabric, page 8.

1.5 Revision 1.1

Updated M2S060 Revision from ES to Rev 0.

1.6 Revision 1.0

The following items are added in revision 1.0 of this document:

- Combined M2S005, M2S010, M2S025, M2S060, M2S090 and M2S150 devices and die revisions to one centralized document.
- Created a separate Errata for the M2S050 device.

Table 1 • **Revisions Released per Device**

Silicon Devices	Revisions	Device Status
M2S005 (S)	Commercial/Industrial	Production
M2S010 (S,T,TS)	Commercial/Industrial	Production
M2S025 (T,TS)	Commercial/Industrial	Production
M2S060 (T,TS)	Commercial/Industrial	Production
M2S090 (T,TS)	Commercial/Industrial	Production
M2S150 (T,TS)	Commercial/Industrial	Production

2 Errata for SmartFusion2 Devices

Table 2 lists the specific device Errata and the affected SmartFusion2 devices. Refer to the Marking Specification Details in the *SmartFusion2 SoC FPGAs Data Security Devices Product Brief* for this Die revision part marking specification.

Table 2 • **Summary of SmartFusion2 Devices, Errata**

Errata No.	Errata	Silicon Revisions													Software Errata
		M2S005		M2S010			M2S025		M2S060	M2S090			M2S150		
		0	1, 2	0	1, 2	3	0	1, 2	0	0	1, 2	3	0	1, 2	
3.1	VPP must be set to 2.5 V when programming and writing the eNVM at Industrial temperatures range, page 5	X		X			X								
3.2	Over-voltage support on MSIOs during Flash*Freeze mode, page 5	X		X			X								
3.3	Verification of the FPGA fabric at junction temperatures higher than 50°C erroneously indicates a failure, page 5	X		X			X								
3.4	DDR_OUT and I/O-Reg functional Errata due to a software bug, page 5														X
3.5	Dedicated differential I/O driving the reference clock of the CCC may cause a functional failure due to a software bug, page 6														X
3.6	Power up digest is not supported, page 6	X		X			X			X			X		
3.7	Programming of the eNVM should only occur as part of a bitstream also containing the FPGA fabric, page 6														X

Table 2 • **Summary of SmartFusion2 Devices, Errata *(continued)***

Errata No.	Errata	Silicon Revisions													Software Errata
		M2S005		M2S010			M2S025		M2S060	M2S090			M2S150		
		0	1, 2	0	1, 2	3	0	1, 2	0	0	1, 2	3	0	1, 2	
3.8	Updating eNVM from the MSS or the FPGA fabric requires changes of the FREQRNG register, page 6	X	X	X	X	X	X	X	X	X	X	X	X	X	
3.9	SYSCTRL_RESET_STATUS macro is not supported, page 6	X		X			X			X			X		
3.10	Zeroization is not supported, page 6	X		X			X			X	X		X		
3.11	Concurrent access of Cortex-M3 I- and D-busses is not allowed, page 7														X
3.12	The System controller RC oscillator runs at 25 MHz after a programming recovery operation, page 7			NS	X					NS	X				
3.13	ECC Point-Multiplication Service and ECC Point-Addition System Service are not supported, page 7									X			X		
3.14	Programming Silicon requires Cortex-M3 firmware code, page 8									X			X		
3.15	Programming of the FPGA fabric can occur only at room temperature, page 8									X			X		
3.16	Programming of the eNVM blocks needs to occur independent of the fabric, page 8									X			X		
3.17	PCIe Hot Reset support requires a soft reset solution, page 8			X	X	X	X	X	X	X	X	X	X	X	

Table 2 • **Summary of SmartFusion2 Devices, Errata *(continued)***

Errata No.	Errata	Silicon Revisions													Software Errata
		M2S005		M2S010			M2S025		M2S060	M2S090			M2S150		
		0	1, 2	0	1, 2	3	0	1, 2	0	0	1, 2	3	0	1, 2	
3.18	Executing SRAM-PUF services fails while the Cortex-M3 code is executed from eNVM_1, page 9									X	X	X	X	X	
3.19	After successful completion of 2-step IAP or CM3 ISP (without a SYSRESET), LSRAM Read and Write access fails from the fabric path, page 9	X	X	X	X	X	X	X	X	X	X	X	X	X	
3.20	SRAM-PUF system services may take two to three seconds to complete, page 9									X	X	X	X	X	
3.21	Disable Cortex-M3 when programming eNVM only, page 10	X	X	X	X	X	X	X	X	X	X	X	X	X	
3.22	The I/Os state during programming is changed from Z to weak pull-up, page 10	X		X			X						X		
3.23	For S (security) grade devices, user must not enable write protection for Protected 4 K Regions, also known as Special Sectors in the eNVM, page 10	X	X	X	X	X	X	X	X	X	X	X	X	X	
3.24	Users must not set page lock in eNVM0 for the 060 device and eNVM1 for 090/150 devices, page 10								X	X	X	X	X	X	

Note: In the preceding table:

- An “X” means that the Errata exists for that particular device and revision number.
- A blank box means that the Errata does not exist or the feature does not exist for that particular device and revision number.
- NS (Not Supported) means the Programming Recovery Mode is not available in this revision.
- Software Errata can be avoided by using Libero SoC v11.4 SPI or newer.

Contact *Microsemi SoC Technical Support* if you have additional questions. To order a specific die, contact your local Microsemi sales office.

3 Errata Descriptions and Solutions

3.1 VPP must be set to 2.5 V when programming and writing the eNVM at Industrial temperatures range

VPP can be set to 2.5 V or 3.3 V. However, when writing or programming the eNVM of Revision 0 of the M2S005, M2S010, and M2S025 devices below 0°C, VPP must be set to 2.5 V. Refer to the *DS0128: IGLOO2 and SmartFusion2 Datasheet* for VPP minimum and maximum settings. Note that the eNVM reading with VPP set to 3.3 V or 2.5 V operates as intended.

3.2 Over-voltage support on MSIOs during Flash*Freeze mode

When the input voltage is driven above the reference voltage for that bank, additional current can be consumed in Flash*Freeze mode for Revision 0 of the following devices: M2S005, M2S010, and M2S025.

3.3 Verification of the FPGA fabric at junction temperatures higher than 50°C erroneously indicates a failure

In Revision 0 of the following devices: M2S005, M2S010, and M2S025, standalone verification (STAPL VERIFY action) should be run at temperatures lower than 50°C. If a VERIFY action is run at temperatures higher than 50°C, a false verify failure may be reported. Note that the Check Digest system services can be used to confirm design integrity at temperatures within the recommended operation conditions.

3.4 DDR_OUT and I/O-Reg functional Errata due to a software bug

This Errata only applies if you created or updated your design using Libero® SoC v11.1 SP1 or v11.1 SP2. If you have one of the following in your design, the corresponding I/O will not function properly in the silicon due to the wrong software implementation of the I/O macro.

- If you use DDR_OUT macro in your design.
- If you combine an output or output enable register with an I/O using the PDC command set_io <portName> -register yes

Solution:

Both Errata are fixed in Libero SoC v11.1 SP3. Migrate your design to Libero SoC v11.1 SP3 or newer version, and re-run Compile and Layout.

3.5 Dedicated differential I/O driving the reference clock of the CCC may cause a functional failure due to a software bug

If your design has the dedicated differential I/O pair driving the reference clock of the CCC, the input clock may not propagate to CCC due to a software bug and the device will fail during silicon testing. There are several options to drive the ref clock of the CCC. One of the options is to drive from “Dedicated Input PAD x” (x = 0 to 3); this uses hardwired routing. In this option, choose single-ended I/O or differential I/O as the ref clock. This Errata exists when you choose the differential I/O option, meaning the dedicated differential I/O is used as CCC reference clock input.

This Errata can’t be detected in any functional simulation, and can only be detected in silicon testing.

Solution:

The Errata is fixed in the Libero SoC 11.1 SP3. Migrate your design to the Libero SoC 11.1 SP3 or newer version, and re-run Compile and Layout.

3.6 Power up digest is not supported

Power up digest is not supported in Revision 0 of the M2S005, M2S010, M2S025, M2S090, and M2S150 devices.

Workaround:

Use NVM Data Integrity Check System service after the device is on and check the data integrity.

3.7 Programming of the eNVM should only occur as part of a bitstream also containing the FPGA fabric

The Bitstream Configuration Dialog Box in the Libero SoC allows for programming eNVM and the FPGA fabric separately. However, if using Libero v11.1 SP2 or an older version, program the eNVM along with the FPGA fabric for the M2S005, M2S010, M2S025, and M2S050 devices. The fabric can be programmed separately, if needed.

Solution:

The Errata is fixed in the Libero SoC 11.1 SP3. Migrate your design to the Libero SoC 11.1 SP3 or newer version, and re-run Compile and Layout.

3.8 Updating eNVM from the MSS or the FPGA fabric requires changes of the FREQRNG register

When updating the eNVM from the FPGA fabric, the NV_FREQRNG register must be changed from the default value 0x07 to 0x0F; eNVM reads are not affected. SmartFusion2 eNVM firmware driver v2.2 has been updated with the correct NV_FREQRNG settings.

3.9 SYSCTRL_RESET_STATUS macro is not supported

3.10 Zeroization is not supported

3.11 Concurrent access of Cortex-M3 I- and D-busses is not allowed

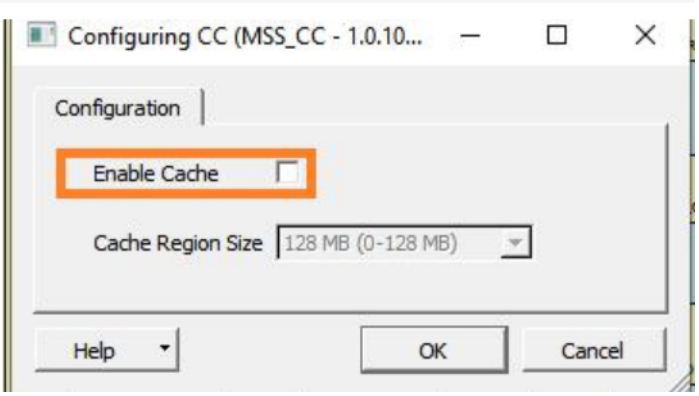
A concurrent access of the Cortex®-M3 I-Bus and D-Bus may result in an invalid value returned to the internal registers from the cache; when both accesses are sourced by the cache.

The following are the possible four workarounds:

Workarounds:

- **Workaround 1:** IAR toolchain users can fix this problem by preventing the Cortex-M3 processor from issuing concurrent I and D buses access through the cache by locating the constants and data variables outside the memory regions accessed by the cache to prevent conflicts in the linker scripts. The compiler also requires adding the `-no_literal_pool` option to prevent the compiler/assembler from locating variables close to instructions known as literal pools. For more information, refer to section 4.2.3.3.1 from *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*.
- **Workaround 2:** Cache can be turned off by disabling the **Enable Cache** check box in the **Cache Configurator** of the SmartFusion2 MSS Subsystem, as follows.

Figure 1 • **Disabling Cache in Cache Configurator**



- **Workaround 3:** Insert NOPs and recompile to remove the condition that causes concurrent access issues of Cortex-M3 I and D buses.
- **Workaround 4:** The application needs to be executed from eSRAM (that is, 0x20000000) instead of eNVM (that is, 0x0000000) by changing the linker script.

3.12 The System controller RC oscillator runs at 25 MHz after a programming recovery operation

After a programming recovery event the system controller will be operating at 25 MHz, normally the System controller should operate at 50 MHz after a programming recovery event.

Workaround:

If operating the system controller at 50 MHz is important to your design contact soc_tech@microsemi.com.

3.13 ECC Point-Multiplication Service and ECC Point-Addition System Service are not supported

3.14 Programming Silicon requires Cortex-M3 firmware code

For the Revision 0 of the M2S090 and M2S150 devices, the eNVM needs to contain valid Cortex-M3 code. By default, SmartFusion2 parts are shipped with a default boot-up program stored at the eNVM address 0x60000000. If this default program is no longer valid or overwritten by the user, and there is no valid user boot code, the Cortex-M3 won't execute to a valid state. This leads to unexpected behavior including the programming lockout condition in Revision 0 of the M2S090 and M2S150 devices.

Workaround:

The firmware code must be programmed into the eNVM prior to re-programming a commercial device. A "while(1)" statement will work. Refer to Knowledge Base (KB) *SmartFusion2: Managing Cortex-M3, while accessing MSS from fabric, when there is no default or valid boot code for Cortex-M3 to execute* for details.

3.15 Programming of the FPGA fabric can occur only at room temperature

3.16 Programming of the eNVM blocks needs to occur independent of the fabric

Customer using Revision 0 of M2S090 or M2S150 devices must Program the eNVM block independently in Libero v11.6 or older. Contact Microsemi SoC Technical Support, if you want to Program the eNVM block independently in Revision 0 of M2S090 and M2S150 devices using Libero v11.7.

3.17 PCIe Hot Reset support requires a soft reset solution

On SmartFusion2 devices, a PCIe® Hot Reset requires a soft FPGA logic reset scheme which clears the sticky bits of the PCI configuration space.

Workaround:

On SmartFusion2 devices, a PCIe Hot Reset requires a soft FPGA logic reset scheme which clears the sticky bits of the PCI configuration space.

The application note *AN437 – Implementing PCIe Reset Sequence in SmartFusion2 and IGLOO2 Devices* describes the PCIe Hot Reset reset scheme. However, this reset scheme causes PCIe violations in some cases.

- For the M2S060/090T(S) devices there are no violations.
- For the M2S010/025/150T(S) devices at Gen1 rates there are no violations.
- For the M2S/025/150T(S) devices at Gen2 rates there are two PCIe CV violations.
  - Test case 1: TD_1_7 (Advanced Error Reporting Capability)
  - Test case 2: TD_1_41 (LinkCap2Control2Status2 Reg).

3.18 Executing SRAM-PUF services fails while the Cortex-M3 code is executed from eNVM_1

In the SmartFusion2 M2S090/M2S150 devices, the System Controller does not release the eNVM1 access after execution of the following SRAM-PUF system services:

- Create User AC (Activation Code) service
- Delete User AC service
- Create User KC for an Intrinsic Key service
- Create User KC for an Extrinsic Key service
- Delete User KC service

The above system services get executed successfully but the eNVM1 becomes inaccessible to Cortex-M3 and also to fabric master.

- Any subsequent access to eNVM1 after this point, where eNVM1 is locked by System Controller, will result in a stall, and a Power on Reset (POR) is required to remove the stall.

Workaround:

Execute “Get Number of the Key Code (GET_NUMBER_OF_KC)” SRAM-PUF system services immediately after the above services.

- The additional GET_NUMBER_OF_KC services releases the eNVM1 access from the System Controller.
- The firmware code for running SRAM-PUF services workaround must be executed from eNVM0, eSRAM or DDR memories only, as Cortex-M3 does not get access to the eNVM1 that time.

3.19 After successful completion of 2-step IAP or CM3 ISP (without a SYSRESET), LSRAM Read and Write access fails from the fabric path

If LSRAM Read and Write access fails from the fabric path after performing 2-step IAP or CM3 ISP, perform a system reset or F*F Entry/Exit.

Workaround:

The user application must execute System Reset as soon as the IAP/ISP system service is completed. Otherwise user write and read accesses to LSRAM/uRAM will not be possible. The System Reset can be generated with the use of the tamper macro (availably in the Libero SoC Catalog). Immediately after the IAP/ISP service, the user logic checks the LSRAM/uRAM access. If access is denied, the user logic sends the reset request/interrupt to the system controller through the tamper macro (by enabling the RESET function in the tamper macro configuration window) and then the system controller executes the system level reset.

For more information, refer to the *UG0451: IGLOO2 and SmartFusion2 Programming User Guide*.

The following application notes have more information and design examples on how to implement the workaround:

- *SmartFusion2 SoC FPGA - In-System Programming Using USB OTG Controller Interface - Libero SoC v11.5 Demo Guide*
- *SmartFusion2 SoC FPGA - In-System Programming Using UART Interface Demo - Libero SoC v11.5 Demo Guide*
- *SmartFusion2 SoC FPGA In-Application Programming Using PCIe Interface - Libero SoC v11.5 Demo Guide*

3.20 SRAM-PUF system services may take two to three seconds to complete

This Errata is fixed in the newer date code devices, where SRAM-PUF system services will run faster. Contact at *soc_tech@microsemi.com* for more information.

3.21 Disable Cortex-M3 when programming eNVM only

The user uses the Bitstream Configuration dialog box in the Libero SoC tool and generates an eNVM only stapl file. During programming, the system controller takes control of the eNVM block. If the user design has the application code running from the eNVM block, the Cortex-M3 processor halts as it cannot access the eNVM block. When the eNVM block programming is completed, the system controller releases the eNVM. The Cortex-M3 continues running from the same address from where it was halted at, unless the device is re-started. If the device in not re-started, the Cortex-M3 behavior will be unpredictable as the eNVM is updated with the new code.

Workaround

- Use the M3_Reset_N signal to hold the Cortex-M3 processor in reset before programming the eNVM block.
- Force a device to re-start.
- Program eNVM and fabric.

Libero v11.7 will fix the unpredictable behavior issue by forcing a re-start of the device after eNVM programming.

3.22 The I/Os state during programming is changed from Z to weak pull-up

The state of the I/O during programming is changed from Z to weak pull-up in the latest die revisions. Affected die revisions (marked with “X” in Table 2, page 2) have I/Os that are tristated during programming.

3.23 For S (security) grade devices, user must not enable write protection for Protected 4 K Regions, also known as Special Sectors in the eNVM

For S (security) devices, there are two or four 4 KB regions per eNVM array that can be protected for read and write, these regions are known as Protected 4 K Regions or Special Sectors. If write protection is enabled for any of these regions, none of the locked pages inside the same eNVM block can be unlocked.

3.24 Users must not set page lock in eNVM0 for the 060 device and eNVM1 for 090/150 devices

For 060, 090, and 150 device densities: Each eNVM memory block has a user page lock bit (refer to PAGE_LOCK_SET register) to lock a page and prevent accidental writing. After the page lock is set in eNVM0 for the 060 device or eNVM1 for 090/150 devices, the user will not be able to clear the lock for subsequent page updates later.

Workaround:

To use page lock feature, the user can use eNVM0 of 090/150 device and set/clear page lock using the master (for example, M3 or fabric). There is no workaround for the 060 device. User must contact SoC tech support if they already used page lock in the 060 device, which they need to unlock now.

4 Usage Guidelines for SmartFusion2 Devices

4.1 Programming support

Note that there may be package dependencies that may not expose certain programming interfaces. Refer to the *PB0115: SmartFusion2 System-on-Chip FPGAs Product Brief* for device/package specific features.

Table 3 • **Revision 0 Devices**

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery	M3 ISP
Programming Interface	JTAG	SPI_SC	SPI_0	SPI_0	SPI_0	SPI_0	N/A
M2S005(S)	Yes	Yes	No	No	No	No	Yes
M2S010 (S,T,TS)	Yes	Yes	No	No	No	No	Yes
M2S025 (T,TS)	Yes	Yes	No	No	No	No	Yes
M2S060 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
M2S090 (T,TS)	Yes	Yes	No	No	No	Yes*	Yes
M2S150 (T,TS)	Yes	Yes	No	No	No	No	Yes

Note: *Refer to Errata item The System controller RC oscillator runs at 25 MHz after a programming recovery operation, page 7.

Table 4 • **Revision 1 Devices**

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery	M3 ISP
Programming Interface	JTAG	SC_SPI	SPI_0	SPI_0	SPI_0	SPI_0	N/A
M2S005 (S)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
M2S010 (S,T,TS)	Yes	Yes	Yes	Yes	Yes	Yes*	Yes
M2S025 (T,TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
M2S090 (T,TS)	Yes	Yes	Yes	Yes	Yes	Yes*	Yes
M2S0150 (T,TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Note: *Refer to Errata item The System controller RC oscillator runs at 25 MHz after a programming recovery operation, page 7.

Table 5 • **Revision 2 Devices**

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery	M3 ISP
Programming Interface	JTAG	SC_SPI	SPI_0	SPI_0	SPI_0	SPI_0	N/A
M2S005 (S)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
M2S010 (S,T,TS)	Yes	Yes	Yes	Yes	Yes	Yes*	Yes
M2S025 (T,TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
M2S090 (T,TS)	Yes	Yes	Yes	Yes	Yes	Yes*	Yes
M2S150 (T,TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Note: *Refer to Errata item The System controller RC oscillator runs at 25 MHz after a programming recovery operation, page 7.

Table 6 • **Revision 3 Devices**

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery	M3 ISP
Programming Interface	JTAG	SC_SPI	SPI_0	SPI_0	SPI_0	SPI_0	N/A
M2S010 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
M2S090 (T,TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes

4.2 SHA-256 System Service

Microsemi recommends the message required to be on byte boundary when using SHA-256 System Service for the SmartFusion2 devices.

4.3 MSS reset mode

To keep the MSS in reset during normal operation, it is necessary to wait for the device to power up, and then apply the reset. The US_POR_B signal from the MSS (the power-on-reset for the FPGA fabric) can be used to check the device's powered up state.

4.4 Accessing the PCIe Bridge register in the high speed serial interface

The PCIe Bridge registers should not be accessed before the PHY is ready. Wait for the PHY_READY signal (which indicates when PHY is ready) to be asserted before updating the PCIe Bridge registers.

The PHY_READY signal is normally asserted within 200 µs after the device is powered up, so wait for 200 µs before accessing the PCIe Bridge registers.

5 Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

5.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**

From the rest of the world, call **650.318.4460**

Fax, from anywhere in the world **650.318.8044**

5.2 Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known Erratas and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

5.3 Technical Support

For Microsemi SoC Products Support, visit *http://www.microsemi.com/products/fpga-soc/designsupport/fpga-soc-support*.

5.4 Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group *home page, at http://www.microsemi.com/products/fpga-soc/fpga-and-soc*.

5.5 Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

5.5.1 Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.The technical support email address is *soc_tech@microsemi.com*.

5.5.2 My Cases

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5.5.3 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (*soc_tech@microsemi.com*) or contact a local sales office. Visit *About Us* for *sales office listings* and *corporate contacts*.

5.6 ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via *soc_tech@microsemi.com*. Alternatively, within My Cases, select Yes in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR webpage.