ER0193
Errata
RTG4 FPGA

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 1.5

The following are the changes made in revision 1.5 of this document:

- Added link to Product Notifications web-page to access latest RTG4 notices. See Introduction, page 2.
- Information about Production Silicon was updated. See Table 1, page 2.
- Summary of RTG4 FPGA Errata was added. See Table 2, page 2.
- New errata items 16 to 23 were added. See Errata Descriptions and Solutions, page 5.

1.2 Revision 1.4

The following are the changes made in revision 1.4 of this document:

- Added a new errata item. For more information, see 214 (MSIO341NB4) and 215 (MSIO341PB4) pins must be tied to V_{DD} 1.2 V in RTG4 CQ352 package engineering samples such as ES and MS, page 7.
- Added a new errata item. For more information, see Single Asynchronous reset in the ES/MS device, page 8.

1.3 Revision 1.3

The following are the changes implemented in revision 1.3 of this document:

- The x36 and x18 configurations are added to the errata item 12, For dual-port RAM (LSRAM), read data does not match with written data in Feed-through x36, x18, x12 or x9 configurations, page 7 in revision 1.3 of this document.
- Errata 13 During boundary scan or programming, a higher than expected current can be observed on the SERDES_x_Lyz_VDDAIO, page 7 is added.

1.4 Revision 1.2

RTG4 PROTO device is added in revision 1.2 of this document.

1.5 Revision 1.1

The following are the changes implemented in revision 1.1 of this document:

- Errata 11, I/Os states during programming mode do not match with “I/O State During Programming” user settings, page 6 and errata 12, For dual-port RAM (LSRAM), read data does not match with written data in Feed-through x36, x18, x12 or x9 configurations, page 7 are added
- Removed the errata item, Package pins are not up-to-date in the Libero SoC RTG4 launch software for the RT4G150-CG1657 device as it is not silicon issue, It is a software issue and got fixed in the latest Libero software
- Updated the document to cover ES and MS silicon

1.6 Revision 1.0

Revision 1.0 was the first publication of this document.

2 RTG4 FPGA Errata

2.1 Introduction

This errata sheet contains information about device issues specific to RTG4™ FPGAs including, RT4G150 Engineering Samples (ES/MS), PROTO devices and Production devices. Each Errata description provides a workaround or solution, when available. See the product notifications website for a complete list of Customer Advisory Notices (CANs), Customer Notifications (CNs), and Product Change Notifications (PCNs) applicable to RTG4.

2.2 Revisions Released per Device

The following table describes the revisions released per silicon device and the device status.

Table 1 • **Revisions Released per Device[1, 2]**

Silicon Devices	Revisions	Device Status
RT4G150	ES/MS	Sold Out/Discontinued
RT4G150	PROTO/Production CG1657	Production
RT4G150	PROTO/Production CQ352	Advanced

1. See *PB0051: RTG4 FPGAs Product Brief* for information about identifying device revision from the package markings.
2. PROTO and Production devices use the same silicon revision (Rev C).

2.3 Summary of RTG4 FPGA Errata

The following table gives the summary of RTG4 Errata items:

Table 2 • **Summary of RTG4 FPGA Errata**

		Silicon Revision	
No.	**Description**	**ES/MS**	**PROTO/ Production**
1.	SPI-Slave programming interface not supported, page 5	✓	✓
2.	VPP ramp time must be greater than 5 ms to ensure device functionality and performance upon power up, page 5	✓	X
3.	12 of the 16 SpaceWire pins are available, page 5	✓	X
4.	SpaceWire RX recovered clock has high jitter, page 5	✓	X
5.	The maximum I/O frequency is lower than the RTG4 Datasheet specification by 10% , page 5	✓	X
6.	I/O drive strength (IOL/IOH) is lower than the Datasheet specification by 30%, page 5	✓	X
7.	Fabric PLL output frequency could be lower than expected, page 6	✓	X
8.	SmartDebug Probe Write is not supported for ES/MS devices, page 6	✓	X
9.	SmartDebug Live Probe feature is not supported when SYSRESET macro is used in the design, page 6	✓	X
10.	PCIe x1 lane configuration is supported, page 6	✓	X

Table 2 • **Summary of RTG4 FPGA Errata *(continued)***

No.	Description	Silicon Revision	
		ES/MS	PROTO/ Production
11.	I/Os states during programming mode do not match with “I/O State During Programming” user settings, page 6	✓	X
12.	For dual-port RAM (LSRAM), read data does not match with written data in Feed-through x36, x18, x12 or x9 configurations, page 7	✓	✓
13.	During boundary scan or programming, a higher than expected current can be observed on the SERDES_x_Lyz_VDDAIO, page 7	✓	X
14.	214 (MSIO341NB4) and 215 (MSIO341PB4) pins must be tied to V_{DD} 1.2 V in RTG4 CQ352 package engineering samples such as ES and MS, page 7	✓	X
15.	Single Asynchronous reset in the ES/MS device, page 8	✓	X
16.	Removal of Read-Before-Write mode on dual-port LSRAMs, page 8	✓	✓
17.	LSRAM does not support non-pipelined ECC configuration when SET mitigation is OFF, page 8	✓	✓
18.	SmartDebug of LSRAMs requires handshake logic to prevent data corruption when switching between user mode and SmartDebug access, page 8	✓	✓
19.	Pipelined-ECC LSRAM exhibits data output errors and ECC flag errors upon de-assertion of BLK select input after issuing a RAM read, page 8	✓	✓
20.	TMR-PLL does not automatically recover lock if loss of lock occurs in radiation environment, page 9	✓	✓
21.	PLL exhibits lock stability issue at high temperature after reset at cold temperature, page 9	✓	✓
22.	UG0573: RTG4 FPGA High Speed DDR Interfaces User Guide incorrectly listed support for dynamic write-leveling and read-training, page 9	✓	✓
23.	Assignment of VREF pin to I/O pin which is a P-side of an I/O pair is prohibited when corresponding N-pad is used as an output, page 9	✓	✓

Note: “✓” indicates that the errata exists for that particular device and revision number.

Note: “X” indicates that the errata does not exist or the feature does not exist for that particular device and revision number.

Note: Contact *Microsemi Global support* if you have additional questions. To order a specific die, contact your local Microsemi sales office.

2.4 Reference Documents

The following documents are referenced in this RTG4 FPGA errata document:

- *RTG4 ES Description*
- *RTG4 MS Description*
- *Prototyping for Space-Flight Designs with Microsemi RT-PROTO FPGAs*
- *SpaceWire Pin Mapping from RTG4 ES/MS Silicon to PROTO/Flight Silicon for RTG4 Development Kit*
- *RTG4 ES Development Kit Release Notes*
- *DS0131: RTG4 FPGA Datasheet*
- *DS0130: RTG4 FPGA Pin Descriptions*
- *UG0576: RTG4 FPGA System Controller User Guide*
- *DG0622: RTG4 FPGA PCIe Data Plane Demo using Two Channel Fabric DMA Demo Guide*
- *AC439:Board Design Guidelines for RTG4 FPGAs Application Note*
- *AC439: RTG4 FPGAs Board Design and Layout Guidelines Application Note Addendum*
- *PCN 18009*
- *PCN 18011*

3 Errata Descriptions and Solutions

3.1 SPI-Slave programming interface not supported

SPI-Slave Programming Mode has been removed from both ES/MS devices and PROTO/Production devices. The ES/MS devices did not support it. The removal of this programming mode from the PROTO/Production devices was related to the recommended usage of System Controller Suspend mode for flight applications. Reprogramming the device with system controller suspend mode enabled requires that the JTAG TRSTB input be driven high during power-up to keep the system controller in an active state. Therefore, for flight applications, SPI programming mode was still dependent on the JTAG interface. Thus, in practical applications, it makes sense to support only the JTAG programming interface for all device revisions.

3.2 VPP ramp time must be greater than 5 ms to ensure device functionality and performance upon power up

This condition is not valid if the power supply sequencing guidelines mentioned in the *AC439:Board Design Guidelines for RTG4 FPGAs Application Note* are followed. To ensure correct device start-up, both V_{PP} and V_{DD} must be brought down to 0 V during power-cycling, or anytime either V_{PP} or V_{DD} falls below the recommended operating voltage, before powering up again. Bringing VPP down and then powering up VPP without bringing V_{DD} down is not allowed. They can be brought down in any sequence but both must be brought down before they are again powered up.

3.3 12 of the 16 SpaceWire pins are available

To ensure pin compatibility (SpaceWire and Global pins) from ES devices to the production/PROTO silicon revision and to help design to the production silicon revision, refer to the *SpaceWire Pin Mapping from RTG4 ES/MS Silicon to PROTO/Flight Silicon for RTG4 Development Kit* guidelines and *RTG4 ES Development Kit Release Notes* along with the ES and Production package pin names mapping sheet, SpaceWire Pin Mapping from RTG4 ES-MS Silicon to PROTO-Flight Silicon. The pin names mapping sheet shows the changes in the package pin names along with the bank number changes, if any.

3.4 SpaceWire RX recovered clock has high jitter

For the ES/MS device, the SpaceWire RX recovery circuit will operate with up to 1 ns of jitter. SpaceWire recovered clock jitter has been improved in production/PROTO devices to be within 200ps typical, 500ps max, per the *DS0131: RTG4 FPGA Datasheet* JITSWCLK parameter.

3.5 The maximum I/O frequency is lower than the RTG4 Datasheet specification by 10%

This restriction applies to all I/O types (MSIO, MSIOD, and DDRIO). This limitation was resolved in the production/PROTO device revision.

3.6 I/O drive strength (IOL/IOH) is lower than the Datasheet specification by 30%

This restriction applies to all I/O types (MSIO, MSIOD, and DDRIO). This limitation was resolved in the production/PROTO device revision.

3.7 Fabric PLL output frequency could be lower than expected

In some cases, the output frequency could be different than what is specified. For ES/MS devices, monitor the PLL out frequency and if the frequency is not what you specified, contact Microsemi technical support.

Production silicon does not have this issue.

3.8 SmartDebug Probe Write is not supported for ES/MS devices

3.9 SmartDebug Live Probe feature is not supported when SYSRESET macro is used in the design

If the SYSRESET macro is used, the design will reset upon using the Live Probe feature. When using the SYSRESET to generate the power-on-reset signal, do not use the Live Probe feature.

This limitation was resolved in the production/PROTO device revision.

3.10 PCIe x1 lane configuration is supported

PCIe® x1 lane3 is the recommended lane to use. For ES, PCIe x1 lane0 can be used for design prototyping. Refer to the *DG0622: RTG4 FPGA PCIe Data Plane Demo using Two Channel Fabric DMA Demo Guide* document for more details.

PCIe x2 and x4 lane configurations are supported in production/PROTO devices.

3.11 I/Os states during programming mode do not match with "I/O State During Programming" user settings

User I/Os (MSIO, DDRIO, and MSIOD) can be configured to be at a specific state during programming using the "I/O State During Programming" option settings. These states can be as follows:

- 1 – I/O is set to drive out logic high
- 0 – I/O is set to drive out logic low
- Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming
- Z (TriState) – I/O is tristated

For ES or MS, during programming mode, the I/O state is as follows.

Table 3 • **I/O State (MSIO and MSIOD) during Programming Mode**

User Selection I/Os State during Programming	Entering Programming	During Programming	Exiting Programming
"1"	1 (weak)	1 (weak)	1 (weak)
"0"	0 (weak)	1 (weak)	1 (weak)
"Last Know State"	BSR Drive (hard)	BSR Drive (hard)	1 (weak)
"Z"	Z	1 (weak)	1 (weak)

Table 4 • **I/O State (DDRIO) during Programming Mode**

User Selection I/Os State during Programming	Entering Programming	During Programming	Exiting Programming
“1”	1 (weak)	1 (weak)	Z
“0”	0 (weak)	1 (weak)	Z
“Last Know State”	BSR Drive (hard)	Z	Z
“Z”	Z	1 (weak)	Z

Note: BSR Drive (hard) indicates that the boundary scan register (BSR) is actively driving the I/O pad with the last known state using sample instructions:

- This Errata item is now fixed in the production/PROTO silicon revision.
- RTG4 devices are shipped as blank from the factory. I/Os of a blank RTG4 device will be tristated and weakly pulled-up during programming.
- I/Os of a programmed RTG4 device will be in the last known states, if no state is selected during programming.

3.12 For dual-port RAM (LSRAM), read data does not match with written data in Feed-through x36, x18, x12 or x9 configurations

In feed-through, write data appears on the corresponding output data port immediately or one clock cycle later if output is registered. Write feed-through is not supported for all configurations.The output read data on Port A does not match the input write data in the following configurations:

- LSRAM – Configured as dual-port configuration
- Port A – Configured as: x36, x18, x12 or x9 and in feed-through (register and non-registered)
- Port B – The issue is seen irrespective of how Port B is configured (Port B read data is not affected)

3.13 During boundary scan or programming, a higher than expected current can be observed on the SERDES_x_Lyz_VDDAIO

The SERDES_x_Lyz_VDDAIO is the TX/RX analog I/O voltage for SERDES lanes. It refers to the low voltage power for Lane-y and Lane-z of SERDES_x. See the *DS0130: RTG4 FPGA Pin Descriptions* for more information.

A current of 100 mA may be observed.The current will not cause any issue with programming, functionality or reliability of the device. After the completion of any boundary scan instruction or programming, the current immediately drops down to the typical standby current, as specified in the Datasheet. See the *UG0576: RTG4 FPGA System Controller User Guide* for more information on the list of boundary scan instructions.

This issue is fixed in the production/PROTO devices.

3.14 214 (MSIO341NB4) and 215 (MSIO341PB4) pins must be tied to V_{DD} 1.2 V in RTG4 CQ352 package engineering samples such as ES and MS

In RTG4 CQ352 package engineering samples, such as ES and MS, pin 214 (MSIO341NB4) and pin 215 (MSIO341PB4) must be tied to V_{DD} 1.2 V.

The power-up to functional sequence does not complete if these pins are not connected to V_{DD} 1.2 V and the RTG4 device will not power up and function as expected.

Migrating PCB designs from CQ352 ES/MS devices to CQ352 PROTO/production devices requires the following steps:

1. Place a 10 kΩ (0.5 W 0805 SMT or similar) pull-up resistor connected to 1.2 V on 214 (MSIO341NB4) and 215 (MSIO341PB4) pins when the CQ352 ES/MS device is installed on the PCB.
2. Replace the 10 kΩ pull-up resistors with 0 Ω (0.5 W 0805 SMT or similar) when the CQ352 PROTO/production device is installed on the PCB.

3.15 Single Asynchronous reset in the ES/MS device

ES/MS has 1 asynchronous reset and production/PROTO devices have up to 206 asynchronous resets in the device.

3.16 Removal of Read-Before-Write mode on dual-port LSRAMs

RTG4 Dual Port LSRAM will no longer have any native support for simultaneous read and write operations at the same address on the same port. The remaining write mode capability is the “Simple Write” mode (WMODE = “00”), which has no built-in collision prevention or detection. Designs that attempt to simultaneously read and write to the same address must be modified to ensure that no simultaneous read and write operations exist on RTG4 LSRAM, either by instantiation or inference. For a given clock cycle and LSRAM address, the RAM port must either perform a write or a read operation.

For more information about RTG4 LSRAM Read-Before-Write Mode Data Errors, see *PCN18011*.

3.17 LSRAM does not support non-pipelined ECC configuration when SET mitigation is OFF

When RTG4 LSRAM blocks are configured in non-pipelined ECC mode, without SET mitigation enabled, a timing issue in the LSRAM ECC circuits can generate incorrect ECC code words and in turn allow read-back of falsely corrected data and flag outputs. For correct operation in non-pipelined ECC mode, SET mitigation must be enabled.

For more information about RTG4 LSRAM ECC Errors, see *PCN18009*.

3.18 SmartDebug of LSRAMs requires handshake logic to prevent data corruption when switching between user mode and SmartDebug access

To prevent LSRAM data corruption, the user design must disable write access to the LSRAM before executing a SmartDebug Memory Debug command. The switch between user mode and SmartDebug access can incorrectly lead to a write operation on the LSRAM. To avoid this, the user logic should gate off the LSRAM Block Select (BLK_x) and Write Enable (WEN_x) inputs before switching to SmartDebug LSRAM access. For more information, see *CN19001*.

3.19 Pipelined-ECC LSRAM exhibits data output errors and ECC flag errors upon de-assertion of BLK select input after issuing a RAM read

Pipelined-ECC LSRAM use-models that actively toggle the BLK select input can encounter a data output error when the associated port's BLK select input is de-asserted after issuing a read. De-asserting the BLK select input after issuing a read clears the internal RAM read-data latch before the ECC decoder pipeline register can capture the valid RAM data. This LSRAM internal timing issue allows all-zero data to shoot-through to the RAM DOUT port, resulting in read data errors and ECC error flag assertion. Libero SoC v11.9 SP3 and v12.1 includes updated RTG4 LSRAM configurator cores that add fabric wrapper logic to avoid the issue described above. If the user design actively toggles BLK select inputs, Microsemi recommends migrating all pipelined-ECC RAM components to the updated LSRAM cores in Libero SoC

v11.9 SP3 or v12.1. An RTG4 Customer Advisory Notice will be published, along with an updated RTG4 Fabric User's Guide, to provide additional details about the issue and the mitigation.

3.20 TMR-PLL does not automatically recover lock if loss of lock occurs in radiation environment

When the PLL is configured for triple redundant configuration via the selection of PLL Internal feedback mode, it can experience a loss of lock that will not self-recover and requires assertion of the PLL_ARSTN_N reset input to regain lock. During this time, the clock output from the triple redundant PLL will continue to run, however, the quality of the clock (frequency stability, jitter) has not been determined. Libero SoC v11.9 and RTG4 Fabric CCC Configurator Core v1.1.226 introduced an auto-reset circuit using fabric logic to ensure the triple-redundant PLL automatically resets and re-acquires lock in such scenarios.

For more information about RTG4 PLL in Internal Feedback Mode (TMR Mode), see *PCN18009.7*.

3.21 PLL exhibits lock stability issue at high temperature after reset at cold temperature

RTG4 fabric PLLs, FDDR FPLLs, and SerDes PCIe/XAUI SPLLs can exhibit a loss of lock when released from reset at cold temperatures and operated at high temperatures. At reset release, the PLL automatically selects a VCO gain setting. However, the automatically selected VCO gain setting does not have sufficient margin to maintain the required VCO frequency as the operating temperature rises significantly above the reset temperature. A PLL reset can be applied to recover from the loss of lock. Resetting the PLL at higher temperatures will cause the PLL to select a higher VCO gain setting, and therefore operate at higher temperatures.

For more information, see *CN19009*.

3.22 UG0573: RTG4 FPGA High Speed DDR Interfaces User Guide incorrectly listed support for dynamic write-leveling and read-training

Earlier versions of UG0573: RTG4 FPGA High Speed DDR Interfaces User Guide, prior to revision 4, contained misleading references to dynamic write leveling and dynamic read training support when using the FDDR in DDR3 mode. This document has been updated to provide an accurate description of the DDR3 DRAM training support in the FDDR. References to the support for dynamic write leveling and read training have been removed. Additionally, the RTG4 Board Design and AC439: Board Layout Guidelines Application Note has been updated with trace length-matching guidelines for DDR3 interfaces.

For more information about this change, see *CAN18009.4* for more information.

3.23 Assignment of VREF pin to I/O pin which is a P-side of an I/O pair is prohibited when corresponding N-pad is used as an output

In the device I/O configuration, the Output Enable (OE) of the I/O pair where VREF is assigned to the P-side was incorrectly tied to ‘0’, resulting in high-Z state on any user output assigned to the corresponding N-side. Libero SoC v11.8 SP2 and later will generate a error, which prevents the user from creating the scenario described above. For more information, see *CAN 18002.1*.