Libero SoC RTG4 Launch Software Release Notes

Libero SoC RTG4™ Launch software is a release specifically for designing with the new RTG4 family of Radiation-Tolerant FPGAs. Microsemi recommends not to use this software release to design any other Microsemi FPGA family!

Libero SoC RTG4 Launch software is a complete release including synthesis and simulation tools. The software features are a subset of those included in the Libero SoC v11.5 release. Microsemi recommends reading the Libero SoC Overview and the Libero SoC v11.5 Release Notes.

What's new in RTG4 Launch Software

Device Support

Die	Package	Speed Grades	Core Voltage	Temperature	Programming
RT4G150	1657 CCGA/LGA	STD, -1	1.2V	MIL	Disabled
RT4G150_ES	1657 CCGA/LGA	STD	1.2V	MIL	Enabled

RT4G150_ES refers to the Engineering Samples (ES) of the RT4G150 device. The **RT4G150_ES** devices use a PLL without the Triple Module Redundancy for radiation mitigation, that is different from the **RT4G150** devices.

Caution: **Customers should not use RT4G150-CG1657 device package pin reports generated by the RTG4 Launch software for PCB designs. Please refer the RTG4 errata in Microsemi website at http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtg4#documents for more details.**

Program Design

Programming capability is enabled for **RT4G150_ES** device in the Libero SoC RTG4 Launch software.

Programming options

Programming options are enabled for **RT4G150_ES** device in the Libero SoC RTG4 Launch software.

- Edit Design Hardware Configuration
  - Device I/O States During Programming
  - Programming Connectivity and Interface
  - Programmer Settings
- Configure Programming Options
  - Configure User Programming Data
    - Design version (number between 0 and 65535)
    - Silicon signature (max length is 8 HEX chars)
  - Configure Programming Bitstream Settings
    - Enable System Controller Suspend mode
    - Disable JTAG interface
    - Disable SPI interface
    - Disable Fabric Erase/Write/Verify
    - Disable Probe Read/Write
    - Disable Digest Check

Export Bitstream

Exporting Bitstream files is enabled for **RT4G150_ES** device in the Libero SoC RTG4 Launch software.

Note: *DAT* file is not supported in the Libero Soc RTG4 Launch software.

Export BSDL

Exporting BSDL files is enabled for **RT4G150_ES** device in the Libero SoC RTG4 Launch software.

SmartDebug Design

SmartDebug capabilities are enabled for **RT4G150_ES** device in the Libero SoC RTG4 Launch software.

- Probes
  - Active Probe
  - Live Probe – only one Live probe is available in RTG4 devices.
  - Post-route Probe Insertion
- Memory debug

Note:

- For the FPGA memory and live probe SmartDebug functions to work properly in Libero flow, the following DEF variables need to be added to the sdebug.def file in the data directory:

  data SMART_DEBUG_USE_12BIT_MODE 0 OVERRIDE

  data SMART_DEBUG_DISABLE_JTAG_RESET 1 OVERRIDE

- Memory Debug supports only 9-bit mode.

Post-layout Simulation

Generation of Back-Annotation files and post-layout simulation are enabled in the Libero SoC RTG4 Launch software.

Multi-standard I/Os and I/O Attributes

A rich set of I/O standards are available across different I/O banks and I/O voltages. The selection of I/O attributes is updated in the Libero SoC RTG4 Launch software.

Important Note for Designs Created with Libero SoC RTG4 LCP Software

The following output drive strengths have been discontinued since Libero SoC RTG4 LCP-3 SP1 release.

MSIO	MSIOD
LVCMOS 3.3 V, 20 mA	LVCMOS 1.5 V, 8 mA
LVTTL 3.3 V, 20 mA	LVCMOS 1.8 V, 10 mA
LVCMOS 1.2 V, 8 mA	LVCMOS 2.5 V, 12 mA
LVCMOS 1.2 V, 6 mA	HSTL 1.8 V, Class II
LVCMOS 2.5 V, 16 mA	
HSTL 1.8 V, Class II	

Due to these changes designs created with the Libero SoC RTG4 LCP-3 SP1 release or prior releases are invalidated and previous I/O pdc files should be updated accordingly.

Dual-Port Large SRAM (LSRAM)

Libero SoC RTG4 Launch software includes a dual-port large SRAM Configurator, which offers the following features specific to RTG4:

- Read-before-write
- Read-enable
- Embedded ECC flags (optionally pipelined) in x18 width
  - Write-feed-through and Read-before-write modes add additional two clock cycles when ECC flags are pipelined.
- Non-ECC x12 widths
  - The simulation MEMORY file size is 2Kx12 in such cases.
- Single Asynchronous reset signal

Two-Port Large SRAM (LSRAM)

Libero SoC RTG4 Launch software includes a two-port large SRAM Configurator, which offers the following features specific to RTG4:

- Embedded ECC flags (optionally pipelined) in x18 and x36 widths.
- Non-ECC x12 widths
    - The simulation MEMORY file size is 2Kx12 in such cases.
- Single Asynchronous reset signal

Three-Port Micro SRAM (uSRAM)

Libero SoC RTG4 Launch software includes a micro SRAM Configurator, which offers the following features specific to RTG4:

- Embedded ECC flags (optionally pipelined) in x18 width
- Non-ECC x12 widths
    - The simulation MEMORY file size is 128x12 in such cases.
- Single Asynchronous reset signal

Clock Conditioning Circuit (CCC) and Globals

The CCC Configurator for RTG4 includes RX clock and data recovery options necessary for SpaceWire applications. The Strobe and Data pins for SpaceWire can be single-ended or differential I/O standard. They can also be directly connected to a DDR_IN macro.

The **RT4G150_ES** device supports only the *No automatic resynchronization* selection for the *Output Resynchronization after lock* option either when the PLL Feedback is CCC internal or external. The other two selections (in the Configurator GUI) are available when the feedback is selected as PLL internal.

Important Note for Designs Created with Libero SoC RTG4 LCP Software
Designs created with the Libero SoC RTG4 LCP-3 SP1 release or prior releases have to use the latest cores and configurators in the Catalog.

For more information about the latest core versions available and to know about downloading configurator versions and replacing configurator in the design, refer to *RTG4 Configurators* section.

1. The following is the list of the ports that have changed in the latest CCC version since Libero SoC RTG4 LCP-3 SP1 release. Ensure to modify the design connections accordingly.

Category	Old Port Name (LCP3-SP1 or prior)	New Port Name
Enable ports	CGL<n>_ENABLE	GL<n>_Y<n>_EN
Reset ports	CGL<n>_ARST_N	GL<n>_Y<n>_ARST_N
Spacewire Data and Strobe ports	CLK0_PAD CLK1_PAD	CLK0_SPWR_STROBE_PAD CLK1_SPWR_DATA_PAD
	CLK2_PAD CLK3_PAD	CLK2_SPWR_STROBE_PAD CLK3_SPWR_DATA_PAD

    - Where <n> can be 0, 1, 2, or 3
    - SpaceWire ports can be single ended or differential

2. The Programmable delay value per step has been updated from 40ps to 100ps. For more information about the **Programmable Delay** option, refer to the **PLL option** page of the CCC Configurator GUI.

Timing Constraints

SmartTime does not automatically infer timing constraints on the output pins of the RCOSC_50MHZ and CCC instances at this time. This feature is planned for a later release. For more information refer to the *RTG4 FPGA Timing Constraints Users Guide*.

Reserve SPI Pins

Four (4) I/O pins for the SPI function are dedicated when the **Reserve Pins for SPI** checkbox is selected in the **Device Settings** page while creating a New Project. This option is also available in the **Project Settings > Device Settings** page.

Total Ionizing Dose (TID) Derating

You can enter Radiation derating in krad units in the *Analysis Operating Conditions* tab of the *Project Settings*. The valid range is 0 (zero) to 100 krad.

Single Event Transient (SET) Mitigation

When the *Single Event Transient (SET) Mitigation* option is selected under *Compile Options,* it activates SET filters globally to help mitigate radiation-induced transients.

The SET filters are disabled by default.

DDR Memory Controller

RTG4 devices contain two independent DDR memory controllers. The configurator for the DDR memory controller has a selection identifying the particular controller being configured.

Note: For more information about the **DDR block initialization**, refer to the DDR Configurator User Guide.

High-Speed Serial Interface (SERDES)

The RTG4 devices contain the following two types of High-Speed Serial Interface blocks:

- Native SERDES ePCS
- PCI Express end-points

Libero SoC RTG4 Launch software includes two High-Speed Serial Interface configurators, one for each type of block.

- PCIe High-Speed Serial Interface Configurator
    - PCIe – Lane width x1 in Gen1 and Gen2 modes (operating at 2.5Gbps)
    - XAUI
    - EPCS
- ePCS High-Speed Serial Interface Configurator
    - ePCS – Lane widths x1, x2, and x4
    - XAUI
    - Multi-protocol ePCS

Each block has a pair of dedicated differential I/Os to source a REFCLK signal. The same pair also serves as two single-ended I/Os. You can get two independent REFCLK signals in the following ways:

- 2 Single-ended I/Os
- 1 Differential I/O and 1 Fabric signal
- 1 Single-ended I/O and 1 Fabric signal

For XAUI and EPCS protocols, the Signal Integrity Dialog box provides control to maintain signal integrity and to mitigate signal integrity problems.

Note: For more information about the initialization, refer to the **RTG4 FPGA High Speed DDR Interfaces User Guide.**

Multiple Pass Layout

Place and Route options to configure the *Multiple passes* are available in the Libero SoC RTG4 Launch software. You can also run *Multiple passes* of *Place and Route* using the batch tcl script "*extended_run_lib.tcl".*

Multiple Pass Layout attempts to improve layout quality, like Timing performance of the design by selecting from multiple number of Layout results. This is done by running individual place and route multiple times with varying placement seeds and measuring the best results with the specified criteria. For more information about **Multiple Pass Layout**, refer to **Multiple Pass Layout Configuration (SmartFusion2, IGLOO2 and RTG4)** section in the Libero SoC online-help.

RTG4 Configurators

Repositories Settings

The default core repositories provide access to all RTG4 Configurators and can be set using the following steps.

1. Launch Libero SoC.
2. Go to **Project > Vault/Repositories Settings**.
3. Select **Repositories in the Options** window.
4. Click **Defaults**.

Downloading Cores or Configurators

The following steps provide information how to download the latest versions of configurators or core.

1. Create a new project or Open a project by selecting **Project > New Project or Open Project.**
2. Select the **Catalog** tab.
3. Browse through the **Catalog** by core/configurators category or you can use search options that is available on the **Catalog** window.
4. After selecting the core, **Double-click** or **Right-click > Download** to download the core.
5. Additionally, use **Download them now** at the bottom of the *Catalog* window to download all new cores available in all the repositories.

Replacing Core or Configurator Version for Designs Created with Libero SoC RTG4 LCP Software

Designs created with Libero Soc RTG4 LCP-3 SP1 or prior release need to replace their configurators and core versions using the following instructions.

1. Open the **Design Hierarchy** in the Project.
2. Select the Configurator's or Core's instance that you want to update or replace in the **Design Hierarchy** pane of Libero SoC.
3. Right click on the instance and select **Replace component version...**
4. Select the version that you want to replace with under **Change to Version** box and click **OK**.
5. Regenerate your design if you are using **SmartDesign** in you project.

RTG4 Configurator Core Versions

The following versions of the RTG4 Configurators are available with Libero SoC RTG4 Launch software:

RTG4 Configurator	Version
RTG4 Clock Conditioning Circuit (CCC)	1.1.204
RTG4 DDR Memory Controller	1.2.402
RTG4 Dual-Port Large SRAM	1.1.105
RTG4 Micro SRAM	1.1.105
RTG4 Two-Port Large SRAM	1.1.104
RTG4 High Speed Serial Interface (EPCS and XAUI)	1.1.208
RTG4 High Speed Serial Interface (PCIe, EPCS, and XAUI)	1.1.207

RTG4 Device Features

- Fabric LUT4
- Fabric flip-flops with built-in TMR support (no latch)
- I/O registers and DDR with built-in TMR
- Multi-standard I/Os and I/O attributes
- 1Kx18 ECC (2Kx12 Non-ECC) Dual-port and Two-port Large SRAM Blocks
- 64x18 ECC (128x12 Non-ECC) Three-port Micro SRAM Blocks
- 18x18 Multiply Accumulate DSP Mathblocks and 9-bit dot-product
- Single global asynchronous reset/set. Each flip-flop has its own synchronous reset.
- 24 globals or 48 half-chip global networks with flexible inputs from I/O, CCC and High Speed Serial Interface blocks
- Clock Conditioning Circuit including PLL and Spacewire clock/data recovery
- 50 MHz RC Oscillator
- DDR SDRAM controllers (with ECC)
- PCI Express end-points
- High Speed Serial Interface blocks supporting ePCS interfaces and XAUI interfaces
- UJTAG
- Power-on-reset
- Total Ionizing Dose (TID) Derating
- Reserve Probe pin
- Reserve SPI pins
- Design level Single Event Transient (SET) Mitigation Filter
- System Controller Suspend mode
- Active Probes
- Live Probe
- Memory debug

Cores

- Arithmetic
  - Hard Multiplier Signed
  - Hard Multiplier AddSub
  - Hard Multiplier Accumulator
- Bus Interfaces
  - CoreAPB3
  - CoreAXI
- Clock & Management
  - RTG4 Clock Conditioning Circuit (CCC)
- I/O
- Memory and Controllers
  - RTG4 DDR Memory Controller
  - RTG4 Dual-port Large SRAM
  - RTG4 Micro SRAM
  - RTG4 Two-port Large SRAM
- Peripherals
  - RTG4 High-Speed Serial Interface (EPCS and XAUI)
  - RTG4 High-Speed Serial Interface (PCIe, EPCS, and XAUI)
- Processors
  - CoreABC
- Several other DirectCores in the catalog

Note: When you create a new project for the first time using Libero SoC RTG4 Launch software, reload the *Catalog* to see SRAM, Multiplier, and I/O Configurators.

Synthesis support with Synplify Pro ME

- Synplify Pro ME J2014.09MSP2

High level synthesis support for DSP design flow with Synphony Model Compiler ME

- Synphony J2014.09M.
- This release does not support RTG4 synthesis library. IGLOO2 synthesis library can be used until RTG4 synthesis library is supported in future releases.

Pre-synthesis and Post-synthesis Simulation Support

- ModelSim ME 10.3c

Power Analysis

- A preliminary Power Calculator Spreadsheet is included.
- SmartPower is not available in Libero SoC RTG4 Launch software.

DirectCores that are not available in Libero SoC RTG4 Launch Software

- CoreI2C
- CoreSDR
- CoreTSE

Device Features that are not supported by Libero SoC RTG4 Launch Software

- SERDES debug
- Automatic timing constraint generation for RC Oscillator and CCC
- uPROM
- Initialization of the contents of 1Kx18 Large SRAM and 64x18 Micro SRAM
- Programming through SPI
- Dynamic configuration of CCC

System Requirements

Platform and Operating Systems

- 64-bit Windows 7 or 64-bit Windows 8.1
- RHEL 5* and RHEL 6, CentOS 5* and CentOS 6
  **RHEL 5 and CentOS 5 do not support programming using FlashPro5*
- **Microsemi recommends a minimum of 12 GB RAM.**

For more information about setting up Red Hat Enterprise Linux for Libero, refer to How to Set Up Your Linux Environment for Libero.

License Requirement

Libero SoC RTG4 Launch software requires a Platinum license to create projects with RTG4 family.

Synopsys and Mentor Graphics Tool Support

These tools are included with the Libero SoC RTG4 Launch software.

- Synplify Pro ME J2014.09M SP2 You must use this Synplify version to take advantage of RTG4 technology mapping.
- ModelSim ME 10.3c
- Synphony Model Compiler ME J2014.09M

Prerequisite Software: In order to run Synphony Model Compiler ME, you must have MATLAB/Simulink by MathWorks installed with a current license. You cannot run Synphony Model Compiler ME without MATLAB/Simulink.

Note: Synopsys Identify Debugger is not supported in this release.

Download Libero SoC RTG4 Launch Software

Installation requires admin privileges. Download links:

- Windows
- Linux

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650. 318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

For Microsemi SoC Products Support, visit http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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