Mitigation of Radiation Effects in RTG4 Radiation-Tolerant Flash FPGAs

WP0191 White Paper

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Background of Flash FPGAs in Radiation Applications

Flash FPGAs have gathered flight heritage in a variety of Low Earth Orbit (LEO) and Lunar space applications. The RT ProASIC®3 FPGA family, using a 130nm Flash fabrication process, can withstand 25 krad to 30 krad of radiation total ionizing dose (TID), which is sufficient radiation tolerance for LEO missions as well as short-duration Geosynchronous Earth Orbit (GEO) and interplanetary missions. However, 20-year GEO missions typically require components that can survive TID of 100 krad. For RT ProASIC3, the limiting parameter for TID is degradation of propagation delay. As the Flash cells that interconnect the routing and logic resources are exposed to radiation, the voltage threshold changes, which manifests as a degradation (slowing down) of propagation delay, to the extent that the FPGA will slow down by 10% at 25 krad to 30 krad. The FPGA will still be functional at this level, but designers need to allow for the reduction in performance by allowing additional timing slack in their design. In order to provide the advantages of Flash-based FPGAs to all space applications, not just LEO and short duration missions, Microsemi® has implemented a Flash interconnect technology on the next generation RTG4™ radiation-tolerant FPGAs, which maintains functionality and performance to a TID level of 100 krad.

In addition to TID effects, designers of equipment for radiation environments must consider Single Event Effects (SEE). Particle radiation can cause glitches in combinatorial logic, bit flips in flip-flops and memory cells, and can even cause destructive latch-up events. All of these effects are mitigated in RTG4, by a variety of "radiation hardening by design" techniques discussed in this document.

The 65nm Flash cells used for configuration of RTG4 have been tested to extreme energy levels and have been shown to be immune to configuration upsets, in contrast to SRAM-based FPGAs where particle radiation can cause configuration changes and device malfunction.

RTG4 Overview

The RTG4 family comprises radiation-tolerant versions of Microsemi's fourth generation of flash-based FPGAs. The family has been developed to provide designers with a selection of high-density, high-performance FPGAs for signal processing applications in radiation environments. Future remote-sensing space systems will have dramatically increased sensor resolution, however, the bandwidth available for transmission of sensor data to ground stations is not expected to increase at the same rate as sensor resolution. Consequently, architects of future space systems are looking for ways to perform as much processing on-board remote sensing satellites as possible, to minimize the amount of data that needs to be transmitted to the ground. RTG4 is intended to satisfy this requirement by providing ample logic resources, hardwired high-speed multiply-accumulate blocks, copious embedded memory, and high-throughput serial transceivers, with the reliability, qualification and radiation tolerance required for space deployment. RTG4 FPGAs are fabricated using a 65nm Flash technology, which provides industry-leading low power consumption and also provides complete immunity to radiation-induced configuration upsets. Consequently, the RTG4 devices never lose their functionality in the harsh space radiation environment. An additional advantage of Flash technology is that the configuration of the FPGA is retained through power cycles, unlike SRAM-based FPGAs, meaning that no companion devices are required for code storage, relieving board space, and eliminating additional component cost.

Mitigation of Radiation Effects

RTG4 radiation effects mitigation includes radiation hardening by design for total dose effects and for single event effects.

Total Ionizing Dose Hardening

Commercial Flash based FPGAs such as Microsemi's IGLOO®2, SmartFusion®2, and ProASIC3 devices use a single Flash cell to make a connection between two routing tracks, or to connect a routing track to an input or output of a logic element. This architecture, which has been implemented on all four generations of Microsemi Flash FPGAs is the most cost-effective for commercial FPGAs, and minimizes the silicon area used for interconnect resources. Figure 1 shows this directly coupled interconnection scheme. For FPGAs intended for radiation environments, however, it has the disadvantage that as the device is exposed to ionizing radiation, charge accumulates on the floating gate, and causes the voltage threshold of the pass transistor to change. This manifests as a degradation in propagation delay, causing signals to slow down. Data gathered from TID testing on multiple lots of 130nm ProASIC3 and 65nm SmartFusion2 Flash FPGAs indicates that signals slow down by 10% at around 25 krad to 30 krad. In order to provide Flash FPGAs that are capable of surviving 100 krad of radiation exposure without propagation degradation, an alternative interconnection scheme is required.

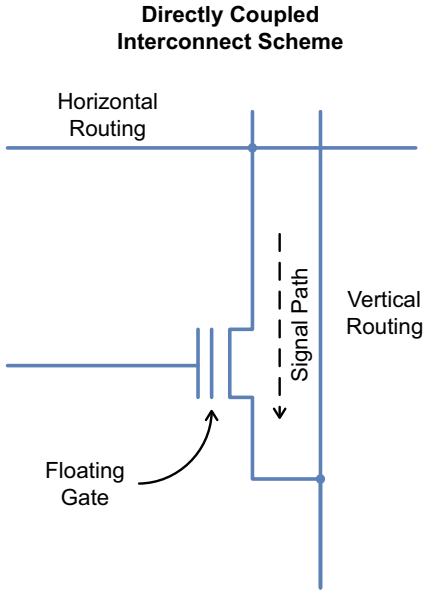

Figure 1: Directly Coupled Interconnection Scheme

Microsemi has developed an **Indirectly Coupled** interconnection scheme for the RTG4 radiation tolerant FPGAs. In this scheme, the data signal does not pass directly through the Flash transistor. Instead, it passes through a conventional pass transistor. The pass transistor is held in the **on** or **off** state by a pair of Flash transistors in push-pull configuration. Any change in voltage threshold of these transistors caused by accumulation of charge in their floating gates, does not result in a change in the state of the push-pull pair until the voltage threshold degrades past the switching threshold of the transistors, which is at a TID level considerably higher than 100 krad.

Initial TID testing performed on RTG4 FPGAs and on test structures built using the **Indirectly Coupled** interconnection scheme have shown that RTG4 FPGAs are able to tolerate TID to levels beyond 100 krad without degradation of propagation delay or loss of functionality.

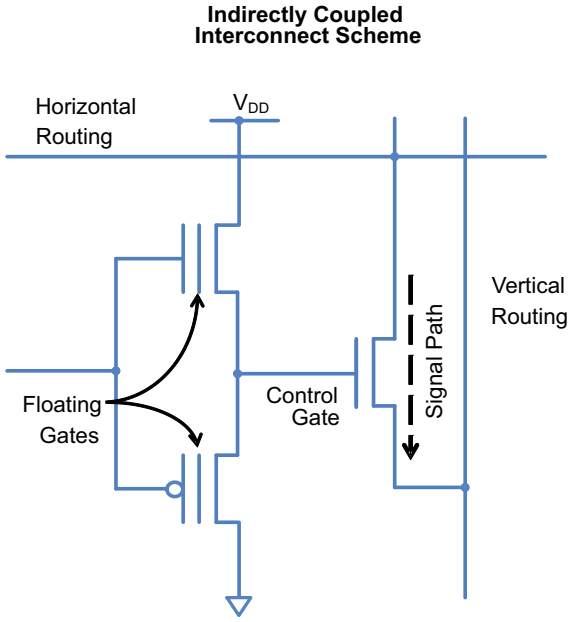

Figure 2: Indirectly Coupled Interconnection Scheme

Single Event Effect Hardening

The effects of particle radiation have been mitigated in several different areas.

The following sections describe single event effect hardening:

- Single Event Latch-Up Hardening
- Single Event Configuration Upset Hardening
- Single Event Data Upsets in Flip-flops
- Single Event Data Upsets in SRAM Blocks
- Single Event Clock Upsets
- Single Event Transients in Combinatorial Logic and Mathblocks
- Single Event Effects in Phase Locked Loops

Single Event Latch-Up Hardening

The RTG4 FPGAs are manufactured on a bulk 65nm CMOS process with an epitaxial layer. The design rules of RTG4 were carefully chosen to eliminate the possibility of SEL in heavy ion radiation, based on a combination of heavy ion beam experiments on test chips and commercial 65nm Flash FPGAs (IGLOO2 and SmartFusion2), and simulation using correlated TCAD models. Design-rules of structures on RTG4 were chosen to provide sufficient low-resistance paths to render harmless any parasitic diode effects, which can cause latch-ups.

Single Event Configuration Upset Hardening

As described in the"Total Ionizing Dose Hardening" section, the RTG4 FPGAs use a pair of Flash transistors in push-pull configuration to connect or disconnect routing tracks. For a heavy ion to cause a configuration upset, it would need to charge or discharge the floating gate in one of the two Flash transistors significantly to change the state of the control gate. Comparing to a commercial 65nm configuration Flash cell, the Flash cells used in RTG4 have significantly greater tolerance to charge or discharge in the floating gate because the switch transistor in the data path is indirectly coupled to the floating gate. Heavy ions found in solar and cosmic radiation do not possess high enough LET (linear energy transfer) to cause a state change of the control gate in RTG4.

Indirect evidence supporting this comes from the SEE test results of commercial 65nm Flash-based FPGAs: 48 units of Microsemi M2S050 SmartFusion2 commercial FPGAs were exposed to heavy ions at LET levels up to 90.3 MeV-cm^2/mg in ten separate test campaigns at Lawrence Berkeley National Laboratory (LBNL) and Texas A & M University Cyclotron facility (TAMU). Functionality of the FPGAs was monitored continuously during radiation exposure. Any change in configuration due to radiation would have resulted in a functional upset of the data path, non-recoverable by power cycling, requiring the flash array to be reprogrammed. No configuration upsets were detected in the 48 parts with a total fluence of 2.83 x 10^9 heavy ions.

The significance of configuration upsets should not be underestimated. Flight-critical or mission-critical applications require FPGAs to retain their configuration in radiation environments. The preceding generation of Microsemi radiation tolerant Flash FPGAs (RT ProASIC3) has exhibited a complete absence of radiation-induced upsets in the Flash cells, which control the configuration of the FPGA. This is in direct contrast to SRAM-based FPGAs, which exhibit single event upsets in the SRAM configuration memory cells that configure the function of logic cells and connects the routing tracks together. These radiation-induced single event upsets cause the SRAM FPGAs to change their function and behave unpredictably. Mitigation of configuration upsets in SRAM FPGAs is complex and cumbersome, and moreover it is not wholly effective because the mitigation schemes work by overwriting a corrupted configuration bit with a correct configuration bit. The corrupted configuration bit causes device malfunction from the occurrence of the single event until it is corrected a period of at least several hundred milliseconds.

During this time the corrupted device behaves unpredictably, pouring erroneous data into the system. A demonstrated absence of configuration upsets due to radiation is an essential property for FPGAs being deployed in high reliability and mission-critical systems.

Single Event Data Upsets in Flip-flops

All flip-flops deployed in RTG4 FPGAs are protected against single-bit data upsets. As with prior generations of Microsemi RT FPGAs (RTSX-SU, RTAX-S/SL/DSP), each SEU-protected flip-flop is implemented as a triple-redundant structure with majority voting implemented on each group of three latches. A single event upset causing a bit flip in one of the latches is immediately detected and corrected by the asynchronous voting circuit, to eliminate the upset before it propagates outside of the flip-flop.

Figure 3 shows a simplified schematic diagram of the SEU-protected flip-flop. Preliminary testing indicates that the SEU-protected flip-flops in the RTG4 FPGAs exhibit fewer than 1 x 10^{-10} errors/bit-day in geosynchronous solar minimum conditions. The probability of a single radiation event causing multiple latches to upset in the same SEU-protected flip-flop is extremely low because the redundant latches are physically dispersed on the silicon.

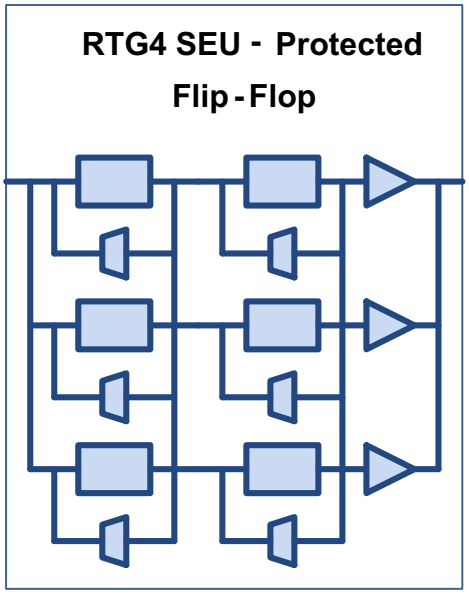

Figure 3: RTG4 SEU-Protected Flip-Flop

Single Event Data Upsets in SRAM Blocks

The RTG4 FPGAs include two different sizes of user SRAM blocks - Large SRAM (LSRAM), comprising 24,576 bits, and Micro SRAM (uSRAM), comprising 1,536 bits. Each of these memory structures features optional hard-wired error detection and correction (EDAC) circuits, to prevent single bit data errors caused by particle radiation. EDAC is implemented as a standard shortened Hamming code to provide single error correct, and double error detect (SECDED) capability. EDAC is available when the SRAM blocks are configured for data widths of 18 bits or higher. Hardwired EDAC is not available on any SRAM block when it is configured for data width of less than 18 bits.

Background scrubbing circuits are not implemented as hard-wired circuits in the RTG4 silicon—the scrubbing requirements are very much dependent on the details of each individual design, so it is left to the designer to choose the most appropriate memory scrubbing circuit for the application. With EDAC deployed and a suitable background scrubbing circuit in place, Microsemi expects that the LSRAM and uSRAM in RTG4 FPGAs will exhibit fewer than 1 x 10^{-10} errors/bit-day in geosynchronous solar minimum conditions. Multiple-bit upsets are effectively mitigated by the interleaving of logical bits in the physical memory blocks in Microsemi FPGAs.

Figure 4 shows a simplified illustration of this principle. By physically separating logically-adjacent memory bits, high energy particles causing upsets in multiple physically adjacent bits cause only single-bit errors to logical words, which are easily corrected with the low-overhead error detection and correction encoding scheme deployed in the RTG4 FPGAs.

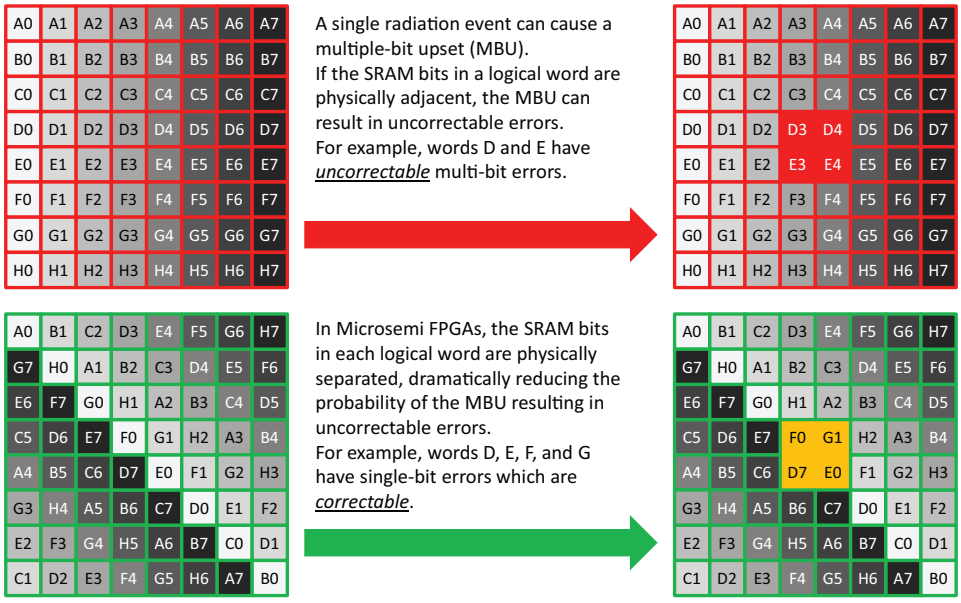

Figure 4: Mitigation of Multiple Bit Upsets by Physical Interleaving of Memory Cells

Single Event Clock Upsets

Upsets and transients in the clock network are mitigated by enhanced clock buffer transistors and wider metal tracks. Stronger drivers and lower resistance networks reduce the possibility of particle radiation causing a transient on the clock network, which can result in unintentional (false) clocking of flip-flops.

Single Event Transients in Combinatorial Logic and Mathblocks

Single Event Transients (SETs) have become of increasing concern to designers of high performance microcircuits for applications in radiation environments. Two factors contribute to designers' increased vigilance - firstly, as manufacturers of integrated circuits have adopted ever more advanced fabrication processes with finer feature sizes and lower operating voltages, the critical charge a radiation particle needs to deposit in order to cause a glitch in combinatorial logic decreases dramatically. Consequently, a greater proportion of particles in solar and cosmic radiation are capable of causing a glitch. Secondly, as operating frequencies have increased, the probability of a combinatorial logic transient occurring within the set-up or hold time of a flip-flop increases.

The consequences of an SET depend on the circuit in which it occurs. A signal processing circuit processing video data at several Gigabits per second may find occasional SETs inconsequential. However, in a control logic circuit, rare SETs may not be tolerable. For this reason, Microsemi has implemented a flexible approach to SET filtering in the RTG4 FPGAs.

Each flip-flop in the programmable logic cells and Mathblocks of RTG4 are provided with SET filters, which can be optionally deployed by designers. Each SET filter is implemented as a guard gate plus delay. Essentially, the function of this structure is to eliminate transients on the D input of duration less than the delay length. The incoming signal (S) is split into two paths, one path going directly to the input of the guard gate, and the other passing through a delay Δ_T before reaching the input of the guard gate (S'). If S and S' have the same value, then the guard gate will output that value. If S and S' have differing values, then the guard gate outputs its prior state until S and S' once again are in agreement.

Figure 5 shows the principle and schematic of the SET filter.

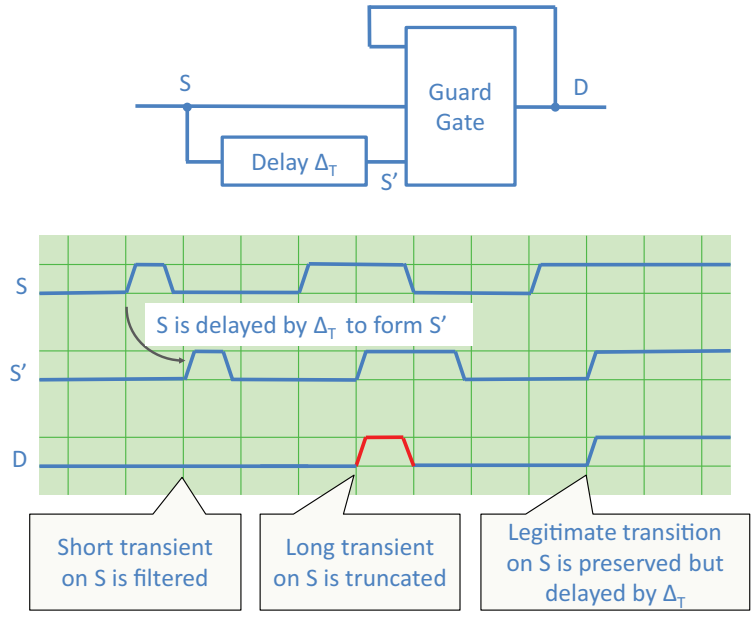

Figure 5: Implementation of SET Filters using Guard Gates with Delay

On RTG4, the SET filter delay value is nominally 600 psec, and is compensated for variation in process, voltage, and temperature. The designer may choose to implement or not implement the SET filter on a selective basis. Filtering can be selectively enabled or disabled on individual flip-flops, on functional blocks, on specific clock domains, or on the entire FPGA at the designer's discretion.

Single Event Effects in Phase Locked Loops

The Phase Locked Loops (PLLs) in the clock conditioning circuit blocks feature protection for radiation single event upsets. Figure 6 shows a block diagram of the PLL design. Within the RT PLL block, there are three redundant PLLs. When the PLL is operating in internal feedback mode, the PLL output is fed back to all three internal PLLs through a voter circuit. In the external feedback mode, the external feedback signal is fed to a single PLL. In this case, only one of the three redundant PLLs in the RT PLL block will be enabled. The input divider ÷R is triple-redundant. The feedback divider ÷F is not triple-redundant because radiation induced transients in the feedback divider path will be filtered by the VCO.

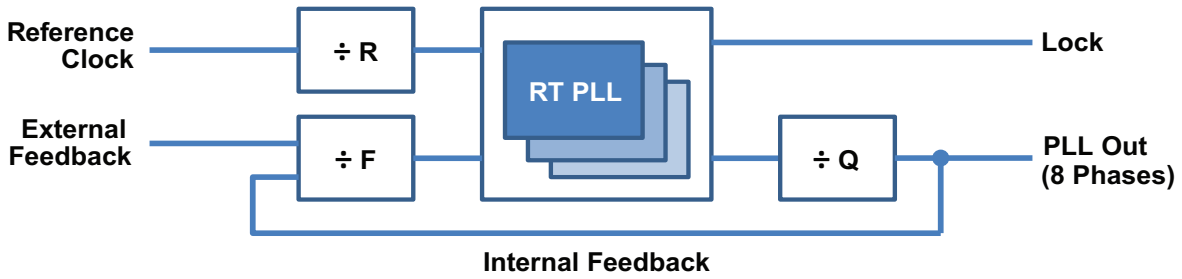

Figure 6: Block Diagram of RTG4 PLL

Conclusion

Microsemi's RTG4 radiation-tolerant FPGAs offer significant performance and flexibility advantages to designers of satellite systems and other equipment intended for high radiation environments. The intrinsic immunity of Microsemi's 65nm Flash cells prevents the occurrence of FPGA configuration changes due to radiation effects. In addition, Microsemi has implemented several "radiation hardening by design" techniques to achieve a high level of total dose hardness and to maintain data integrity in flip-flops, combinatorial logic, Mathblocks, and memory structures. Consequently, RTG4 FPGAs can be used to solve signal processing problems in most radiation environments without sacrificing reliability.

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