Analog Front End Integrated Circuits for Mixed Signal Spacecraft Applications

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Abstract

By definition mixed signal systems include a digital processing function and an analog or power function. When complex circuits are integrated to reduce parts count, it is typically not optimal to combine the analog and digital portions in one device. Application targeted Analog Front End (AFE) ICs tend to be a more efficient combination of circuitry than a random programmable analog array. By partitioning the majority of the digital circuitry in a programmable device such as an FPGA, control functionality can be readily programmed using an intuitive hardware definition language such as VHDL or Verilog. An AFE reduces the number and complexity of the analog to digital communication links.

I. Introduction

Digital electronics are designed to function at low voltages to minimize power dissipation due to logic transitions. The digital sensor interfaces that are present in the spacecraft environment typically must be buffered to be compatible with I/O thresholds of the digital circuits. [1] Provision must be made for ground references within the spacecraft which introduce common mode voltage differences between the sensor and monitoring equipment. Linearly varying signals are not compatible with logic and must therefore be sampled and converted to digital format. Power delivery is not possible with the limited current sourcing ability of the digital I/O. Redundant control interfaces require cold sparing which is typically not supported by digital I/O. Table 1 summarizes typical signal conditioning provided by the AFE.

Table 1: Typical AFE signal conditioning functions

- Differential Receiver
- Level Shifting
- ADC or DAC Converters
- Power Driver
- Cold Sparing
- Bi-level logic buffer

II. Discussion

The best approach for implementing an AFE is to target a specific range of applications and combine the commonly used functions for those applications. A more flexible approach is to implement the design using single function ICs, but this has the drawback of requiring a large number of components and circuit board area. A more integrated solution is to design a fully custom AFE for a particular application; this is the least flexible solution if the requirements change. The development of custom ICs also presents a schedule risk and requires the investment of NRE costs. Another approach is configurable general purpose analog circuitry; the popularity for these parts comes from the metaphor they represent AFEs with configurable higher level functions. [2] Table 2 summaries the pros and cons of the first three approaches.

Table 2: AFE implementation approach comparison

	Single Function ICs	AFE	Custom
NRE	Low	Low	High
Development Time	Months	Months	Years
Qualification	Fast	Fast	Long
Risk	Small	Small	High
Flexibility	High	High	None
Power	Worst	Good	Best
Reliability	Average	Excellent	Excellent
Size and Weight	Poor	Good	Best

The development time and schedule risk are reduced when the AFE solution is available as a prequalified standard part. Reducing the part count through integration helps reduce size and weight and improves reliability at the system level.

FPGA processes optimized for spacecraft SEE immunity have specific provisions such as Triple Modular Redundancy with voting logic help mitigate single event upsets due to radiation. [3] Anti-fuse programming offers better retention than other forms of reconfigurable logic. The FPGA utilizes a smaller geometry process than can be used to implement radiation tolerant mixed signal designs; this results in denser more highly integrated solutions than are possible with a mixed signal process. AFE processes can utilize higher voltage devices that tolerate a wide range of input voltages. Processes with dielectric isolation (DI) allow for fault tolerance between sections of circuitry such that a failure in one place on the die does not impact adjacent circuits.[4] Bipolar CMOS DMOS (BCD) processes provide a combination of bipolar devices for developing precision bandgaps and linear circuits, CMOS devices for logic and switches and DMOS devices for high current capability. The separation of the digital functions from the analog and power functions allows for process optimization of both resulting in smaller size, increased reliability and improved performance.

Table 3: Specialized digital and analog process advantages

Process	**Attribute**	**Advanatage**
Digital	Small geometry	High density
	Anti-fuse	High retention
	Triple redundancy	SEU immunity
Analog	Higher voltage	Wide range I/O
	DI process	Fault containment
	BCD process	High power and Precision linear

Using an FPGA to implement the data processing function has several advantages. If there are multiple data paths, it is possible to provide parallel processing of each path allowing multiple data pipelines. If the FPGA is equipped with math blocks that efficiently implement multipliers, these data processors can quickly perform complex arithmetic. The FPGA can also be sized to the application providing only the needed number of logic cells for high utilization.

Table 4: Some FPGA advantages over microprocessor

- Parallel processing
- Complex math using predefined math blocks.
- Number of gates per device scalable to application

Several areas of spacecraft design are well suited for AFE integration. Telemetry is an application where a large number of sensors are monitored for health monitoring or attitude adjustment. The sample rate required can be relatively slow since the changes are gradual; the sensors can be monitored sequentially rather than continuously. A multichannel multiplexer is a common circuit to integrate into an IC. For motor driving applications, typically a power driver is required and position sensing is often used for feedback to control the speed, torque and position. For power control applications, power is switched, sequenced, supervised and adjusted.

Table 5: Applications benefiting from AFE

- Telemetry management
- Motor Control
- Power Control

Sensors can typically be passive or active. Passive sensors require an applied stimulus such as a current to provide a measurable voltage. A four wire technique is typically used for this type of measurement where a current is directed into the sensor to develop a voltage and a voltage measurement is taken across the terminals of the sensor to reduce errors that can occur due to line drops in the higher current path; this is particularly useful when measuring low impedance sensor voltages such as RTDs (resistor temperature detectors). A higher impedance sensor such as a thermistor might tolerate a two wire measurement and still provide sufficient accuracy.

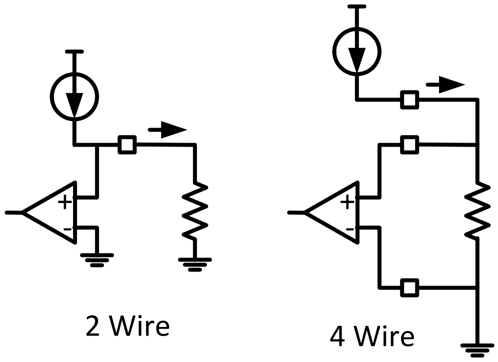

Figure 1: Two and four wire measurements

One method of configuring an AFE is through control registers. Typically a register map defines which bit codes must be written to the control registers to initiate certain commands. Similarly data can be extracted from the AFE using status register reads. For space applications and AFE can be provided with a redundant control interface. In the case of the LX7730, two SPI interfaces are provided.[5]

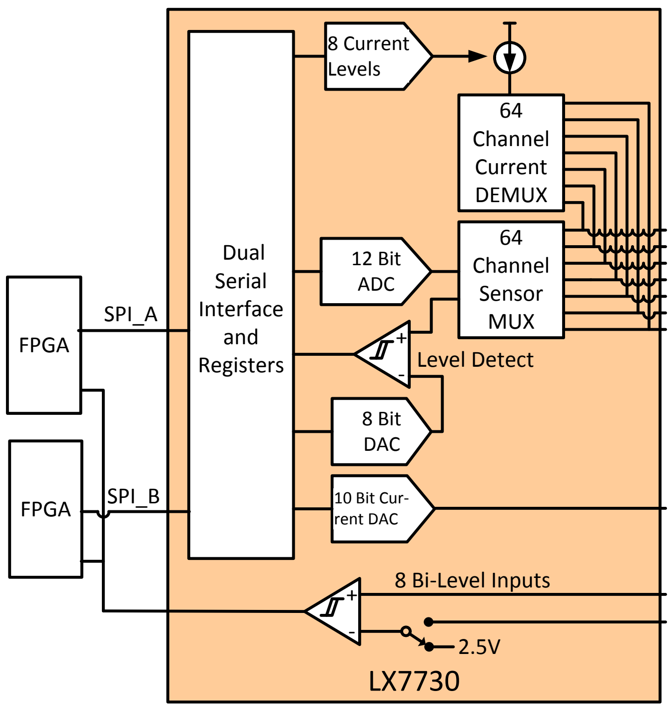

Figure 2: Block diagram of Telemetry AFE

An AFE optimized for telemetry measurements would contain inputs that were configurable for single ended or differential inputs and a current de-multiplexer that can be used to stimulate passive sensors. With the 64 channel multiplexer in Figure 3, the inputs of this device can be configured as any combination of single ended or differential inputs. When using single ended inputs, 8 of the channels can be simultaneously routed to a level detector comparator bank.

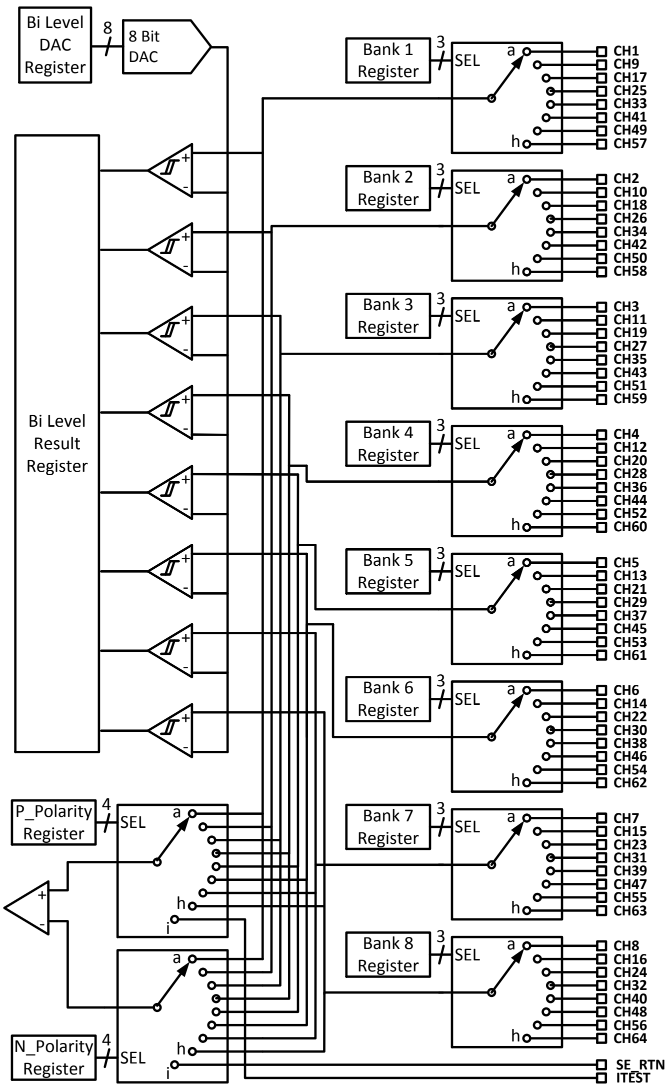

Figure 3: Multifunctional Sensor Multiplexer

The HDL modules being developed to support the LX7730 AFE include:

Table 6: HDL modules for support of telemetry management

- SPI interface
- Parallel interface
- Single register reads and writes
- Data logging routine
- Calibration

An AFE used for motor driving applications requires a high power half bridge configured driver; using external transistor switches allows the driver to be sized to the voltage and current required for the application. An N channel switch typically has a lower resistance than a P channel; an upper N channel transistor driver is floating and receives power via a charge pump or boot strap. Motor coil currents are typically sensed and used as part of the control loop for the motor torque. Sensing motor currents directly at the output of the half bridge on the switch pin gives the most accurate reading for the motor coil current. Unfortunately, since the switch pin moves between the upper rail and ground with the PWM switching action, there is a large common mode signal present at the current sensor resistor terminals. Using several stages of amplifiers and level shifters it is possible to accurately extract this current with integrated circuit techniques. The diagram in figure 4 shows one of four half bridge drivers in the LX7720. [6]

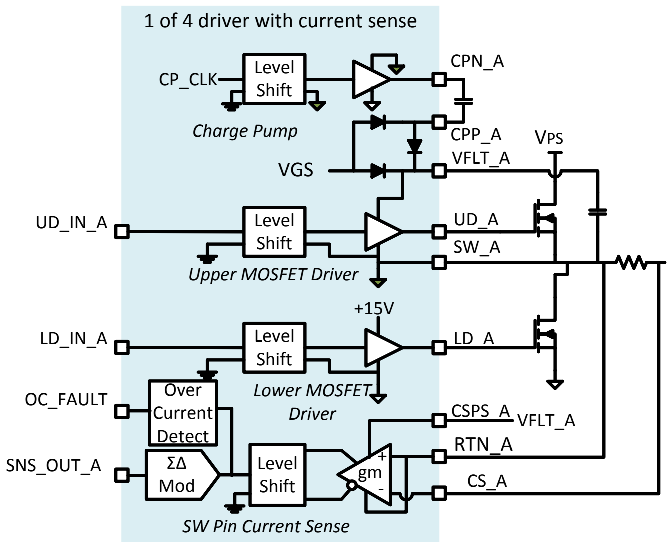

Figure 4: Half bridge power driver with current sense

The output of the current sensor is a ΣΔ modulated ones density data stream that feeds directly into the FPGA. This data has its own dedicated processing pipeline in the FPGA where the sin3 filter and decimator reside. The application can determine the tradeoff between number of bits and the latency limit required by adjusting the decimation rate.

Motor driver applications that use field oriented control require feedback on the position of the motor rotor relative to the stator fields. Resolver transformers coupled to a tracking speed and position algorithm (Resolver-to-Digital) can be used for this. Where motors drive a precision actuator, a linear variable differential transformer (LVDT) is used to sense linear speed and position. These transformer systems require a reference carrier to drive the transformer and a demodulator to extract the sine and cosine angle data from the transformer outputs. A digital processor can implement the tracking conversion but requires a precision ADC input with typically 15 to 16 bit accuracy.

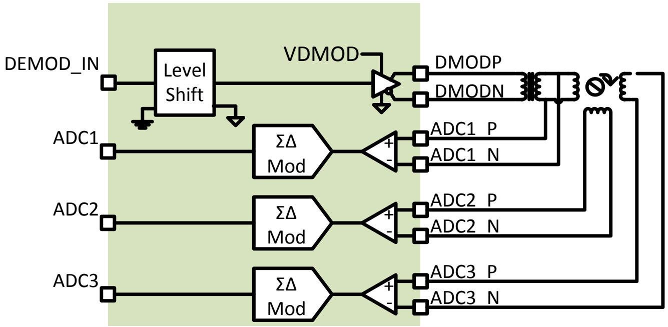

Figure 5: Resolver or LVDT AFE interface

The DEMOD_IN is a pulse stream that is continuously loop read from a lookup table and represents the ΣΔ modulated carrier; the transformer magnetizing inductance provides the filtering to remove the modulation leaving the carrier fundamental. ADC1 monitors the carrier amplitude and ADC2 and ADC3 provide the modulated sine and cosine inputs. These are sigma delta modulated inputs that feed directly into dedicated FPGA processing pipelines.

In some cases an optical encoder or hall sensors are used to provide motor position feedback and the AFE should provide bi-level inputs with adjustable thresholds to sense these inputs and level shift them to FPGA compatible levels.

The complete motor driving system for a brushless DC motor is diagrammed in Figure 6.[7] The blocks that are colored blue are implemented in the FPGA and the blocks that are colored green are implemented in the AFE.

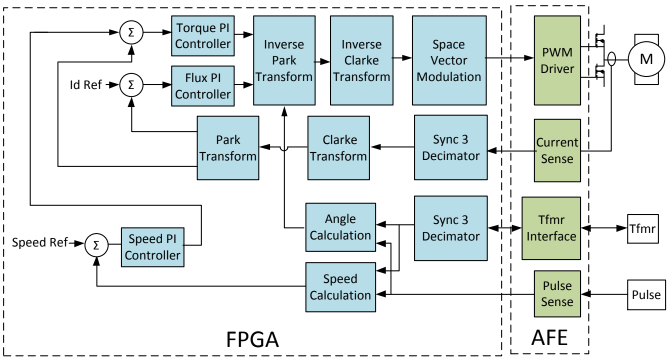

Figure 6: Motor control partitioning

The motor driver AFE is designed to be universal and can also be configured to drive permanent magnet synchronous motors, bipolar stepper motors or unipolar stepper motors. Several VHDL modules are in development to support these applications:

Table 7: HDL modules to support a motor driver system

- 2 phase bipolar drive with microstepping
- Stepper average current regulation
- Sinc 3 filter and decimator w adjustable accuracy
- Pulse exciter for Resolver or LVDT
- Tracking Resolver to digital converter
- BLDC motor with trapezoid drive
- PMSM with sinusoidal drive
- Field oriented transformations
- Space vector modulation
- Fault management

III. Summary

The use of a standard integrated circuit AFE paired with a configurable FPGA takes advantage of high levels of integration. Separation of the analog and digital functions allows IC process optimization for both the implementation of the digital and the analog functions. The application targeted AFE provides a higher level of integration over an implementation of basic single function ICs but avoids the development expense and time associated with developing a fully custom IC. Higher integration reduces parts count which improves reliability and reduces size and weight of the spacecraft electronic modules.

IV. References

All bibliographical references should be numbered and listed at the end of the paper in a section called “REFERENCES”. When referring to a reference in the text, place the corresponding reference number in square brackets [1], [2], [3], etc...

Example:

[1] Vincent Piscane. (2005). Fundamentals of Space Systems 2nd Edition. Text Book: Pages 616-622

[2] Ron Wilson. (2009). Programmable Chips: Piecing Together an Analog Solution. Magazine Article: EDN Network

[3] Sana Rezgui, et al. (2010). SEE Characterization of the New RTAX-DSP Antifuse-Based FPGA, IEEE Transactions on Nuclear Science

[4] NAVSEA SD-18. (2006). Radiation Tolerant Isolation Technology

[5] LX7730, 64 Analog Input Rad Tolerant Telemetry Controller, Datasheet, Microsemi (available on request)

[6] LX7720, Rad Hard Spacecraft Power Driver with Rotation and Position Sensing, Datasheet, Microsemi (available on request)

[7] Microsemi Users Guide (2012). Smart Fusion Field Oriented Control of Permanent Magnet Synchronous Motors Using Hall and Encoder

[8]