



Microsemi Corporation

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Customer Notification No: CN1502

Customer Advisory Notice (CAN) – Action Required

Subject: This Customer Advisory Notice covers two fixes provided in Libero SoC v11.5 SP1 related to SmartFusion devices

- Item - 1: Configuration of unused MSS I/Os
- Item - 2: Change in system selection of eNVM read access from 5:1:1:1 to 6:1:1:1 when the MSS clock is operating at frequencies between 50MHz-80MHz. This is applicable only for A2F060 and A2F200 devices.

Dear Valued Customer,

Item – 1 Configuration of unused MSS I/Os

Description:

Currently unused MSS I/Os on SmartFusion products are not terminated internally. If these I/Os are not terminated externally in hardware, then this may result in a slight increase I/O leakage current not exceeding 2.5mA per unused I/O.

Impact:

Microsemi has determined through thorough analysis and circuit level simulation, that, the leakage per unused I/O is not significant and would remain constant; therefore there is no reliability impact.

Mitigation and Change:

Given the relatively small change in leakage current associated with the unused I/Os no action is required even if these I/Os are not terminated externally. However, if the power consumption budget of the application does not allow such an additional current, Microsemi is releasing a new Libero SoC release, namely v11.5 SP1 to configure unused SmartFusion MSS I/Os to be internally terminated. This setting for the unused I/Os will remove the potential I/O current leakage.

Libero SoC v11.5 SP1 will provide new global options in the device I/O settings section of Libero project for users to configure unused MSS I/Os. Options will include weak pull-up; pull-down and none (default). Notice that this process will not impact the internal timing attributes of customer designs and should be seamless (See below for the step-by-step design update process using this new Libero SoC v11.5 SP1 release).

Customer Action:

Opening Libero SoC 11.5 or older projects in Libero SoC v11.5 SP1

- 1) If user opens Libero SoC v11.5 or older designs, the Resister Pull will be configured as 'none' for the unused MSS I/Os.
- 2) If user would like to change the default state of Resister Pull ('none'), then the user needs to open the Device setting page under Project settings window and select the Resister Pull options as required from the drop down menu.
- 3) If the user has changed the Resister Pull settings from the default 'none' option, then the user needs to:



- a. Regenerate the MSS component and run the entire design flow till programming file generation.
- b. Re-program the device with above generated programming file.

Item – 2 eNVM access Mode Change

Description:

The SmartFusion A2F200 and A2F060 devices may fail to read the eNVM content while the MSS is operating between 50-80MHz. In this frequency range, Libero versions 11.5 and older will configure the eNVM burst read access to be 5:1:1:1 cycles for 4 data words. If the frequency is in the aforementioned range, then, the read data may be corrupted. This is a time zero failure or data corruption, i.e. not a latent failure.

Impact:

Microsemi confirms that there is no reliability concern due to the change in the eNVM read access from 5:1:1:1 to 6:1:1:1.

The change to the default control logic setting, as described below, may have a slight bandwidth implication and it is recommended that customers validate the change on their systems.

Change:

Starting with Libero SoC v11.5 SP1, the MSS configurator will automatically select the eNVM burst read access of 6:1:1:1 cycles when the MSS clock is operating at frequencies between 50MHz and 80MHz. This change is summarized in the table below and the device datasheet.

eNVM Block Timing, Worst Commercial Case Conditions: $T_J = 85^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	A2F060		A2F200		A2F500		Units
		-1	Std.	-1	Std.	-1	Std.	
$t_{FMAXCLKeNVM}$	Maximum frequency for clock for the control logic – 5 cycles (5:1:1:1*)	50	50	50	50	50	50	MHz
$t_{FMAXCLKeNVM}$	Maximum frequency for clock for the control logic – 6 cycles (6:1:1:1*)	100	80	100	80	100	80	MHz

Customer Action:

If existing designs have been tested functionally both at the high end of operating temperature and low end of operating VCC, before deployment, without displaying any eNVM issue then no action is required.

For existing designs that have not been tested as mentioned above or for new designs, Microsemi recommends opening these designs with Libero SoC v11.5 SP1 to create a new programming file and reprogram the A2F060 and A2F200 devices. Please note that this change will not require the design to go through an entire map, place and route iteration. Please review the Release Notes of Libero SoC V11.5 SP1 for more details.

Libero SoC v11.5 SP1 release notes can be downloaded from

http://www.microsemi.com/document-portal/doc_download/134971-libero-soc-v11-5-sp1-release-notes

Contact Information:

For further clarifications or questions, please contact Microsemi's Technical Support at:

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