Libero SoC v11.5 SP1 Release Notes

Libero® System-on-Chip (SoC) is a comprehensive and powerful field programmable gate array (FPGA) design and development software offered by Microsemi®. The Libero SoC software provides start-to-finish design flow guidance and support for novice and experienced users alike. Libero SoC combines Microsemi SoC Products Group tools with such electronic design automation (EDA) powerhouses as Synplify Pro® and ModelSim®.

Libero SoC v11.5 SP1 contains key changes for SmartFusion devices. Read CN 1502 for the key change information.

Libero SoC v11.5 SP1 can be used for designing with Microsemi's SmartFusion2 and SmartFusion SoC FPGAs and IGLOO2, IGLOO, ProASIC3, and Fusion FPGA families.

To access Datasheets and Silicon User Guides, visit www.microsemi.com. Any product can be selected and clicked to go to the **Documents** tab of that particular product. Tutorials, Application Notes, Development Kits and Starter Kits are listed in the **Design Resources** tab of each product.

For more information on new software features and enhancements, refer to the *Libero SoC Online Help*.

Contents

What's New in Libero SoC v11.5 SP1?

SmartFusion eNVM Configuration for the A2F060M3E and A2F200M3F Devices

Libero SoC v11.5 SP1 and later releases automatically select the eNVM control logic cycle of 6:1:1:1 when the MSS clock operates at frequencies above 50 MHz. This change is applicable only for A2F060 and A2F200 devices. This feature is implemented to avoid potential eNVM read failures.

When the designs created in Libero SoC v11.5 or older with MSS frequency in the range of 50 MHz < MSS_CLK <= 80 MHz are opened in Libero SoC v11.5 SP1, the MSS_ENVM_0.efc (Libero manages an internal file that contains the MSS configuration and control logic settings) file is automatically updated by Libero to modify the control logic to select 6 cycles instead of 5 cycles.

The Programming file and the Programming tool states are invalidated in Libero. Designs with MSS clock frequency outside the 50 MHz – 80 MHz range are not affected.

Table 1 lists the new eNVM control logic and MSS frequency relationship.

Parameter	Description	A2F060		A2F200		A2F500		Units
		-1	Std	-1	Std	-1	Std	
$t_{FMAXCLKeNVM}$	Maximum frequency for clock for the control logic –5 cycles (5:1:1:1*)	50	50	50	50	50	50	MHz
$t_{FMAXCLKeNVM}$	Maximum frequency for clock for the control logic –6 cycles (6:1:1:1*)	100	80	100	80	100	100	MHz
*Note: *6:1:1:1 indicates 6 cycles for the first access and 1 each for the next three accesses. *5:1:1:1 indicates 5 cycles for the first access and 1 each for the next three accesses.*								

Opening a SmartFusion Project Created with Libero SoC v11.5 or Older Version

When opening an older SmartFusion project with v11.5 SP1, the user vault must contain either v2.5.106 or v2.2.101 MSS core, whichever is used in the project being opened. If the required MSS core is not present in the vault, the following warning message is displayed.

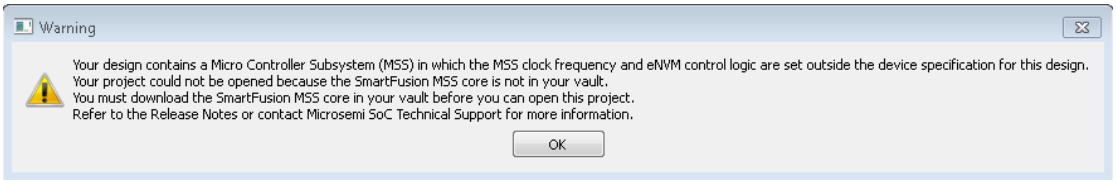

Figure 1 Warning Message

If the above warning message is displayed while opening a design in Libero v11.5 SP1, the MSS core must be downloaded to the user's vault first.

Downloading MSS core in Libero SoC with Internet Connection:

To download MSS core in Libero SoC,

1. Launch the **Libero SoC v11.5 SP1**.
2. Select **View** > **Windows** > **Catalog**. The **Catalog window** is displayed.
3. Right-click **SmartFusion Microcontroller Subsystem** (v2.5.106 or v2.2.101) under **Processors** and click **Download**.

Note: If you have any problem in downloading the SmartFusion MSS core, contact our technical support team at *soc_tech@microsemi.com*.

Observations on successfully opening older designs in Libero SoC v11.5 SP1

1. The following dialog box is displayed upon successful conversion of the design if 50 MHz < MSS_CLK <= 80 MHz.

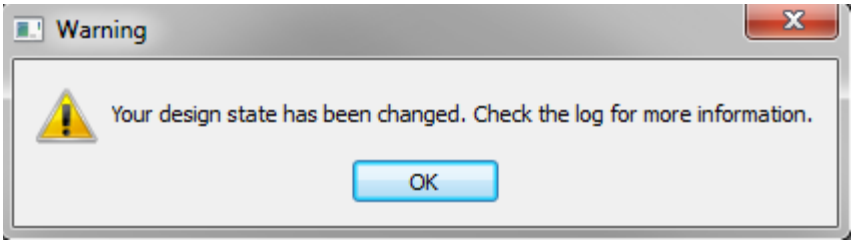

Figure 2 Warning Message

2. Click **OK**. The following warning message is printed to the Libero log window:

   "Your design contains a Micro Controller Subsystem (MSS) in which the MSS clock frequency and eNVM control logic are set outside the device specification for this design.

   Your design is now in a pre-programming state.

   You must re-generate your programming file."

3. The programming file and the programming tool states in Libero SoC v11.5 SP1 are invalidated.

Action Required on Programming File Invalidation

If existing designs have been tested functionally both at the high end of operating temperature and low end of operating VCC before deployment without displaying any eNVM issue, then no action is required.

For existing designs or new designs that have not been tested as mentioned above, Microsemi recommends opening these designs with Libero SoC v11.5 SP1 to create a new programming file and reprogram the A2F060 and A2F200 devices. Note that this change does not require the design to go through an entire map, and place and route iteration.

SmartFusion Unused MSS I/Os Configuration

Prior to Libero v11.5 releases, the unused MSS I/Os are configured with no resistor termination. The default configuration with v11.5 SP1 is the same as with the previous v11.5 releases, no termination.

In Libero SoC v11.5, Microsemi configures the unused SmartFusion MSS I/Os (including military grade devices) to be internally terminated with weak Resistor pull-up. It is done to avoid potential I/O current leakage when the MSS I/Os are not assigned.

Starting with Libero SoC v11.5 SP1, Microsemi provides new global options in the **Device Settings** page of **Libero New Project** window to configure the unused MSS I/O Resistor Pull to weak pull-up, pull-down, and none. The **None** option is configured by default for all the designs.

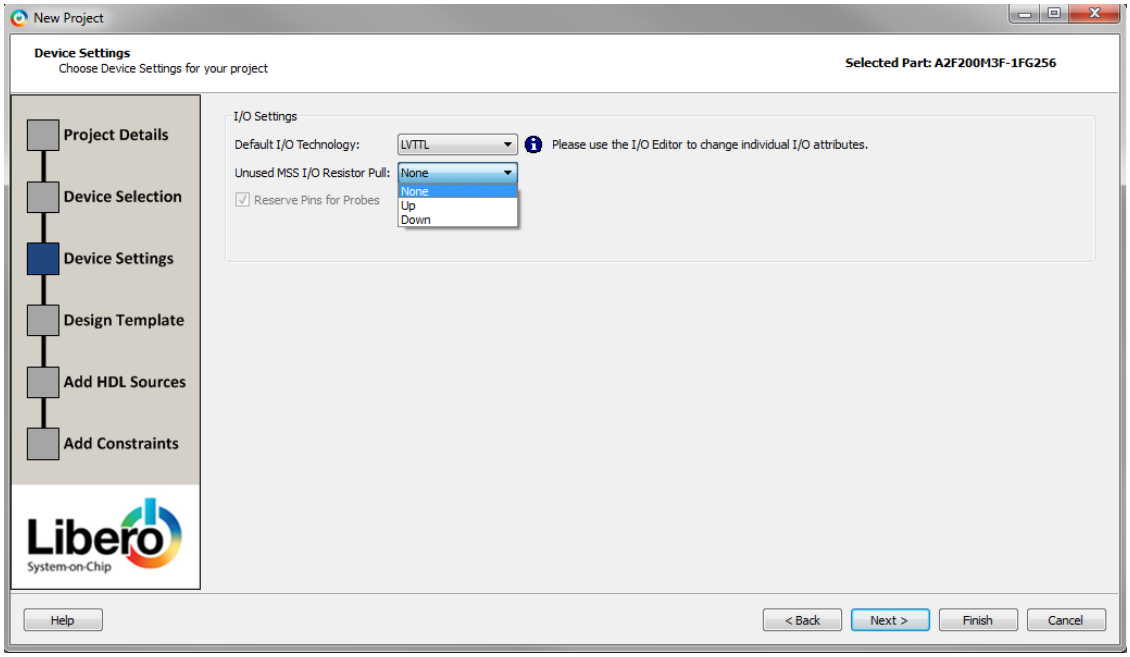

Figure 3 New Project - Device Settings Window

Opening a SmartFusion Project Created with Libero SoC v11.5 or Older Version

In Libero SoC v11.4 SP1 and older software, the Unused MSS I/O Resistor Pull is unassigned for all the design files. In Libero SoC v11.5, the Unused MSS I/O Resistor Pull is configured as weak pull-up.

If the user opens the Libero SoC v11.5 or older project in Libero SoC v11.5 SP1 (assuming that the MSS_CLK frequency is within the new datasheet parameters corresponding to the eNVM control logic speed settings), no invalidation is done. However, if the user regenerates the MSS component, the Resistor pull of the unused MSS I/Os is configured as per the new Unused MSS I/O Resistor Pull setting present in the **Device Settings** page of the **Project Settings** window (see Figure 4). The default setting is **None**. If the user is required to change the Resistor pull of the unused MSS I/Os to either pull-up or pull-down from the default **None**, it can be changed (see Figure 4).

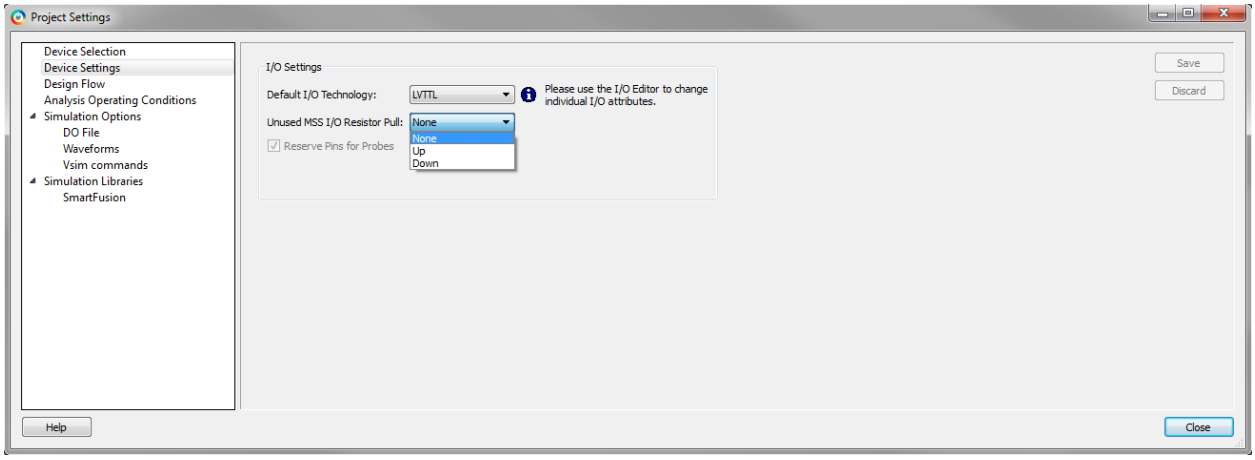

Figure 4 Project Settings Window

Instantiate Multiplexor Basic Block

Multiplexor SmartGen core under basic block can be instantiated for ProASIC3/e, ProASIC3L, ProASIC3 nano, IGLOO/e, IGLOO nano, IGLOO plus, and SmartFusion designs.

Introduced in Libero SoC v11.5

Libero SoC v11.5 is the premier release for the new SmartFusion2 SoC FPGA M2S060 and IGLOO®2 FPGA M2GL060 devices.

Table 2 List of IGLOO2 Devices (New Device Support)

Die	Package	Speed Grade	Temp Ranges	Free Libero Gold
M2GL005	144 TQ	STD, -1	COM, IND	Yes
M2GL005S	144 TQ	STD, -1	COM, IND	No
M2GL010	144 TQ	STD, -1	COM, IND	Yes
M2GL010S	144 TQ	STD, -1	COM, IND	No
M2GL060	676 FBGA	STD, -1	COM, IND	Yes
M2GL060T	676 FBGA	STD, -1	COM, IND	Yes
M2GL060TS	676 FBGA	STD, -1	COM, IND	No
M2GL150	FCV484	STD, -1	COM, IND	No
M2GL150T	FCV484	STD, -1	COM, IND	No
M2GL150TS	FCV484	STD, -1	COM, IND	No

Table 3 List of SmartFusion2 Devices (New Device Support)

Die	Package	Speed Grade	Temp Ranges	Free Libero Gold
M2S005	144 TQ	STD, -1	COM, IND	Yes
M2S005S	144 TQ	STD, -1	COM, IND	No
M2S010	144 TQ	STD, -1	COM, IND	Yes
M2S010S	144 TQ	STD, -1	COM, IND	No
M2S060	676 FBGA	STD, -1	COM, IND	Yes
M2S060T	676 FBGA	STD, -1	COM, IND	Yes
M2S060TS	676 FBGA	STD, -1	COM, IND	No
M2S150	FCV484	STD, -1	COM, IND	No
M2S150T	FCV484	STD, -1	COM, IND	No
M2S150TS	FCV484	STD, -1	COM, IND	No

Production Data

Production (post-silicon) Timing and Power analysis for M2S005/M2GL005

Production (post-silicon) Power analysis for M2S090/M2GL090 and M2S150/M2GL150

Table 4 lists the device and the version of power and timing data for the SmartFusion2 and IGLOO2 devices.

Table 4 Power and Timing Data for SmartFusion2 and IGLOO2 Devices

Device	Power Data	Timing Data
SmartFusion2		
M2S005	Production	Production
M2S010	Production	Production
M2S025	Production	Production
M2S050	Production	Production
M2S060	Advanced	Advanced
M2S090	Production	Advanced
M2S150	Production	Advanced
IGLOO2		
M2GL005	Production	Production
M2GL010	Production	Production
M2GL025	Production	Production
M2GL050	Production	Production
M2GL060	Advanced	Advanced
M2GL090	Production	Advanced
M2GL150	Production	Advanced

Silicon Features

Sub-LVDS Support

A new multi-standard inputs/outputs (MSIO) type is provided for support of sub-LVDS, a reduced voltage form of LVDS.

MSS RTC Clock Source Enhancement

The microcontroller sub-system (MSS) Real Time Counter (RTC) has been updated to add more clock source options. You can now select the main crystal oscillator and specify any mode/frequency supported by this oscillator. The MSS 1.1.300 version must be used to access this enhanced feature.

Device Removal

The following devices have been removed in Libero SoC v11.5:

- M2S100/M2GL100
- M2S/M2GL “S” devices (except all 005S packages, and 010S TQ144 and VQ144)
- 144 VQ devices are replaced with 144 TQ

Software Enhancements

Runtime Improvements

Layout runtime is improved by 2x over the Libero SoC v11.4 SP1 for SmartFusion2 and IGLOO2 designs. System Builder generation runtime is improved by 2x over Libero SoC v11.4 SP1.

Libero UI Enhancements

Changes to Export Functions

All **Export** functions now bring up a User Interface with:

- **Export** parameters, if any
- Location/File Browsing

All **Export** functions have a new 'single' Tool Command Language (TCL) command.

The previous used configure/run **Export** commands are still supported for backward compatibility.

New Project Wizard and Project Settings User Interface

New Project Wizard

Libero SoC v11.5 introduces a **New Project** wizard to facilitate the creation of Libero projects. The new wizard includes the following pages:

- **Project Details Page:** Specifies the project details such as name, location, and description.
- **Device Selection Page:** Specifies the part filters - Family, Die, Package, Speed, Core Voltage, and Range - and/or the Search Part field to search a part in the Part table. Select a part in the table to move to the next page by clicking **Next**. The **Finish** option is enabled from this page onwards on selection of a part.
  Note: The last project settings are used to pre-populate the settings of a new project.
- **Device Settings Page:** The I/O Settings and other family specific device settings such as the 'Power Supplies' settings for Smartfusion2 and IGLOO2 can optionally be selected here.
- **Design Templates and Creators Page:** This enables to start a project by creating a System Builder based design (for the SmartFusion2 and IGLOO2 devices only), or an MSS based design (for the SmartFusion2 and SmartFusion devices only). To use the Standalone Initialization for the microcontroller subsystem double-data rate (MDDR)/Fabric DDR (FDDR)/serializer deserializer (SERDES) peripherals (for SmartFusion2 and IGLOO2 devices only). For other families, these options are disabled.
- **Add HDL Source Files Page:** The Hardware Description Language (HDL)/ electronic design interoperability format (EDIF) files can directly be Imported or Linked into the project.
- **Add Constraint Files Page:** The physical design constraints (.pdc) and timing constraint files (.sdc) can directly be Imported or Linked into the project.

Note: The custom operating ranges cannot be selected when selecting a part. The custom operating temperature, core, and I/O voltage ranges can be selected for the purpose of Timing and Power analysis in the Project Settings **Analysis Operating Conditions** page.

For ProASIC3, IGLOO, Fusion, and SmartFusion families, only the custom operating temperature and core voltage ranges can be selected by opening interactively Designer from within Libero (right click menu on the **Compile tool** in the Design Flow tree)

Project Settings UI

The **Project Settings** dialog has been re-organized and includes the following pages:

- Device Selection
- Device Settings
- Design Flow

- Analysis Operating Conditions: Temperature, Core Voltage, and I/O Voltage Range settings can be changed in this page. Note that Temperature and Core Voltage ranges can only be changed for the SmartFusion2 and IGLOO2 families. For other families (ProASIC3, ProASIC3E, ProASIC3L, IGLOO, IGLOO+, IGLOOE, Fusion, and SmartFusion), these settings are disabled in Libero and can be changed only through the Designer.
- Simulation Options
- Simulation Libraries

Note: The Temperature and Voltage range settings for the purpose of Timing and Power Analysis are now independent from the selected part range for SmartFusion2 and IGLOO2. The Temperature and Voltage range settings for analysis are defaulted to the part range setting on project creation.

Messaging Widget

Libero SoC v11.5 introduces a new **Message** window that is complementary to the existing log window. The new **Message** window provides a better organization of the messages produced during the creation, validation, and implementation of the design. Each message (warning/error/information) has a short description and allows crossing probe, when possible, to the source of the reported issue.

Libero SoC v11.5 supports messaging for the following actions in the design flow:

- SmartDesign generation errors and warnings
- HDL syntax checker
- Bus functional model (BFM) syntax checker
- Synthesis (Synopsys) messages

Messages produced by Compile, Place and Route, Simulation, Timing, and Power Analysis will be added in future releases.

System Builder

AXI Fabric Master Support

Advanced extensible Interface (AXI) Fabric Masters can be added to the following subsystems in the **Peripherals** tab in the **System Builder** wizard (see Figure 5).

- MSS/ high-performance memory subsystem (HPMS) FIC_0 – Fabric Master Subsystem
- MSS/HPMS FIC_1 – Fabric Master Subsystem

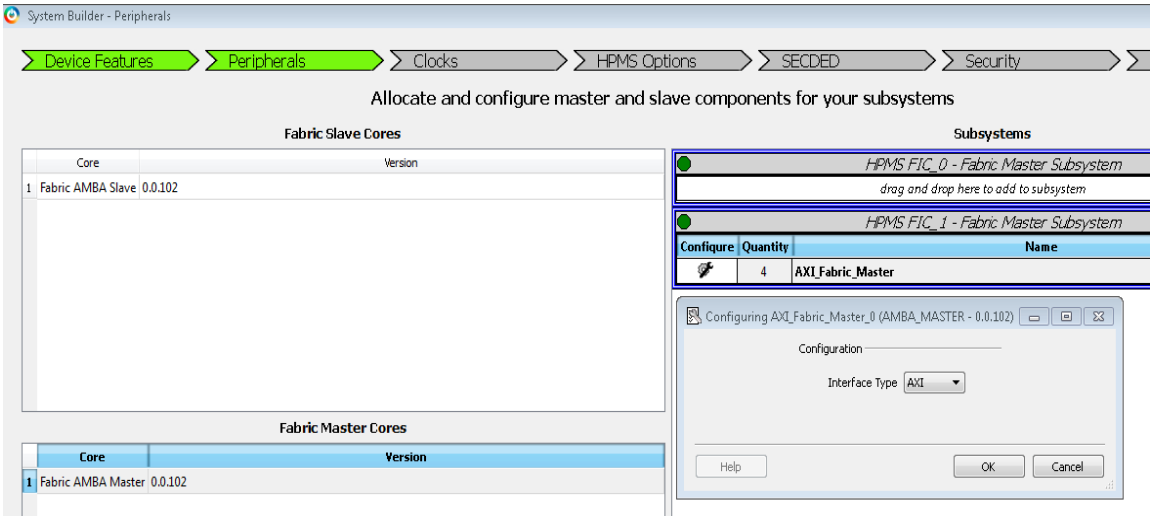

Figure 5 Peripherals Tab in System Builder Wizard

To add a User AXI Fabric Master to one of the above subsystems, drag-and-drop the **Fabric AMBA Master** v0.0.102 core seen in the **Peripherals** tab to the subsystem of interest, as shown in Figure 5. This core must be configured as an AXI Master. After System Builder generation completes, the actual AXI Fabric Master component needs to be connected to the appropriate AXI Master BIF exposed on the System Builder component interface.

By adding an AXI Fabric Master to one of the above subsystems, the entire MSS/HPMS space can be accessed by the AXI Fabric Master. System Builder configures the bus core CoreAXI with the combined region slave slot option such that the MSS/HPMS regions with base addresses 0x00000000, 0x20000000, 0x40000000, and 0x60000000 (to access eSRAM, eNVM, PDMA, HPDMA, and different MSS/HPMS peripherals) are all addressable from AXI Master component. For more information about the memory map computation, refer to the **System Builder Memory Map** tab.

Note: Up to four AXI Fabric Masters can be added to each of these subsystems.

FEED THROUGH Mode for AXI Fabric Master Accessing External DDR Memory

In order to provide better throughput for the design, System Builder configures the CoreAXI bus in bypass mode (FEED THROUGH option) when creating an MSS/HPMS DDR FIC subsystem/ Fabric DDR subsystem in which there is a single AXI master and single AXI slave. This mode is like a wire-wire connection between the master and the slave, and there will be NO restrictions on the addressable space normally imposed by the slave slot size or base addresses.

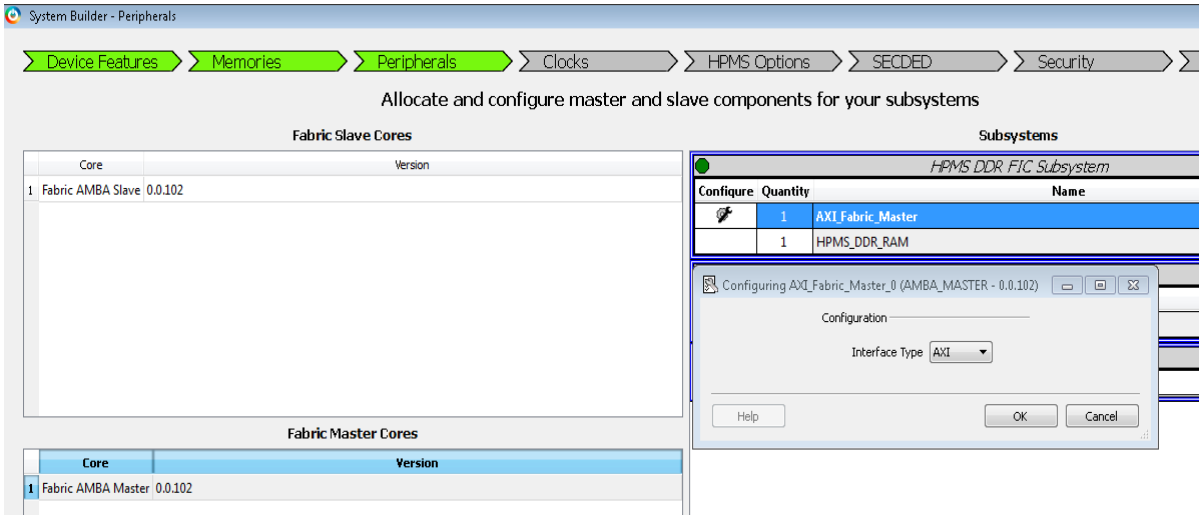

Figure 6 MSS/HPMS DDR FIC Subsystem or Fabric DDR Subsystem Options

Address Space Configuration and Memory Map Computation Bug Fixes.

IGLOO2 System Builder 'Open as SmartDesign...' Feature

As with SmartFusion2, an IGLOO2 System Builder component can now be opened as a SmartDesign to view the internal configuration of the peripherals of the HPMS or the other blocks instantiated and configured by the System Builder.

Right-click on the **System Builder** component in the **Design Hierarchy** window, and choose the option **Open as SmartDesign** to open the **System Builder** component as a regular Smart Design component.

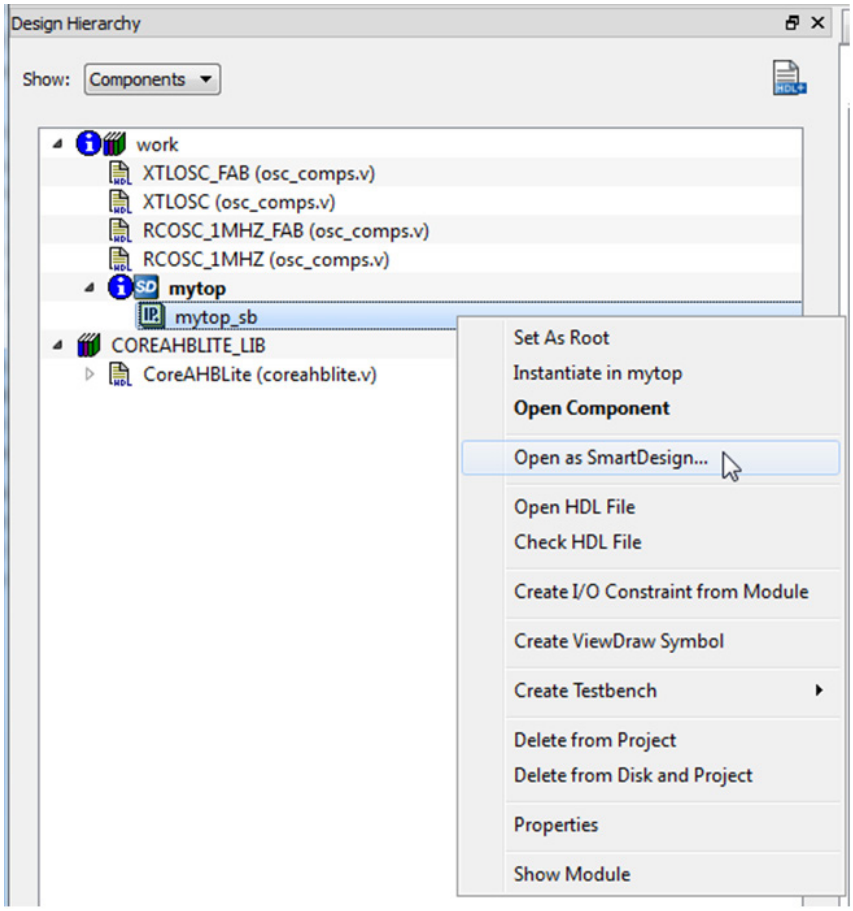

Figure 7 System Builder Component in the Design Hierarchy Window

For more details, refer to the section - “Opening a System Builder Block as SmartDesign” under “Modifying/Inspecting System Builder Design” in the *IGLOO2 System Builder User Guide*.

SmartFusion2 and IGLOO2 Place and Route

Optimization of Global Usage

Better routing assignments of mixed HW/routed topologies (I/O driving Global buffer and Fabric).

SmartFusion2 and IGLOO2 User Managed Flow (non-IDE)

Component Manifest Generation

For each successfully generated SmartDesign component (including the MSS/HPMS and System Builder components), a text file called the component manifest is generated. The component manifest includes the complete list of files generated, their location, and which tools require each file. The manifest file can be found in the component directory <prj>/component/work/<comp_name>/<comp_name>_manifest.txt. It is also available in the report view.

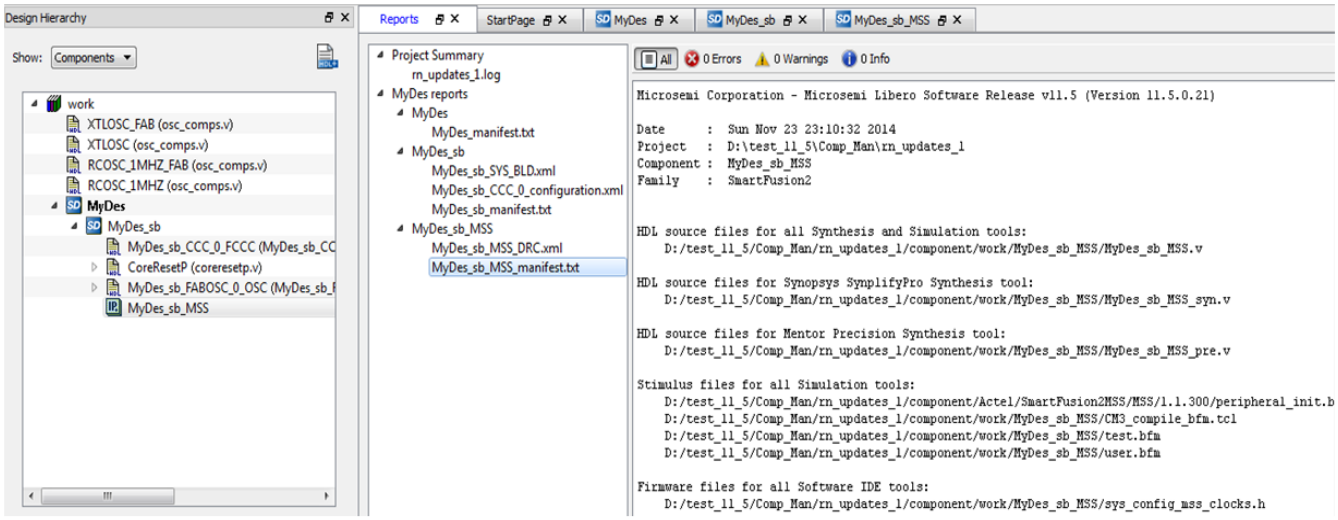

Figure 8 Component Manifest Generation

I/O Advisor

The I/O Advisor enables to balance the timing and power consumption of the I/Os in the design. It offers suggestions on Output Drive and Slew values that meet (or get as close as possible to) the timing requirements and generate the lowest power consumption. Timing data information is obtained from the analysis scenario in SmartTime. Power data is obtained from SmartPower by the specific operating mode (Active mode).

SmartDebug Probe Insertion for SmartFusion2 and IGLOO2

Within SmartDebug, any node (or list of nodes) can be brought in the design to an unused I/O. Libero SoC then runs an incremental route to re-route just those nets with an extra load to an I/O. This feature does not use the built-in probe feature and is invasive to the design. It is done post-Layout from within SmartDebug.

Programming

Export STAPL with Updated IDCODE for ProASIC3 UMC Devices

Export STAPL with updated IDCODE which is now available in FlashPro v11.5. ProASCI3, IGLOO, and RT ProASIC3 devices from UMC require the STAPL file to be generated using the Libero/FlashPro v8.2 or later. Older STAPL files can now be updated without regenerating. Load the older STAPL file and export using File > Export Single device STAPL file.

For more information about STAPL for ProASIC3 FPGAs, refer to *PCN1109*.

FlashPro Express Serialization Programming Support

Production serialization programming support with STAPL files are there for SmartFusion2, IGLOO2, SmartFusion, IGLOO, ProASIC3, Fusion, and RT ProASIC3 families.

Update eNVM Memory Content Enhancements

The **eNVM Memory Update tool** has been enhanced to use the same graphical UI as **MSS eNVM configurator**. Any data storage such as client's address, size, and content can be modified. Serialization clients' data can also be specified (see Figure 9).

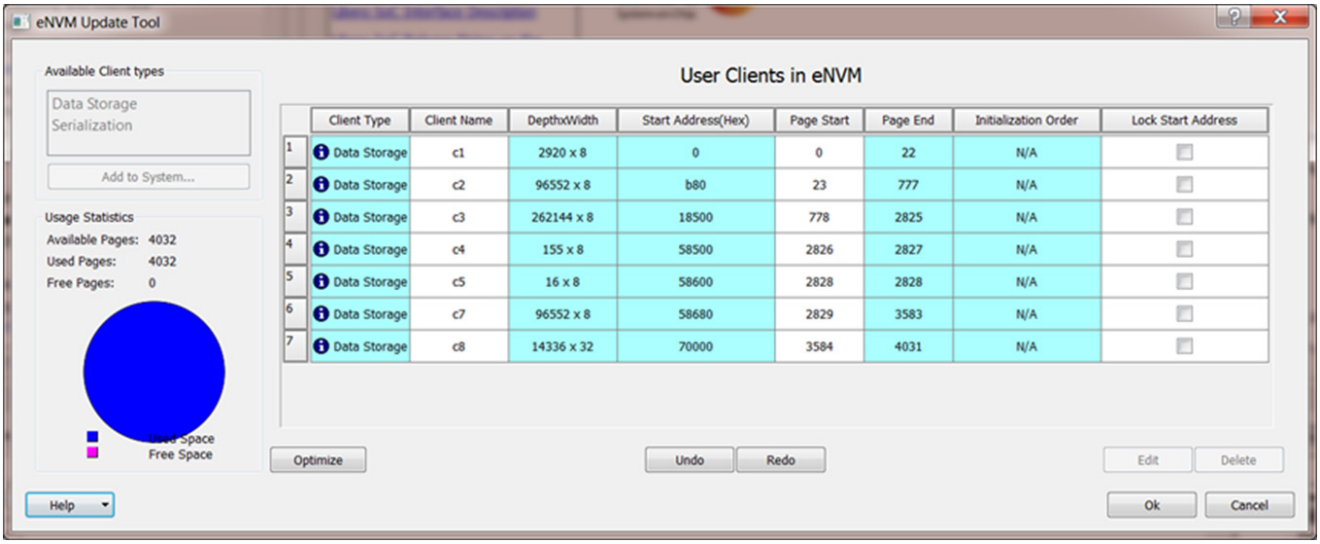

Figure 9 eNVM Update Tool GUI

Note: The client must be modified to disable programming for a client and the **No Content (client is a placeholder and will not be programmed)** option must be selected. The memory file location will be remembered if the client is programmed at a later time.

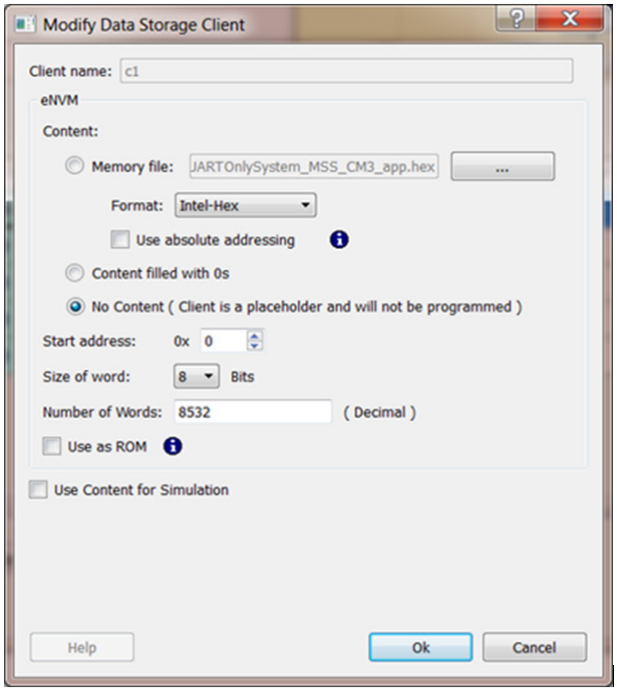

Figure 10 Modify Data Storage Client Window

TCL Support for Chain Configuration and Programmer Settings

Chain Configuration and Programmer Settings can be implemented using TCL commands. For more details, refer to the *Libero SoC Online Help*.

Synthesis Hierarchical Area Report

Synplify Pro ME now supports Hierarchical Area Reporting. This report is found under the Area Summary section of the **Synplify Pro Project Status** tab.

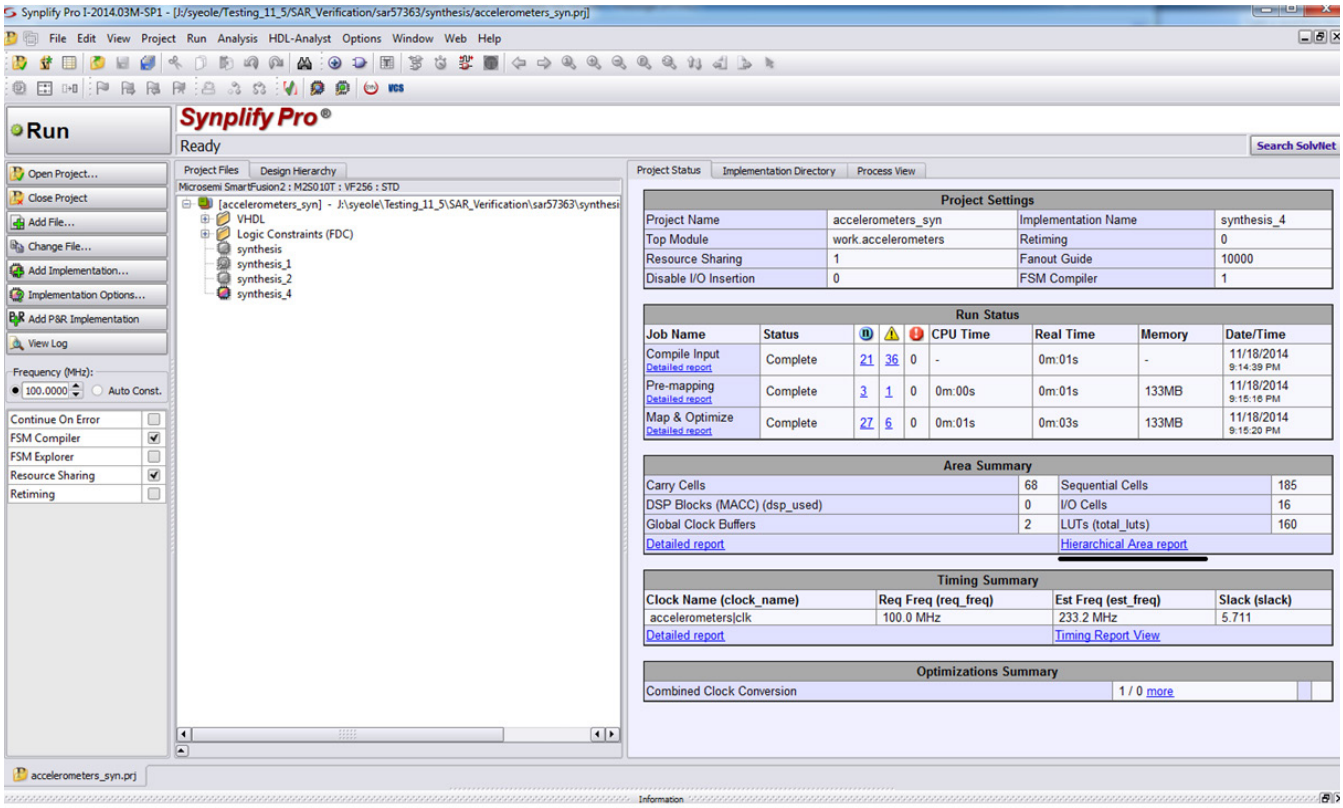

Figure 11 Synplify Pro Project Status Tab

SoftConsole 3.4 SP1

SoftConsole v3.4 requires a service pack to be compatible with Libero SoC v11.5.

Install SoftConsole 3.4 SP1 over SoftConsole 3.4. Use CMSIS version 2.2.101 or later with SoftConsole 3.4 SP1 and Libero SoC v11.5.

Download *SoftConsole 3.4 SP1*.

Updating Design to Libero SoC v11.5

Libero Project Invalidation

Each new update of the Libero SoC design suite includes new features, new device support, and resolved issues. As the Libero SoC design suite is upgraded, it is sometimes necessary to invalidate Libero projects created with previous versions of Libero SoC. Design invalidation means that the current Libero project will not be able to use either a subset or all of the existing data structures of the previous project. This means that the design flow may be reset back to a pre-synthesis state or that portions of the design may need to be regenerated in the case of IP or architectural elements. The decision to invalidate a previous Libero SoC project is not taken lightly and every option to provide a backward compatible solution is always considered. The following sections detail the conditions for project invalidation with Libero SoC v11.5SmartFusion2 and IGLOO2 Project Invalidation Conditions

Discontinued Devices

Some SmartFusion2 and IGLOO2 Data Security devices as listed in Table 5 are discontinued. These devices are not available in Libero SoC v11.5. The design needs to be moved to a different device before upgrading to Libero SoC v11.5. Before moving to Libero SoC v11.5, Libero SoC v11.4 SP1 should be used to port the design to the replacement device. For details, refer to the *CN1419: Availability of SmartFusion2 and IGLOO2 Data Security, "S" Devices*.

Table 5 Discontinued SmartFusion2 and IGLOO2 Data Security Devices

Discontinued				Replacement		
SmartFusion2	M2S010S	256 VF	>	SmartFusion2	M2S010TS	256 VF
SmartFusion2	M2S010S	484 FBGA	>	SmartFusion2	M2S010TS	484 FBGA
SmartFusion2	M2S010S	400 VF	>	SmartFusion2	M2S010TS	400 VF
SmartFusion2	M2S025S	256 VF	>	SmartFusion2	M2S025TS	256 VF
SmartFusion2	M2S025S	325 FCSBGA	>	SmartFusion2	M2S025TS	325 FCSBGA
SmartFusion2	M2S025S	400 VF	>	SmartFusion2	M2S025TS	400 VF
SmartFusion2	M2S025S	484 FBGA	>	SmartFusion2	M2S025TS	484 FBGA
SmartFusion2	M2S050S	325 FCSBGA	>	SmartFusion2	M2S050TS	325 FCSBGA
SmartFusion2	M2S050S	400 VF	>	SmartFusion2	M2S050TS	400 VF
SmartFusion2	M2S050S	484 FBGA	>	SmartFusion2	M2S050TS	484 FBGA
SmartFusion2	M2S050S	896 FBGA	>	SmartFusion2	M2S050TS	896 FBGA
SmartFusion2	M2S090S	325 FCSBGA	>	SmartFusion2	M2S090TS	325 FCSBGA
SmartFusion2	M2S090S	484 FBGA	>	SmartFusion2	M2S090TS	484 FBGA
SmartFusion2	M2S090S	676 FBGA	>	SmartFusion2	M2S090TS	676 FBGA
SmartFusion2	M2S150S	FC1152	>	SmartFusion2	M2S150TS	FC1152
SmartFusion2	M2S150S	FCV484	>	SmartFusion2	M2S150TS	FCV484
SmartFusion2	M2S150S	FCS536	>	SmartFusion2	M2S150TS	FCS536
SmartFusion2	M2S100S	FC1152	>	SmartFusion2	M2S150TS	FC1152
IGLOO2	M2GL010S	256 VF	>	IGLOO2	M2GL010TS	256 VF
IGLOO2	M2GL010S	400 VF	>	IGLOO2	M2GL010TS	400 VF
IGLOO2	M2GL010S	484 FBGA	>	IGLOO2	M2GL010TS	484 FBGA
IGLOO2	M2GL025S	256 VF	>	IGLOO2	M2GL025TS	256 VF
IGLOO2	M2GL025S	325 FCSBGA	>	IGLOO2	M2GL025TS	325 FCSBGA
IGLOO2	M2GL025S	400 VF	>	IGLOO2	M2GL025TS	400 VF
IGLOO2	M2GL025S	484 FBGA	>	IGLOO2	M2GL025TS	484 FBGA
IGLOO2	M2GL050S	325 FCSBGA	>	IGLOO2	M2GL050TS	325 FCSBGA
IGLOO2	M2GL050S	400 VF	>	IGLOO2	M2GL050TS	400 VF
IGLOO2	M2GL050S	484 FBGA	>	IGLOO2	M2GL050TS	484 FBGA
IGLOO2	M2GL050S	896 FBGA	>	IGLOO2	M2GL050TS	896 FBGA
IGLOO2	M2GL090S	325 FCSBGA	>	IGLOO2	M2GL090TS	325 FCSBGA
IGLOO2	M2GL090S	484 FBGA	>	IGLOO2	M2GL090TS	484 FBGA
IGLOO2	M2GL090S	676 FBGA	>	IGLOO2	M2GL090TS	676 FBGA
IGLOO2	M2GL100S	FC1152	>	IGLOO2	M2GL150TS	FC1152
IGLOO2	M2GL150S	FC1152	>	IGLOO2	M2GL150TS	FC1152
IGLOO2	M2GL150S	FCS536	>	IGLOO2	M2GL150TS	FCS536
IGLOO2	M2GL150S	FCV484	>	IGLOO2	M2GL150TS	FCV484

Follow these steps using Libero SoC v11.4 SP1

1. Select the new TS version of the device and package combination a dialog box appears as shown in Figure 12.
2. Click **Yes**.

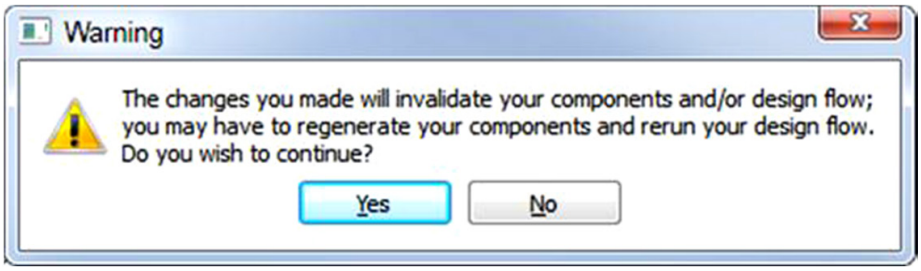

Figure 12 Warning Dialog Box

After clicking **Yes**, all the design flow tools and some of the components will be invalidated. As the warning message above states that some of the components need to regenerated and re-run the design flow tools.

Now, if it is required to run any design flow tool and the design contains one or more components which need to be generated before it can be continued, the following error message will be displayed. If the design has a System Builder component, open the System Builder and regenerate the design.

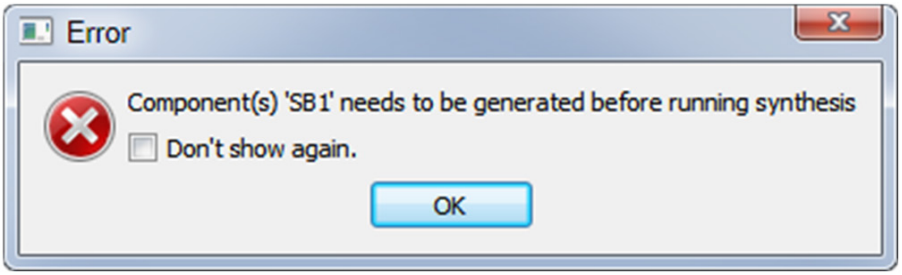

Figure 13 Error Message

3. If the design has any other component that needs to be generated (like MSS), open that component and regenerate the design.

Use Libero SoC v11.4 SP1 to update SmartFusion2 M2S100 and IGLOO2 M2GL100 designs

Table 6 SmartFusion2 M2S100 and IGLOO2 M2GL100 Designs Replaced with M2S150 and M2GL150 Designs

Discontinued				Replacement		
SmartFusion2	M2S100	FC1152	>	SmartFusion2	M2S150	FC1152
SmartFusion2	M2S100S	FC1152	>	SmartFusion2	M2S150TS	FC1152
SmartFusion2	M2S100T	FC1152	>	SmartFusion2	M2S150T	FC1152
SmartFusion2	M2S100TS	FC1152	>	SmartFusion2	M2S150TS	FC1152
IGLOO2	M2GL100	FC1152	>	IGLOO2	M2GL150	FC1152
IGLOO2	M2GL100S	FC1152	>	IGLOO2	M2GL150TS	FC1152
IGLOO2	M2GL100T	FC1152	>	IGLOO2	M2GL150T	FC1152
IGLOO2	M2GL100TS	FC1152	>	IGLOO2	M2GL150TS	FC1152

Use Libero SoC v11.5 to update SmartFusion2 and IGLOO2 144 VQ designs to 144 TQ

Table 7 SmartFusion2 and IGLOO2 144 VQ designs Replaced with 144 TQ

Discontinued				Replacement		
SmartFusion2	M2S005	144 VQ	>	SmartFusion2	M2S005	144 TQ
SmartFusion2	M2S005S	144 VQ	>	SmartFusion2	M2S005S	144 TQ
SmartFusion2	M2S010	144 VQ	>	SmartFusion2	M2S010	144 TQ
SmartFusion2	M2S010S	144 VQ	>	SmartFusion2	M2S010S	144 TQ
IGLOO2	M2GL005	144 VQ	>	IGLOO2	M2GL005	144 TQ
IGLOO2	M2GL005S	144 VQ	>	IGLOO2	M2GL005S	144 TQ
IGLOO2	M2GL010	144 VQ	>	IGLOO2	M2GL010	144 TQ
IGLOO2	M2GL010S	144 VQ	>	IGLOO2	M2GL010S	144 TQ

Resolved Issues

Issues Fixed in v11.5 SP1

SAR 63961 – Fixed eNVM datasheet changes in SmartFusion MSS.

SAR 64085 – SmartGen cannot use the Multiplexor for AGLE3000V5 in Libero SoC v11.5.

SAR 64306 – Fixed unused MSS I/O settings in SmartFusion.

SAR 64935 – Cannot instantiate Multiplexor basic block core in Libero v11.5.

Issues Fixed in v11.5

SAR 62063 – Fixed **Reserve Pins for Probes Feature**

The two live probe I/Os are dual-purpose. If you uncheck **Reserve Pins for Probes** in Libero, these pins should behave as regular I/Os.

However, in Libero SoC v11.4 SP1 and earlier releases, the probe I/Os, if not used by the design, will be programmed as Outputs IOs. As a result, if you try to connect these pins to power nets you may have board contention (Any unused regular I/O must be left unconnected on the board).

To fix this issue in Libero SoC v11.5 or later, you have to run “Place and Route” in Incremental mode and regenerate your programming file.

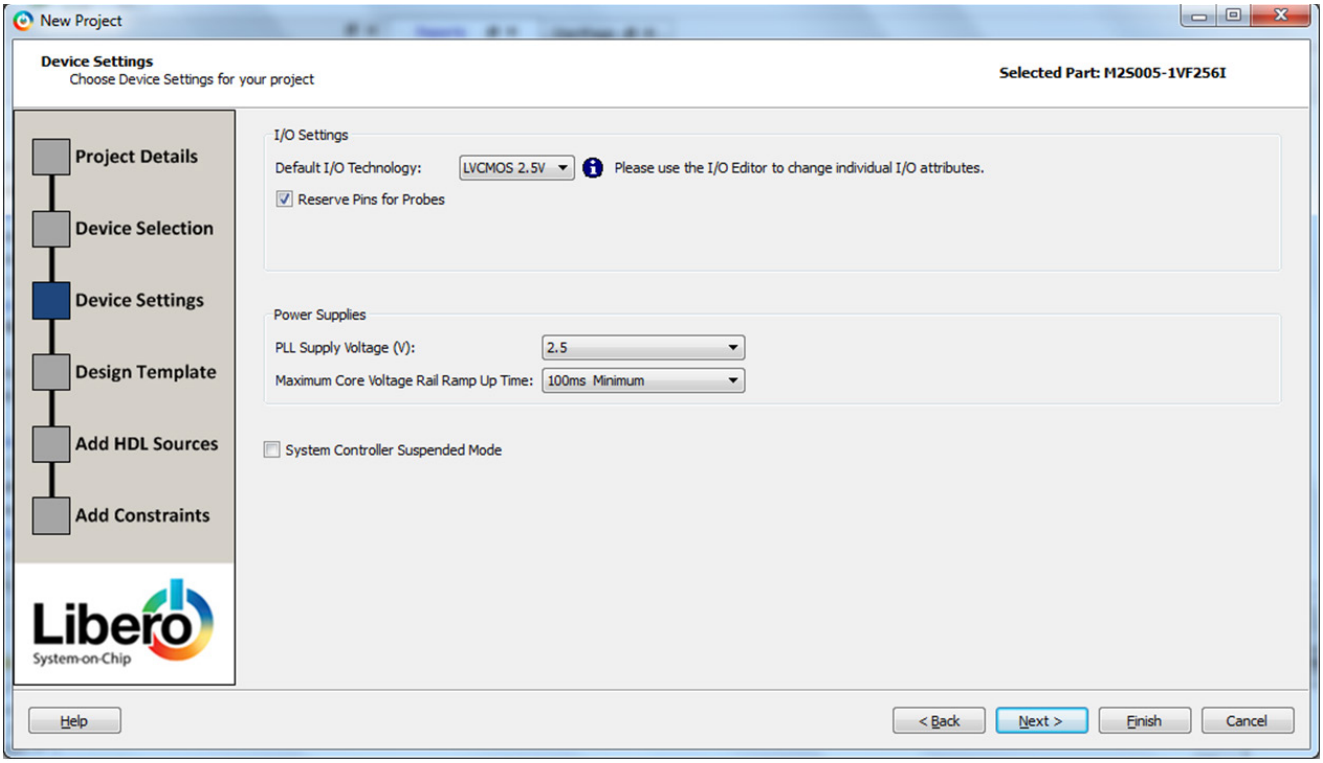

Figure 14 Reserve Pins for Probes Feature

SAR 60565 – Read back eNVM page status for new silicon revisions

New SmartFusion2 and IGLOO2 silicon revisions, as listed below, require using SmartDebug in Libero SoC v11.5 which supports eNVM page status read back.

M2S/M2GL 005 Die Rev 1
M2S/M2GL 010 Die Rev 1
M2S/M2GL 025 Die Rev 1
M2S/M2GL 050 Die Rev 2
M2S/M2GL 060 Die Rev0
M2S/M2GL 090 Die Rev0
M2S/M2GL 150 Die Rev0

SAR 59184 – SmartFusion MSS resets when SmartDebug is opened.
JTAG reset is disabled inside the SmartDebug GUI session by default. Power-cycling, resetting device or accessing JTAG port from any other tool will invalidate SmartDebug GUI session.

SAR 60230 – When moving a project from Libero SoC v11.3 to 11.4 with SERDES, Replace Instance results in an invalid configuration of the design after Generation

SAR 60102 – PCIe BAR2 and BAR3 settings incorrect with SERDESIF version 1.2.102

SAR 60089 – MSS Timing Data is optimistic

SAR 59212 – Export Design Summary sometimes results in an empty html file => 0 KB

SAR 43772 – Linux: The SmartFusion2 configurators for DDR and FICs are missing the diagram describing the details of the block

SAR 59407 – VHDL synthesis and simulation issues when multiple Fabric AMBA AXI slaves are added to a FIC subsystem.

SAR 41069 – Add PDB loading from DDF for Libero environment

SAR 55543 – The *.so has *.edf option for synthesis_1/2 implementation through Libero

SAR 59220 – Export Bitstream, Export Programming Job and Generate Bitstream will fail if DPK is not entered in the Security Policy Manager

SAR 59218 – Debug policy shouldn't require DPK to be set if only digest check option is selected.

Customer Reported SARs Fixed in Libero v11.5

Refer to the Technical Support Hotline Case Number to determine if the SAR has been fixed in this release. The case number and SAR are listed in Table 8.

Table 8 The Case Numbers and SARs

SAR	Case Number	Product	Summary
24961	1-39887569	Project Manager	Importing .vh header files.
29616	489394-310988253	Enhancement	HDL extensions to be supported (.vhdl, .sc).
44552	493642-1213326815	Project Manager	There is no TCL command that allows all files of a design to be removed.
48245	493642-1338645805	FlashPro	Program_NVM action is not given in the advanced features.
50624	493642-1442993788	FlashPro	Security issue with SVF programming file.
62663	493642-1467541775	STAPL	Need to Export STAPL with updated IDCODE for ProASIC3 UMC devices
52560	493642-1507553340	Project Manager	No option to import Verilog/VHDL netlists.
52835	493642-1511595850	Project Manager	Issue while creating core from HDL.
61361	493642-1533328502	STAPL	Change default ERASE/PROGRAM action to Disable Fabric Quickly via RLOCK prog.
61203	493642-1533328502	STAPL	Add encrypted PA3 STAPL action to Disable Fabric Quickly via RLOCK Prog.
54095	493642-1533328502	STAPL	Add PA3 STAPL Action to Disable Fabric Quickly (via RLOCK Prog).
36598	493642-1555946063	FlashPro	Need to change the names in [Strings] section of .INF file.
54197	493642-1560992401	Synplify Pro ME	syn_preserve not preserving others clause.
54798	493642-1570889103	Synplify Pro ME	Internal Error in m_proasic.exe.
54943	493642-1576701973	System Builder	Open System Builder as SmartDesign for IGLOO2.
56583	493642-1586311562	MSS Configuration	MSS Configurator - HTRANS signal.
55948	493642-1602133594	SmartDesign	"<>_hw_platform" shows the wrong block name.
60814	493642-1602265092	Verilog Lib	PCIe BFM byte read looks different than hardware.
56040	493642-1602756582	SmartDesign	Memory map not generated in the data sheet for the APB slave.
56043	493642-1603314030	Installation	Wrong path of Identify Debugger in Tool Profile.
56815	493642-1613798767	IBIS	Incorrect VMEAS level in IBIS models.
56926	493642-1622854612	IBIS	Generate IBIS with separate input and output model.
57006	493642-1624432244	Project Manager	Ramp Rate labelling.
57005	493642-1625178848	Designer	Out of data EDN file warning after Layout.
57680	493642-1626930271	SmartDesign	Blank datasheet.
57446	493642-1627561290	Project Manager	Error: "The right value cannot be equal to the left value if no dependency is set".
57563	493642-1641747338	FlashPro Express	Provide GUI option to disable Core check during scan chain.
57924	493642-1645046087	Project Manager	Verilog file Parsing bug.
56290	493642-1651231793	FlashPro	Log the digest values in programming log and serialization log.
59381	493642-1652945173	ModelSim ME	CCC simulation timing issue. Rounding issue in the PLL VCO inside ModelSim.
58879	493642-1655249065	BFM (Simulation)	SERDES AXI slave issue with 64-bit bursts longer than 10.

SAR	Case Number	Product	Summary
58650	493642-1657127624	Project Manager	Automatic generated .do file broken.
58895	493642-1661049099	MSS Configuration	RTC crystal frequency fixed at 32 kHz.
58779	493642-1661928381	Synplify Pro	No Block RAMs inferred
58697	493642-1662534406	IBIS	ERROR:unknown model= Model not found: LVCMOS25:OUT_DRIVE:0110:SLEW:00
58845	493642-1663046516	Project Manager	VHDL 2008 support in Libero.
59009	493642-1667874630	Project Manager	Automation of EDIF to HDL netlist conversion feature in Libero.
59285	493642-1668148912	Project Manager	When updating temp grade for device, user must go through design flow.
59364	493642-1673389018	Project Manager	Issue in exported TCL file from Libero SoC.
59468	493642-1677542773	Project Manager	Highlight placer warning/error messages in Libero GUI log window.
36598	493642-1688013883	FlashPro	Need to change the names in [Strings] section of .INF file.
59794	493642-1689579593	HDL	vhdl2008 constructs show error in v11.4
59786	493642-1691015991	BFM (Simulation)	PCIe BFM simulation issue. Rounding issue in the PLL VCO inside ModelSim.
60395	493642-1693139310	Synplify Pro ME	LSRAM for x36/x32 configuration - *_WEN should be static.
60029	493642-1697999155	Synplify Pro ME	Error Code [nlverify.c:5742 Found functional mismatch inside module SV_Compute_0].
60096	493642-1701899271	Installation	Unable to start Designer in Libero V11.4.
60107	493642-1703893901	BFM (Simulation)	Async Clocks between MSS and fabric. Rounding issue in the PLL VCO.
60794	493642-1707018161	Synplify Pro ME	Floating signal found with latest Synplify Pro ME release compare to older release.
60379	493642-1713612459	Synplify Pro ME	Unspecified package "VF256" in M2GL005 device.
62146	493642-1713863157	SmartPower	Best and worst case voltage are swapped in custom mode.
56815	493642-1719014042	IBIS	Incorrect VMEAS level in IBIS models.
61293	493642-1721214029	IO Editor	Suspect I/Os default configuration is incorrect for the unused MSS I/Os.
61056	493642-1722670821	Verilog Lib	Improve the SRAM warning related to clocks synchronization in the write x36 mode.
60761	493642-1724305399	Synplify Pro ME	Add VF256 package in synthesis tool.
60892	493642-1725864350	Synplify Pro	Synplify fails to detect changes in Verilog files
61762	493642-1739017018	Project Manager	In Libero 11.4 while exporting firmware if no IDE is selected CMSIS for IAR is generated by default.
61752	493642-1741562910	License	v11.4SP1 does not check out USB Dongle license
61752	493642-1746730855	License	v11.4SP1 does not check out USB Dongle license
62227	493642-1748741660	Timing	Hold time problem IGLOO static timing analysis.
61752	493642-1754262403	License	v11.4SP1 does not check out USB Dongle license
61752	493642-1758204191	License	v11.4SP1 does not check out USB Dongle license
36598	493642-615983223	FlashPro	Need to change the names in [Strings] section of .INF file.

Known Limitations, Issues, and Workarounds

Libero SoC v11.5 SP1 Users

SmartFusion

SAR 64650 - Warning message is displayed while generating the MSS component after migrating to Libero SoC v11.5 SP1.

In the designs with 50 MHz < MSS_CLK<= 80 MHz, if MSS is generated for the first time after migrating to Libero SoC v11.5 SP1, the following message is displayed in the log window.

Warning: Unable to access the file

'<Project Directory>\component\work\sf_200_208_80_MSS\MSS_ENVM_0\MSS_ENVM_0.efc'.

Please check that the core file 'sf_200_208_80_MSS.cxf' is valid; you may need to regenerate this core.

It does not affect the design and can be ignored.

Libero SoC v11.5 Users

Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines the **InstallShield** Wizard displays a message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click **Yes** and the installation will complete successfully.

Antivirus Software Interaction

Many antivirus and Host-based Intrusion Prevention System (HIPS) tools flag executable and prevent them from running. To eliminate this problem, the security setting must be modified by adding exceptions for specific executable. This is configured in the antivirus tool. Contact the tool provider if any assistance is required.

Many users are running Libero successfully with no modification to their antivirus software. We are aware of issues when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version and security settings all contribute to the end result. Depending on the environment, the operation of Libero, ModelSim ME and/or Synplify Pro ME may or may not be affected.

SmartFusion2 and IGLOO2

SAR 46571 – M2S050 has only one Oscillator

When you instantiate the Oscillator in your design and also use MSS RTC, the Clock Source of the RTC must match the clock source used in the Oscillator. For example, configuring the RTC with Clock Source set to 32 KHz RTC Crystal Oscillator while the Oscillator block is configured with the External Main Crystal Oscillator set to 5 MHz is invalid. The frequencies must match.

MIL Temp Removed from 400 VF, 676 FBGA and 896 FBGA Packages

Military Temperature for all SmartFusion2 and IGLOO2 packages was introduced in V11.2. Subsequently, we decided to offer MIL Temp only for 484 FBGA and 1152 FC packages.

If you started a design using Libero SoC v11.2 and selected MIL Temp for any 400 VF, 676 FBGA or 896 FBGA packages, when you open the project in Libero SoC v11.3 or later the software will crash. Please contact soc_tech@microsemi.com for instructions on how to modify your project so that it can be opened in the current release.

For IGLOO2 projects use System Builder for the following cores; do not use these cores from the Catalog directly.

- DDR Memory Controller
- CoreConfigP
- CoreResetP
- CoreConfigMaster

SAR 58852 – Back-annotated netlist created using a previous release will be invalidated when the project is opened in Libero SoC v11.5. MSS and SERDES timing has been updated in the simulation models necessitating invalidation of the back-annotated netlist.

Libero

When a Pre-Libero SoC v11.3 project using EDIF netlist flow is changed to Verilog netlist flow, the project will be invalidated post-synthesis.

SAR 62697 – (Linux Only) - Libero does not refresh the screen or handle clipboard requests while a configurator is open. Unable to copy the content in Libero and paste it in CoreABC (or any core) when a configurator is open.

Workaround:

1. Outside Libero, navigate to the location on disc where the source file exists.
2. Open the source file in a text editor and copy the text.
3. Go back to Libero, open the core and paste the content in the core.

SAR 58638 – CoreAXI v3.0.112 is dropping the BIF connection

Using the **Replace Instance Version...** feature with the latest release of CoreAXI results in error messages in the log window. CoreAXI v3.0.112 has new features and the port and parameter lists are not identical to the older versions. This results in errors during the "Replace..." command.

Workaround: Manually open the newly replaced CoreAXI configurator and double check that your settings are as you expect.

SAR 54877 – Block design cannot be used with Verilog flow.

Synplify Pro ME does not write the definition of the blocks in the .vm file. You have to pass them manually to the compile tool.

You can do that from “Organize Input Files -> Organize Source Files” from the right click menu on the tool. The file you need to pass is the *_syn.v files from the blocks (under <project>/designer/<blkname>*_blk/)

SAR 51880 – Project Archiving tool states are not retained when a Libero Project is uploaded on SVN

Workaround: Zip the project and upload to SVN in order to retain the tool states.

SAR 50267 – Selecting SMEV RAM available in Fusion’s Advanced Analog System Options dialog degrades the Resolution performance

In the datasheet we state a resolution of 1/0.25 Deg while using ADC in 10/12 bit mode. When using SMEV RAM we have observed a resolution of 3-4 Deg. in some cases.

SAR 49569 – Libero does not support importing an FDC file. To add constraints for Compile Point, you must open Synplify Pro to add them.

SAR 47957 – SmartFusion2/IGLOO2 RAM Initialization Configurator – Importing Simple-Hex and Motorola-Hex files is not working

When you try to import Simple-Hex or Motorola-Hex files for initialization for simulation, Libero may crash or the import may fail (content initialized to all zeroes).

Workaround: There is a workaround available that utilizes a *.shx file generated for Fusion. Contact Microsemi Technical Support at soc_tech@microsemi.com for details. Ask for the workaround for SAR 47957.

SAR 46161 – The post-synthesis EDN file will not appear in the design hierarchy until the project is closed and reopened.

SAR 42170 – MVN Cross probing is not supported for Path List and Expanded Path View of the Min and Max Analysis windows

This issue will be fixed in a future release.

SAR 41619 – IGLOO+ hot-swappable option is not displayed correctly in the GUI

Hot-swappable is always ON for IGLOO+ and cannot be changed. The GUI allows you to check/uncheck this feature, but it is ignored by the tools. These I/Os are always hot swappable.

SAR 57617 – Automated meta.out file creation is missing scenarios

The automated mapping file for VHDL, meta.out, generated by Libero does not take into account the following VHDL syntax:

- Packages defined in other libraries apart from work.
- Constants declared in package or in the generic map of the entity
- Unbounded Array specified in the package
- Integers with negative range
- Usage of IEEE NUMERIC_STD package

Workaround: For the above scenarios, the VHDL mapping file (meta.out in the hdl folder) needs to be updated based on the meta.out file format rules mentioned in the Libero online help. If using numeric_std package, the following lines should be included:

```
usedpackages numeric_std
end
```

SAR 62922 – MDDR/FDDR configured for LPDDR with LVCMOS18 is still using ODT

When the MDDR/FDDR is configured for LPDDR using the LVCMOS18 buffers ODT is expected to be disabled. In releases prior to and including Libero SoC v11.5 the ODT is enabled causing an increase in power on the VDDIx 1.8V supply. This will be fixed in a future release.

Workaround: Contact soc_tech@microsemi.com.

Termination of Unused I/Os for MSS in SmartFusion

For New Design: *Libero SoC v11.5 automatically configures each unused MSS I/O as a weak pull-up to avoid I/O current leakage.*

For Existing Design: *Existing user needs to re-generate the MSS component and re-run the design implementation that configures each unused MSS I/O as a weak pull-up.*

System Builder

SAR 62676 – IGLOO2: "Info: 'Fix Vlnv Instance' failed because the instance USB is not enabled."

When an IGLOO2 System Builder design is generated, you will see the following message in the log window:

```
"Info: 'Fix Vlnv Instance' failed because the instance 'USB' is not enabled."
```

It doesn't affect your design and can be ignored.

SmartTime

SAR 57161 – Automatic hold violation fixing is currently not supported for SmartFusion2 and IGLOO2.

SAR 34365 – Asynchronous Register paths are not displayed in Timing Analysis view.

This issue will be fixed in a future release.

SAR 43767 – Maximize Window button is missing from the title bar for Constraints Editor, Max Analysis and Min Analysis

Workaround: Double-click the title bar to maximize the window.

SAR 43726 – The exported Tcl file does not include commands to organize SDC files.

Workaround: Requires editing the exported TCL file carefully. This issue will be fixed in a future release.

Programming

SAR 63118 – The following message may appear during programming operations with FlashPro5 programmers: "Please check programmer setup", which will prevent the user from programming.

Workaround: Disconnect and re-connect the FP5 programmer from the USB port connected to the computer.

SAR 62608 – FlashPro5 programming time is longer than FlashPro4

FlashPro5 programming time may be significantly longer for large devices vs. FlashPro4. For example, M2S090 programming takes 30 seconds more when using FlashPro5 than with FlashPro4.

SAR 62640 – No error is provided in the Update eNVM Memory Content tool when the maximum number of devices to program for serialization clients is set to 0.

SAR 62337 – Export bitstream tool fails when network paths are used.

Workaround: Map the network drive prior to exporting bitstream files.

SAR 62057 – SmartFusion2/IGLOO2 Programming action “Help link” in Libero Messages/Errors window links to ProASIC3 Help.

SAR 58063 – For SmartFusion2 and IGLOO2, optional procedures for a programming action configured in Libero are not exported in the Programming Job.

Workaround: Open the programming job project in FlashPro to configure and save this setting.

FlashPro5 is not supported for RHEL 5 and CentOS 5.

SVF for SmartFusion2 and IGLOO2 will be available in a future release.

SAR 51767 – Error: The command 'load_programming_data' failed.

During programming file generation if the serialization content files cannot be found, then you will see the following error: "Error: The command 'load_programming_data' failed.”

Workaround: Open **Update eNVM Memory Content** and specify a valid path for each serialization content file.

SAR 45867 – STAPL player for SmartFusion2 or IGLOO2 will be available in a future release.

SAR 47452 – FlashPro verify and erase errors are reported as programming failures.

If you run programming ACTION VERIFY/ERASE and there is a failure, then the error code will indicate it is a programming failure even though you were running action VERIFY/ERASE.

SmartDebug

SAR 54004 – Search in Debug FPGA GUI does not support wild card. This will be supported in a future release.

SmartDebug SERDES is not supported for M2S050PP and ES parts.

SAR 63803 – Using the assigned pin for Probe Insertion is not supported for SmartFusion2 and IGLOO2.

The used I/Os in the design cannot be assigned to debug using Probe Insertion.

Synopsys Synplify Pro

SAR 55447 – Compiler Error <btextio.c:1228 NIL file pointer: Cannot write to file. Please check write permissions>. This issue is under investigation.

Workaround**:** Remove the synplifypro_ini file from AppData/Roaming and re-run synthesis.

SAR 46982 – Synplify Pro treats the PLL as a black box

SDC constraints applied to the PLL input do not propagate forward. To actively constrain it; you must constrain both the input and the output of the PLL using the create_clock and create_generated_clock constraints. More information can be found in KI70291.

SAR 46983 – False Path, Multicycle Path and Max delay constraints are not propagated to the SDC file used by Synplify Pro

For more information about constraints consult Chapter 4, Specifying Constraints, in the Synplify Pro User Guide.

Synplify Pro Warning: Unrecognized technology/part/package in Synplify Pro

When executing synthesis using the Libero integrated flow a warning appears if the silicon family, die or package is not present in Synplify Pro. In most cases the design will automatically be mapped to an existing device and continue. If no mapping exists the flow will halt.

Missing Die

```
Unrecognized part [die] specified for device [silicon_family] in
[design_name]:synthesis
```

Design will be mapped to a pre-programmed default and synthesis will proceed.

Missing Package

```
Unrecognized package [package_name] specified for part [die] in
[design_name]:synthesis
```

Design will be mapped to a pre-programmed default and synthesis will proceed.

Missing Silicon Family

```
Warning: Unrecognized technology: [silicon_family]
```

```
Unrecognized technology: [silicon_family] in [design_name]:synthesis
```

Synplify Pro halts.

System Requirements

Refer to *System Requirements* on the web for more information regarding operating systems support and minimum system requirements. 64-bit OS is required for designing SmartFusion2 and IGLOO2 devices.

Setup Instructions for Linux OS can be found on the *Libero SoC Documents* webpage.

Changes in OS support

Supported

Windows 7, Windows 8.1

RHEL 5* and RHEL 6, CentOS 5* and CentOS 6

** RHEL 5 and CentOS 5 do not support programming using FlashPro5*

Discontinued

32-bit operating systems are no longer supported.

Windows XP is no longer supported.

Synopsys and Mentor Graphics Tools

These tools are included with the Libero SoC v11.5 installation.

Synplify Pro ME 2014.03M SP1 Release Notes

ModelSim ME 10.3c Release Notes

Identify ME 2014.09M-1 Release Notes *- Identify ME for Linux will be released in early 2015*

Synphony Model Compiler 2014.09M Release Notes

Prerequisite Software: In order to run Synphony Model Compiler ME, you must have *MATLAB/Simulink* by MathWorks installed with a current license. You cannot run Synphony Model Compiler ME without MATLAB/Simulink.

Download Libero SoC v11.5 SP1

Installation requires Admin privileges.

- Windows
- Linux

Libero SoC v11.5 SP1 is an incremental service pack and must be installed over Libero SoC v11.5.

Download Libero SoC v11.5

Installation requires Admin privileges.

- Windows
- Linux

SoftConsole v3.4 SP1 should be installed over SoftConsole v3.4 for use with Libero SoC v11.5

SoftConsole 3.4 SP1

SoftConsole v3.4 requires a service pack to be compatible with Libero SoC v11.5

Download *SoftConsole 3.4 SP1*

List of Changes

The following table lists critical changes that were made in each revision of the document.

Date	Change	Page
March 2015	Updated the release notes for Libero SoC v11.5 SP1 changes.	NA
January 2015	Initial release.	NA

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650. 318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

For Microsemi SoC Products Support, visit http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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