UG0609
User Guide
Stepper Theta Generation v4.1

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Power Matters.™

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- Added the IP version to the document title.
- Removed Configuration Parameter section from Hardware Implementation, page 4.

1.2 Revision 2.0

Updated Table 1, page 4 and Table 2, page 6 (SAR 71204).

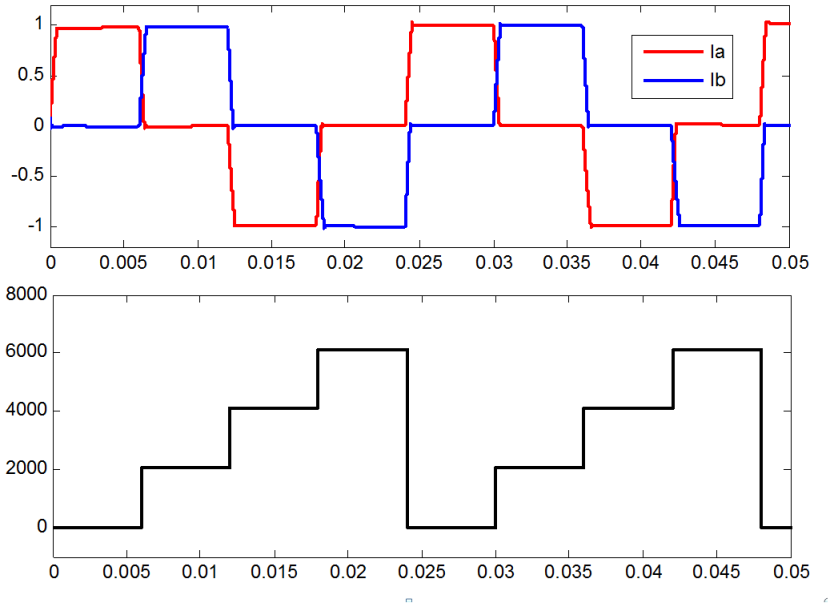
1.3 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Introduction

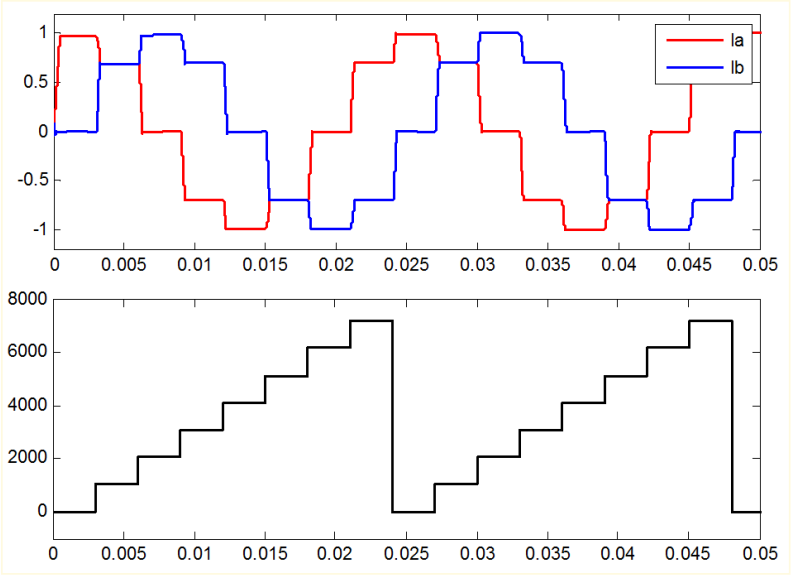
The stepper motor is used for position control by moving through a certain number of steps. While a stepper motor has a fixed number of steps per revolution, it is possible to move through micro-steps, which improves the step resolution. Micro-stepping also reduces torque ripple and power losses in the motor. The IP block generates theta that is used by the stepper motor control algorithm. It is possible to select micro-stepping up to 2048 micro steps. The profile of the stepper theta output and resultant current for various micro-stepping options are shown through the following figures.

Figure 1 • **Currents and Theta in Full Step Mode**



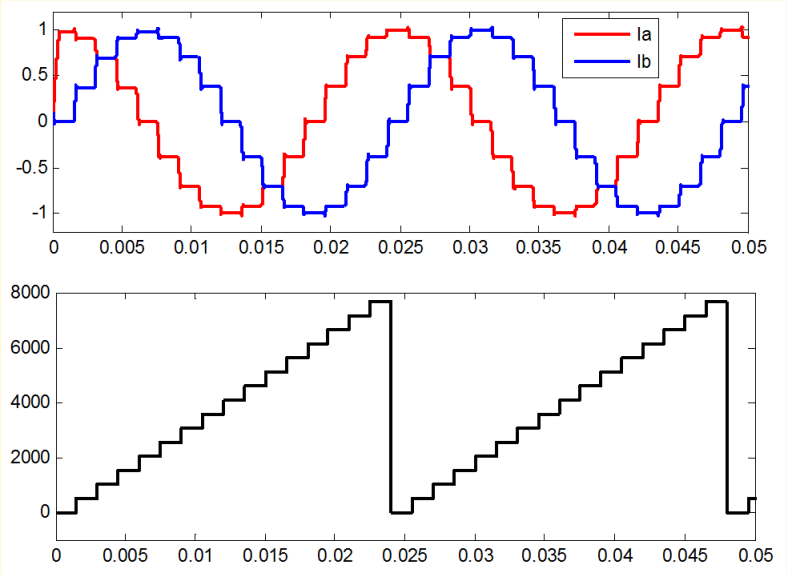
The following figure shows the theta generation in motor phase currents for half step mode.

Figure 2 • **Currents and Theta in Half Step Mode**



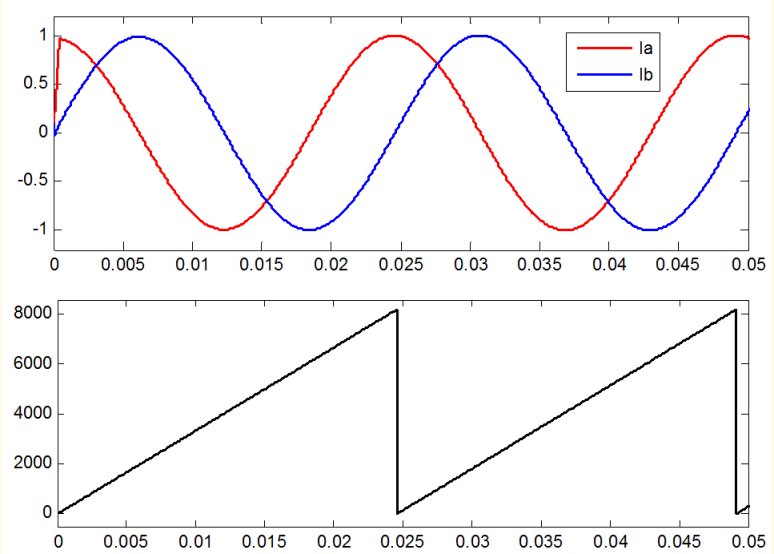
The following figure shows the theta generation motor phase currents in quarter step mode.

Figure 3 • **Currents and Theta in Quarter step mode (micro-stepping)**



The following figure shows the theta generation motor phase currents in 1024 micro-stepping mode.

Figure 4 • **Currents and Theta in 1/1024 step mode (micro-stepping)**



The level of micro stepping is decided by the rate limit input and must be an exponent of 2. The slew count input, then decides the speed at which theta value is updated. The output theta is generated till the command number of steps are met and then theta is held at last updated value until command steps changes. However, in speed mode, the output theta is continuously updated.

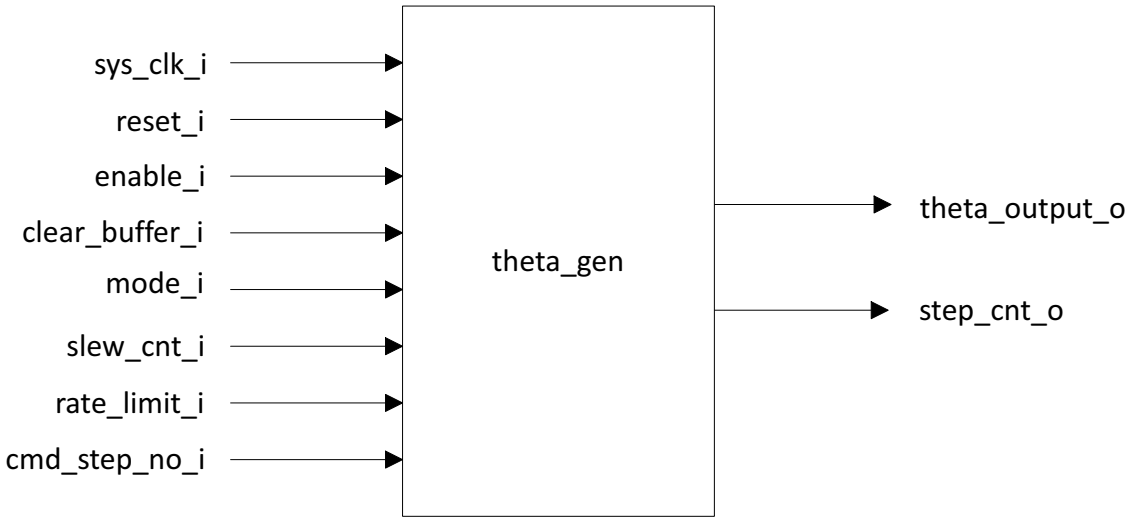
3 Hardware Implementation

This section describes the implementation details of the theta generation.

3.1 Design Description

The following figure shows the system-level block diagram of the theta generation.

Figure 5 • **System-Level Block Diagram of Theta Generation**



3.2 Inputs and Outputs

The following table lists the input and output ports of the theta generation configuration parameters

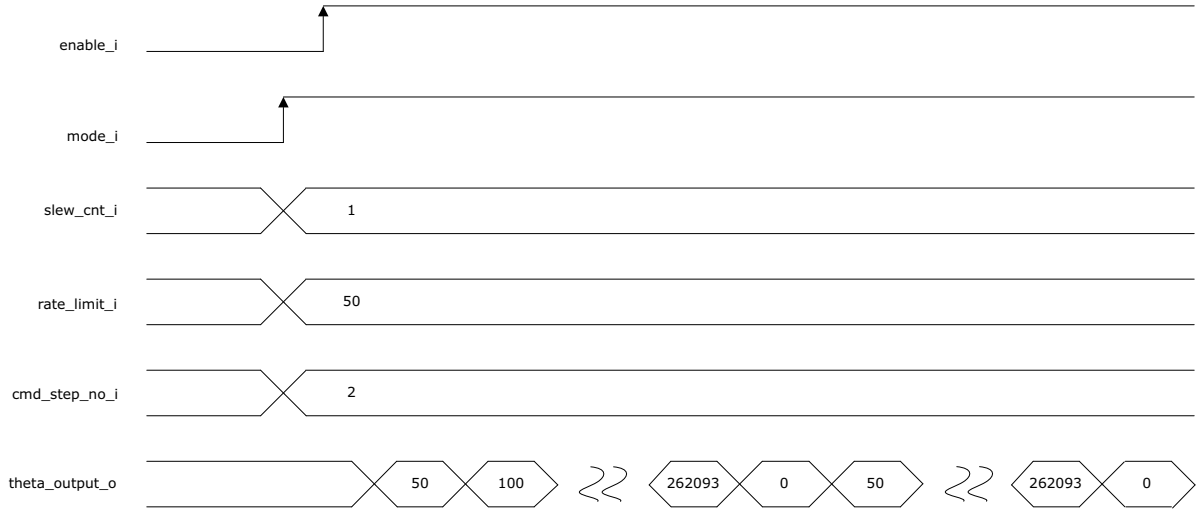
Table 1 • **Input and Output Ports of the Theta Generation**

Signal Name	Direction	Description
sys_clk_i	Input	System clock.
reset_i	Input	Asynchronous active low reset signal.
enable_i	Input	Input signal enables angle generation.
mode_i	Input	When set to 0 (zero), generates angle in the Position Mode. When set to 1, generates angle in the Speed Mode (Continuous rotation mode).
slew_cnt_i	Input	Slew count input – decides the speed at which theta value is updated in terms of 1 µs.
rate_limit_i	Input	Rate limit input – decides the number of Microsteps by defining angle increment. Microstep length should be exponent of 2 (for example, 1, 2, 4, 8, 16 and so on).
cmd_step_no_i	Input	Command – the number of steps/micro-steps motor must move.
theta_output_o	Output	Angle generated based on the inputs.
step_cnt_o	Output	Step count output to track the number of steps.

3.3 Timing Diagrams

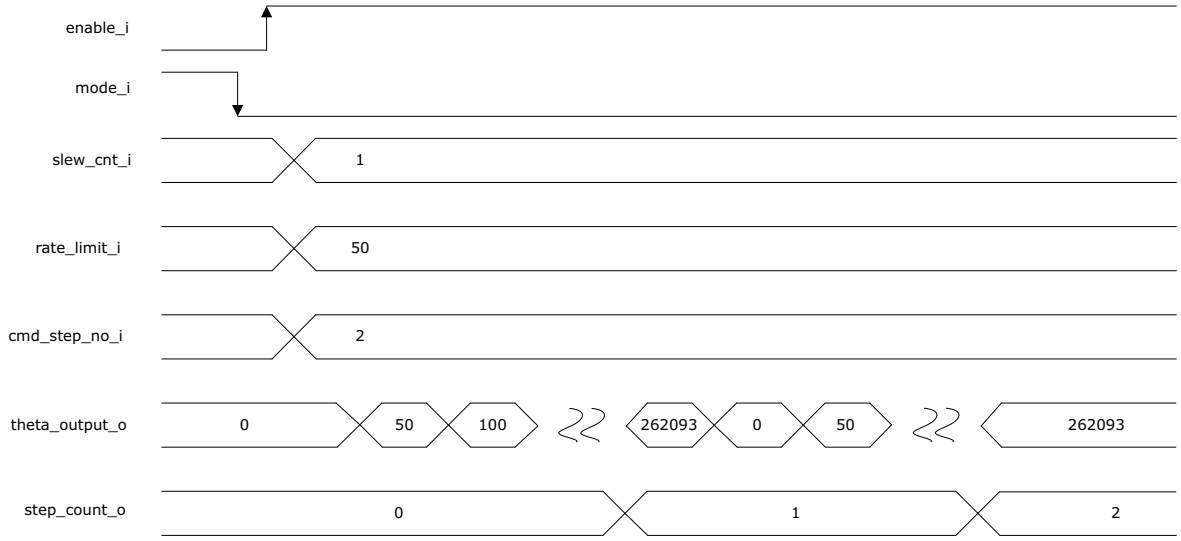
The following figure shows the timing diagram of the theta generation in speed mode.

Figure 6 • **Timing Diagram of the Theta Generation in Speed Mode**



The following figure shows the timing diagram of the theta generation in position mode.

Figure 7 • **Timing Diagram of the Theta Generation in Position Mode**



3.4 Resource Utilization

Theta generation is implemented on the SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) device. The following table lists the resource utilization report after synthesis.

Table 2 • **Resource Utilization of the Theta Generation**

Cell Usage	Description
SLE (Sequential)	130
Combinational Logic	230
BUFFER	0
MACC	0
RAM1kx18	0
RAM64x18	0