UG0595
User Guide
Rate Limiter IP v4.1

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- Added the IP version to the document title.
- Removed Configuration Parameter section from Hardware Implementation, page 4.

1.2 Revision 2.0

Updated SAR (69844).

1.3 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Introduction

A Rate Limiter controls the rate of change of variable and is used to avoid abrupt change of values that causes transient and jerky operation. Rate Limiter is generally used to generate a smooth speed profile while changing from one speed range to another speed range.

2.1 Rate Limiter Theory

The rate of change of output remains within the specified limit whether the output is increasing or decreasing with respect to time. The output slope is configured by two parameters—rate count and slew count. see the following figures.

Note: Rate count = Value with which output is incremented or decremented after every slew count

Note: Slew count = Wait period in number of start signals after which the output is updated

Figure 1 • **Acceleration**

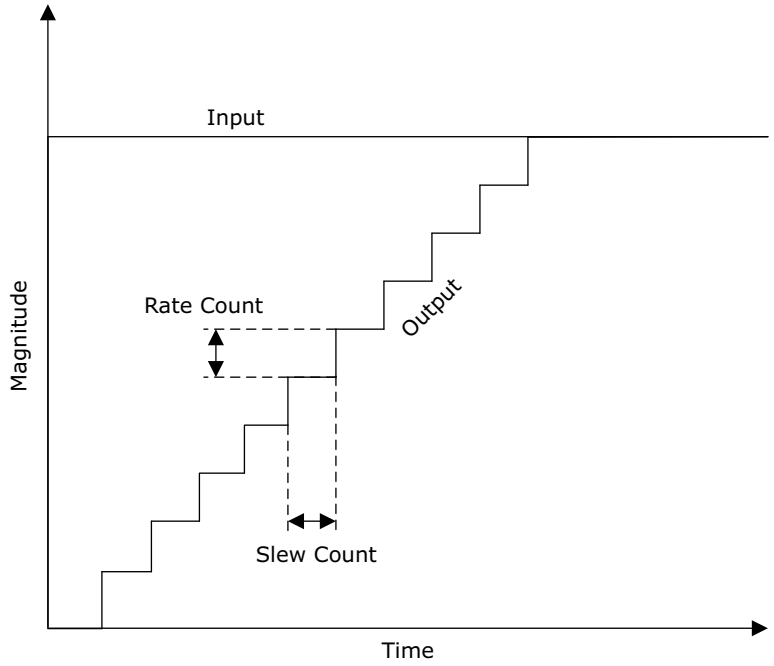
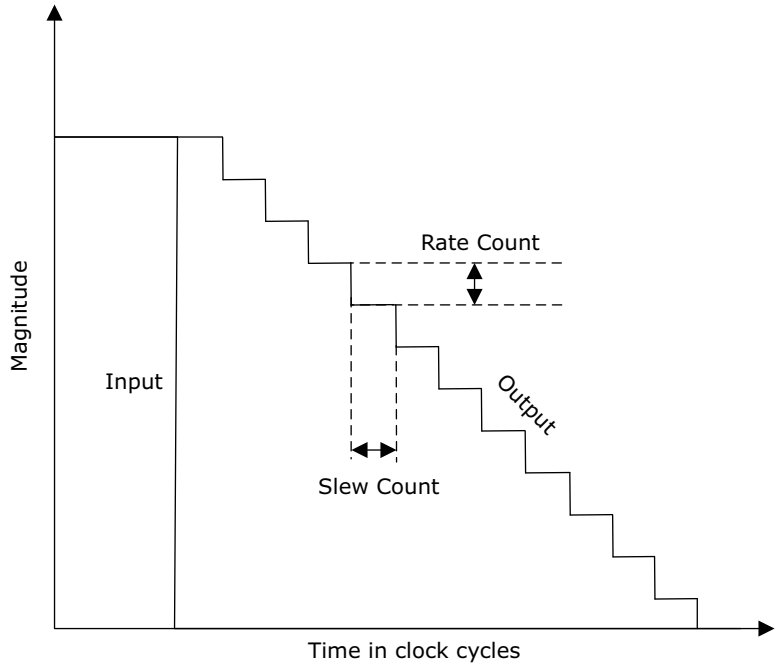


Figure 2 • **Deceleration**



The Rate Limiter IP also has a reset ramp input, which forces the output to zero instantaneously irrespective of the input value. This feature is useful for auto-restart in the motor control application to initialize speed reference output from the Rate Limiter IP to zero before starting motor again.

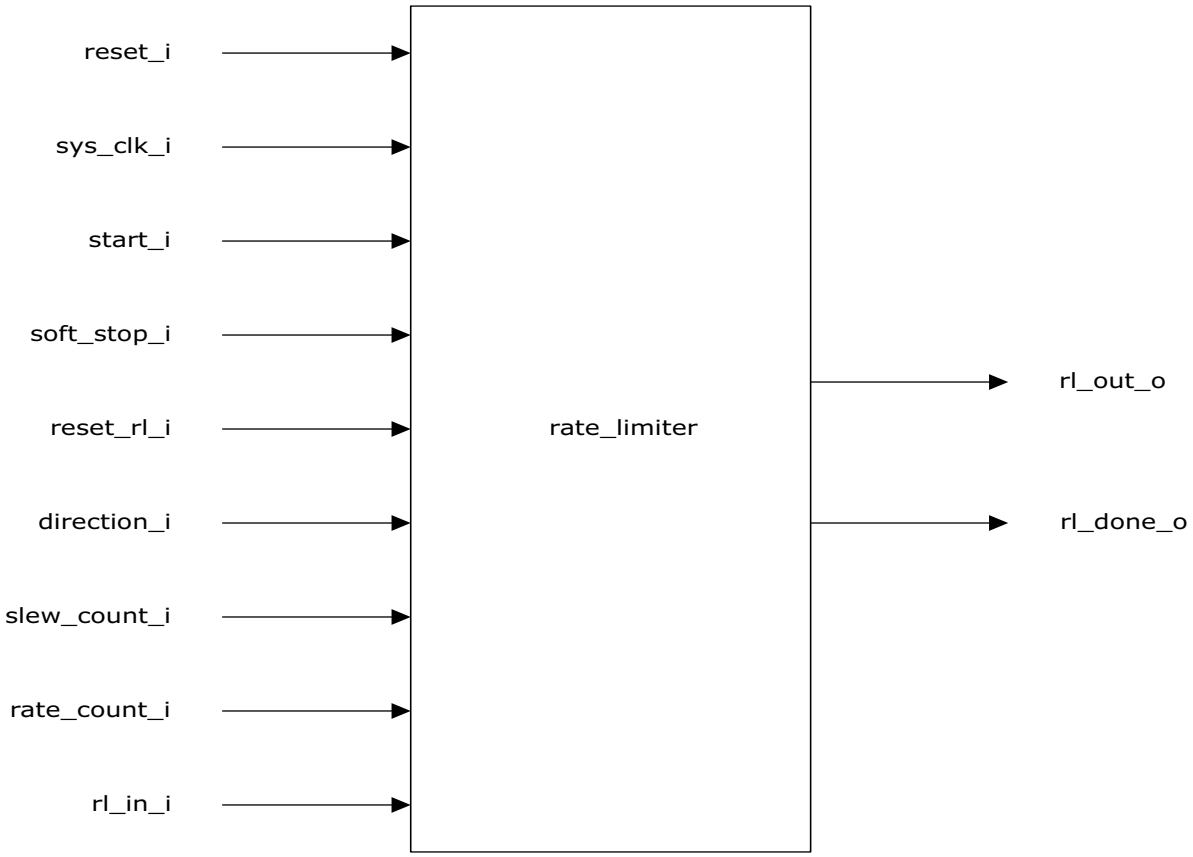
The soft stop input forces the output to zero irrespective of the input value. However, the output goes towards zero according to the ramp profile configured by slew count and rate count. Direction input is used to negate the input. This is generally related to changing direction of motor rotation.

3 Hardware Implementation

This section describes the implementation details of the Rate Limiter implemented in the SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) device.

The following figure shows the system-level block diagram of the rate limiter.

Figure 3 • **System-Level Block Diagram of Rate Limiter**



3.1 Inputs and Outputs

The following table lists the input and output ports of the Rate Limiter.

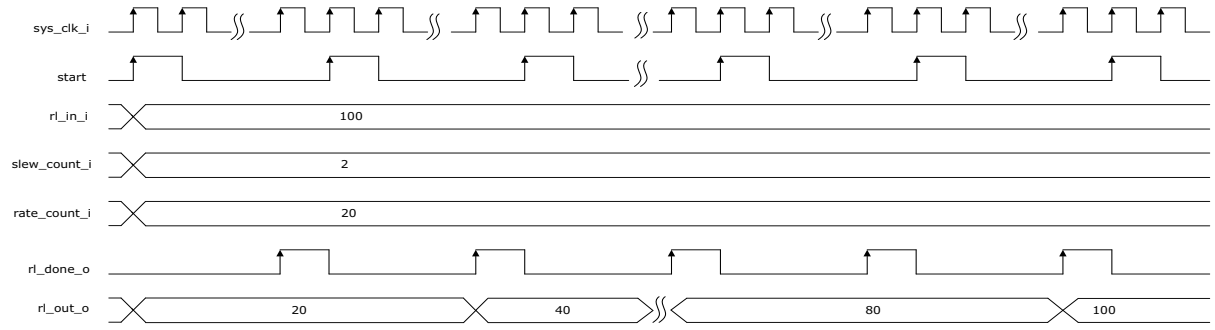
Table 1 • **Input and Output Ports of the Rate Limiter**

Signal Name	Direction	Description
reset_i	Input	Asynchronous active low reset signal to design
sys_clk_i	Input	System clock
start_i	Input	Start signal for module computation - high for one system clock cycle
soft_stop_i	Input	Triggers Soft Stop
reset_rl_i	Input	Resets the Rate Limiter output immediately
rl_in_i	Input	Input reference
slew_count_i	Input	Number of start signals after which the output is updated
rate_count_i	Input	Rate at which the output is incremented or decremented
direction_i	Input	Refers to the motor direction
rl_out_o	Output	Rate limited output of the block
rl_done_o	Output	Completion of block execution - high for one system clock cycle

3.2 Timing Diagrams

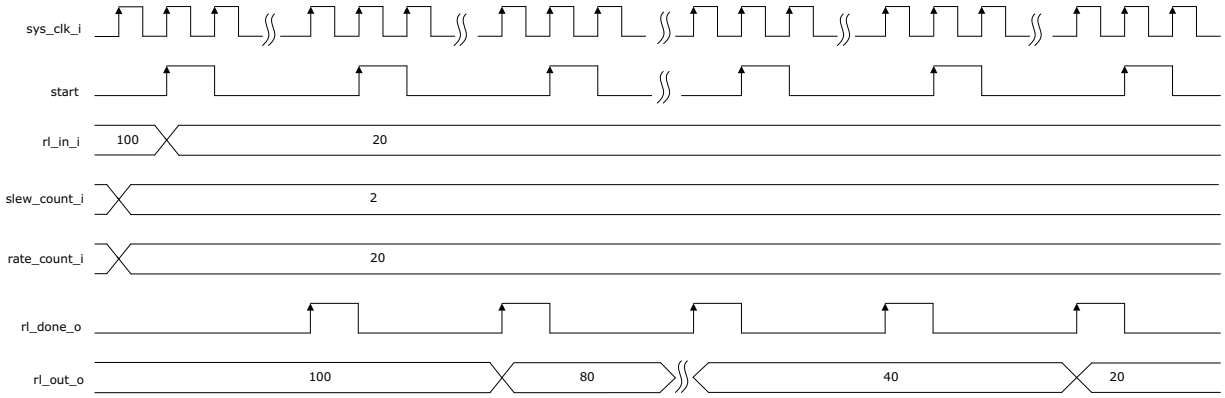
A minimum of three clock cycles are required between two successive start signals. The following figure shows the timing diagram for incrementing operation.

Figure 4 • **Timing Diagram for Incrementing Operation**



The following figure shows the timing diagram for decrementing operation.

Figure 5 • **Timing Diagram for Decrementing Operation**



3.3 Resource Utilization

The following table lists the resource utilization of the Rate Limiter implemented in the SmartFusion2 device.

Table 2 • **Resource Utilization of the Rate Limiter Block**

Cell Usage	Description
Sequential elements	80
Combinational logic	260
MACC	0
RAM1kx18	0
RAM64x18	0