UG0608
User Guide
BLDC Estimator v4.2

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Power Matters.

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 4.0

The following is a summary of the changes made in revision 4.0 of this document.

- Table 1, page 4 is updated to add a new signal name, clear_buffer_i and its description.
- Figure 2, page 3, is edited to add the input signal name, clear_buffer_i.
- Figure 3, page 5 is edited to show simultaneous generation of pulses for EALPHA_FILTER_START, EBETA_FILTER_START and EALPHA_FILTER_DONE, EBETA_FILTER_DONE pulses.

1.2 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- Added the IP version to the document title.
- Moved Configuration Parameter section in chapter 3, Hardware Implementation, page 3 to Configuration Parameters, page 5.

1.3 Revision 2.0

Updated for SAR 71202.

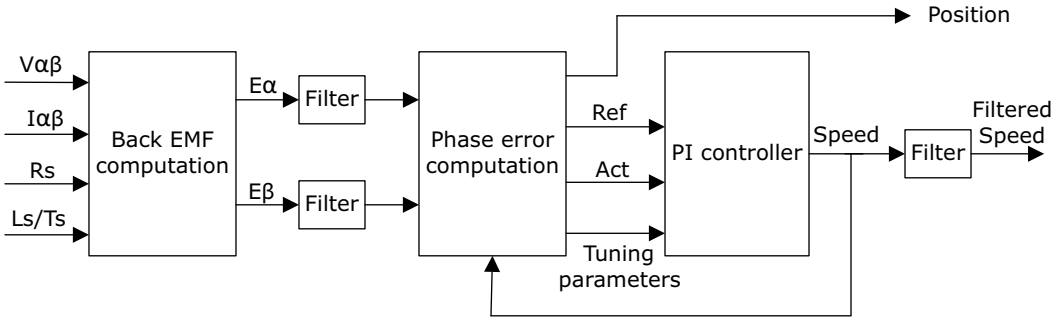
1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Introduction

The brush less DC (BLDC) estimator computes the rotor position based on motor parameters, voltage, and current values. The block also estimates motor speed. The algorithm is based on back-emf estimation and filtering. The motor parameters Rs, Ls, and sampling time Ts are used to build motor model. The voltages that are fed to the actual motor are fed to the motor model along with motor currents and are used to compute back-emf. A phase-locked loop (PLL) structure is used to find the angle of filtered back emf which is, aligned to rotor electrical position.

Figure 1 • **Block Diagram of BLDC Estimator**



The motor can accelerate or decelerate rapidly, in this case the rate of change of rotor position has to be dynamically and accurately tracked by the PLL. This is achieved by proper tuning of the PI controller that is part of the PLL.

The PLL block uses the theta_factor_i input to scale the speed used in computing the rotor angle. This value is computed as:

$$pll\_theta\_factor = \frac{67}{120} \times \frac{N_{rpm} \times N_{pp}}{f_{sw}}$$

where,

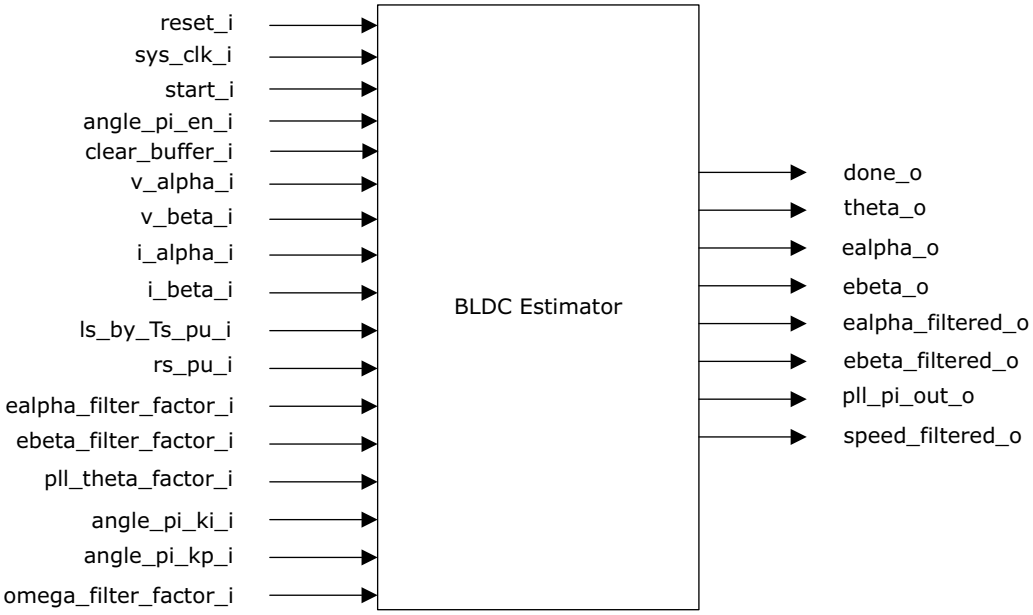
N_{rpm} is rated motor speed in RPM
N_{pp} is number of pole pairs
f_{sw} is switching frequency

3 Hardware Implementation

This section describes the implementation details of the BLDC estimator.

The following figure shows the system-level block diagram of the BLDC estimator.

Figure 2 • **System-Level Block Diagram of BLDC Estimator**



3.1 Inputs and Outputs

The following table lists the input and output ports of the BLDC estimator.

Table 1 • **Input and Output Ports of the BLDC Estimator**

Signal Name	Type	Description
reset_i	Input	Active low synchronous reset signal
sys_clk_i	Input	System clock
start_i	Input	Start signal to start module computation - must be high for one system clock cycle
clear_buffer_i	Input	When 1, internal speed filter buffer is cleared. When 0, buffer is normally operated.
angle_pi_en_i	Input	Enable signal for PLL PI controller
v_alpha_i	Input	Alpha axis voltage input for angle estimation
v_beta_i	Input	Beta axis voltage input for angle estimation
i_alpha_i	Input	Alpha axis current input for angle estimation
i_beta_i	Input	Beta axis current input for angle estimation
Ls_by_Ts_pu_i	Input	Motor Inductance L (in per unit) / sampling time
Rs_pu_i	Input	Motor Resistance R (in per unit)
ealpha_filter_factor_i	Input	Represents the Ealpha filter time constant – input as an exponent of 2 2^(ealpha_filter_factor_i) * sampling time
ebeta_filter_factor_i	Input	Represents the Ebeta filter time constant – input as an exponent of 2 2^(ebeta_filter_factor_i) * sampling time
pll_theta_factor_i	Input	Theta factor value
angle_pi_kp_i	Input	Proportional constant for angle PI
angle_pi_ki_i	Input	Integral constant for angle PI
omega_filter_factor_i	Input	Represents the speed filter time constant – input as an exponent of 2 2^(omega_filter_factor_i) * sampling time
done_o	Output	Indicates completion of speed computation. High for one clock cycle.
theta_o	Output	Estimated angle (theta) output
ealpha_o	Output	Back-emf on alpha axis
ebeta_o	Output	Back-emf on beta axis
ealpha_filtered_o	Output	Filtered back-emf on alpha axis
ebeta_filtered_o	Output	Filtered back-emf on beta axis
pll_pi_out_o	Output	Speed output from PLL
speed_filtered_o	Output	Filtered speed output

3.2 Configuration Parameters

The following table shows the configuration parameter used in the hardware implementation of the BLDC estimator. This parameter is a generic and can be varied based on the application requirement.

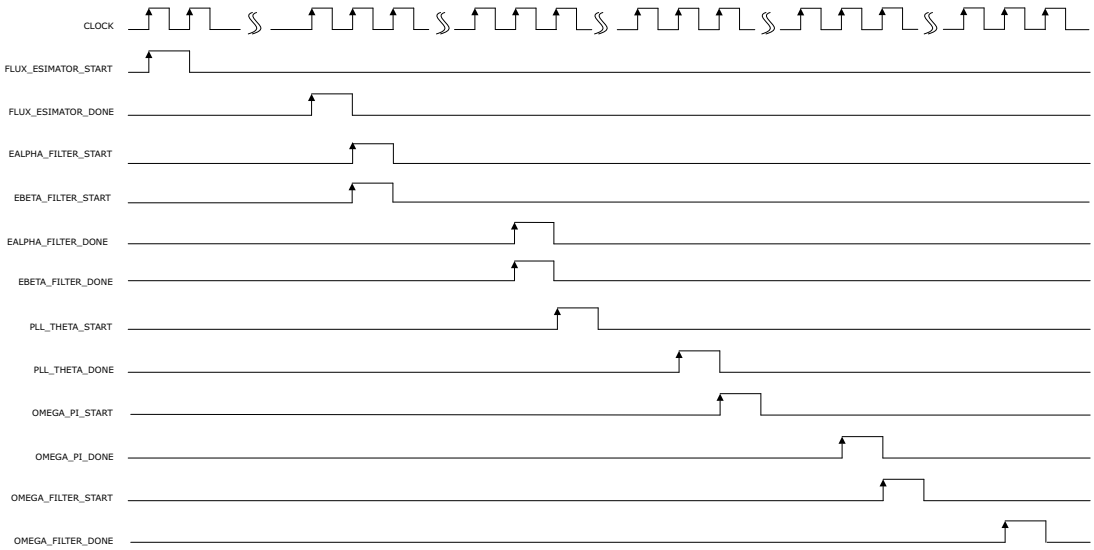
Table 2 • **Configuration Parameter of the BLDC Estimator**

Name	Description
g_NO_MCYCLE_PATH	Defines the number of clock delays required before asserting the multiplier done signal.

3.3 Timing Diagram

The following figure shows the timing diagram of the BLDC estimator.

Figure 3 • **Timing Diagram of the BLDC Estimator**



3.4 Resource Utilization

BLDC estimator is implemented on the SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA), IGLOO®2 and RTG4™ devices. The following table lists the resource utilization report after synthesis.

Table 3 • **Resource Utilization of the BLDC Estimator**

Cell Usage	Description
Sequential elements	890
Combinational logic	1450
MACC	3
RAM1kx18	0
RAM64x18	0