Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 January 2015</td>
<td>1</td>
<td>First release</td>
</tr>
</tbody>
</table>

Confidentiality Status
This is a non-confidential document.
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Introduction

This user guide describes the RTG4™ Power Estimator for RTG4 field programmable gate array (FPGA) device families. Early power estimation helps designers to define the architecture within the power budget by applying power saving strategies. It also helps the board designers to design and select the power supplies and heat sink. The Power Estimator workbook is used to estimate the power consumption from early design concept to design implementation. It also provides details about thermal analysis and factors that contribute to power consumption. Device resources, operating frequency, clock resources, toggle rates, and many other parameters are entered into the Power Estimator workbook. These parameters are then combined with the power models to estimate the power. The power models are based on simulation or characterized device data.

The accuracy of power estimation depends on the data entered into the workbook. Therefore, ensure that realistic data is entered into the design. The actual power depends greatly on actual RTL design, place-and-route, and operating conditions. The Power Estimator result is an early estimation of power consumption rather than measured. Use the SmartPower tool in the Libero® System-on-Chip (SoC) software for accurate and detailed power estimations for designs after place-and-route. Power must be measured during device operation.

Features

The RTG4 Power Estimator has the following features:

- Estimation of power consumption from design concept phase to implementation.
- Integrated graphical user interface (GUI) in a worksheet to initialize the Power Estimator and for I/O Bank voltage settings.
- Power estimation of Active and Standby power modes.
- Power estimation using scenarios.
- Separate worksheet for device features and also a subtotal of power consumed by each device feature.
- Calculation of the Junction temperature and thermal input support.

Additional Documentation

- RTG4 FPGA Product Brief
- RTG4 FPGA Pin Descriptions
- RTG4 FPGA Fabric User Guide
- RTG4 FPGA High Speed DDR Interfaces User's Guide
- RTG4 FPGA High Speed Serial Interfaces User Guide
- RTG4 FPGA Clocking Resources User Guide
- Libero SoC User Guide
Launching Power Estimator

This section contains the following sub sections:

- System Requirement
- Downloading Power Estimator and Enabling Macros
- Minimum Input Requirements

System Requirement

- The Power Estimator workbook requires Microsoft Excel. Table 1 shows the supported software.
- Windows operating system.

Table 1 • Supported Software

<table>
<thead>
<tr>
<th>Supported Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microsoft Excel 2003</td>
</tr>
<tr>
<td>Microsoft Excel 2007</td>
</tr>
<tr>
<td>Microsoft Excel 2010</td>
</tr>
<tr>
<td>Microsoft Excel 2013</td>
</tr>
</tbody>
</table>

Note: OpenOffice and Google Docs spreadsheet editors are not supported.

Downloading Power Estimator and Enabling Macros

The Power Estimator workbook for the RTG4 devices are available in the RTG4 Lead Customer Program (LCP) Documents and Design Resources web page. The latest version can be downloaded from:
http://www.microsemi.com/rtg4-lcp

The Power Estimator workbook has several built-in macros. By default, the macro security level in Microsoft Excel software is set to High. The macros are automatically disabled if the macro security level is set to High. Ensure that Microsoft Excel settings allow macro executions for the Power Estimator workbook to function properly.

The following sections describe how to change the macro security settings in different versions of Microsoft Excel software:

- "Microsoft Excel 2003" on page 6
- "Microsoft Excel 2007" on page 6
- "Microsoft Excel 2010 and 2013" on page 8
Microsoft Excel 2003

1. Open the Power Estimator Excel file and select **Tools > Macro > Security** from the main menu.

2. From the **Macro Security** dialogue box, click **Security Level** tab and select **Medium**. Click **OK**.

3. Close the Power Estimator file and reopen it.

4. Click **Enable Macros** when prompted to enable macros.

Microsoft Excel 2007

1. Open the Power Estimator Excel file and click the **Office** button at the upper left corner.
2. Click Excel Options.

3. Click Trust Center from the left panel.
4. Click Trust Center Settings....
5. From the Trust Center window, click Macro Settings from the left panel. Select Disable all macros with notification and click OK.
6. Close the Power Estimator file and reopen it.
7. A security warning notification appears under the Office ribbon. Click Options.
8. Choose Enable this content in the Microsoft Office Security Options window.
Microsoft Excel 2010 and 2013
1. Open the Power Estimator Excel file.
2. Click the File tab and click Options.

3. Click Trust Center from the left panel.
4. Click Trust Center Settings....
5. From the Trust Center window, click Macro Settings from the left panel. Select Disable all macros with notification and click OK.
6. Close the Power Estimator file and reopen it.
7. A security warning notification appears under the Office ribbon. Click Options.
8. Choose Enable this content in the Microsoft Office Security Options window.

Minimum Input Requirements
Estimating power for the RTG4 devices is highly dependent on the amount of logic present in the FPGA Fabric.
The following are the minimum input requirements for a reasonably accurate power estimation:
• Select a proper device with suitable operating conditions.
• Proper estimation of FPGA Fabric resources (for example, flip-flops, LUTs, LSRAM, uSRAM, MACC, and I/O).
• Proper estimation of high speed serial and DDR interfaces.
• System clock and clock domain.
• Toggle rates of logic and I/Os.
• Enable, write, and read rates for RAMs.

Power Estimator Excel Workbook

This section describes each worksheet of the RTG4 Power Estimator Excel workbook. Separate worksheets for device features are available. Also, a subtotal of power consumed by each device feature is available. The usage and activity details of the different resources available in the targeted RTG4 device can be entered (for example, flip-flops, LUTs, LSRAM, uSRAM, MACC, I/O, high speed serial and DDR interfaces, system clock and clock domain, toggle rates of logic, and I/Os). The Power Summary section in the Summary worksheet provides the total power and power breakdown by rail and resource type.

This section contains the following sub sections:
  • Cell Color-Coding
  • Recommended Flow

Cell Color-Coding

The RTG4 Power Estimator Excel workbook has several worksheets. The cells of each worksheet are color coded to simplify the data entry and review.

Table 2 lists the cell colors and description.

<table>
<thead>
<tr>
<th>Table 2 • Cell Color Coding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cell color</strong></td>
</tr>
<tr>
<td>Editable</td>
</tr>
<tr>
<td>Non Editable</td>
</tr>
<tr>
<td>Read-Only</td>
</tr>
<tr>
<td>Read-Only</td>
</tr>
<tr>
<td>Read-Only</td>
</tr>
</tbody>
</table>

Recommended Flow

**Step - 1: Settings**

Select the device, package, temperature grade, operating condition and thermal inputs settings.

**Step - 2: Active Mode Configuration**

Set up the design specific information that is used to compute the dynamic power.

• FPGA Fabric Components:
  – Set up the FPGA Fabric components and their operating frequencies.

• I/Os:
  – Set up the I/O technology and their operating frequencies.

• Built-in Blocks (SERDES and FDDR):
  – Configure the SERDES and DDR subsystems with appropriate settings.

**Step - 3: Scenarios**

Optional: Update the percentage of time the device must be in a given mode during its operational time (for instance, 50% of the time Active and 50% in Standby).
Step - 4: Power Estimation Summary

The power summary section in the Summary worksheet provides the total power and its breakdown based on the power sources and rails. The total power for the scenario is described in "Step - 3: Scenarios" on page 25.

The following sections describe these steps in detail:

- "Step - 1: Settings" on page 10
- "Step - 2: Active Mode Configuration" on page 13
- "Step - 3: Scenarios" on page 25
- "Step - 4: Power Estimation Summary" on page 26

Step - 1: Settings

Figure 4 shows the Settings section in the Summary worksheet.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>General Settings</td>
<td></td>
</tr>
<tr>
<td>Family</td>
<td>RTG4</td>
</tr>
</tbody>
</table>

Table 3 • General and Thermal Inputs Settings

Figure 4 • Settings Section in Summary Worksheet

Table 3 shows the General and Thermal Inputs settings in the Settings section of the Summary worksheet. Ensure that you select the device with the appropriate operating conditions.
**Table 3 • General and Thermal Inputs Settings (continued)**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
<th></th>
</tr>
</thead>
</table>
| Device              | Select the device.  
The following devices are supported:  
• RT4G150           |  |
| Package             | Select the package. |  |
| Range               | Select the product grade.  
The following grades are available:  
• Military  
Temperature grade for different ranges:  
• Military (-55°C to 125°C) |  |
| Core Voltage        | Core supply voltage (1.2 V) |  |
| Process             | Select the process.  
The following conditions are available:  
• Typical  
Process accounts for manufacturing process variations that affect power dissipation. **Typical** uses average power dissipation factors for your design. Voltage and Temperature are controlled independent of the process. |  |
| Data State          | **Advanced:**  
Initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.  
**Preliminary:**  
Information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.  
**Production:**  
Information that is considered to be final. |  |

**Thermal Inputs**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
<th></th>
</tr>
</thead>
</table>
| Junction Temperature $T_j$ (°C)  
**Note:** Thermal data is not yet available. **User Entered $T_j$ option is only supported.** | Enter the Junction Temperature of the device.  
This field is available only when **User Entered $T_j$** option is selected. In this case, other thermal input fields are disabled.  
When **Estimated $T_j$** option is selected, the junction temperature is calculated based on the thermal inputs entered. |  |
| Ambient Temperature $T_a$ (°C)  | Enter the temperature of the air surrounding the device. This field is available only if **Estimated $T_j$** option is selected.  
Valid temperature ranges are:  
• Military: -55°C to 125°C  
When **Estimated Theta $J_A$** option is selected, this field is used to calculate the junction temperature based on the thermal resistance and power dissipation.  
When **Custom Theta $J_A$** option is selected, this field is used to calculate the junction temperature based on the Effective $\theta_{JA}$ and power dissipation. |  |
Table 3 • General and Thermal Inputs Settings (continued)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
</table>
| Effective $\theta_{JA}$  | Effective thermal resistance. User selected device, package, airflow, heat sink and board model are used with characterization and simulation data to calculate effective thermal resistance. To enter a custom effective Theta JA, select Custom Theta JA and enter a value, to account for conditions not covered by the available choices or where more extensive thermal modeling has been done. The following fields are disabled when Custom Theta JA is selected and enabled Estimated Theta JA is selected:  
  • Heat Sink  
  • Air Flow  
  • Custom $\theta_{SA} \left( ^\circ C/W \right)$  
  • Board Thermal Model |
| Heat Sink                | Select one of the following options:  
  • None  
  • Custom  
  • 10 mm-Low Profile  
  • 15 mm-Medium Profile  
  • 20 mm-High Profile  
  This field is enabled only when Estimated $T_J$ and Estimated Theta JA options are selected. |
| Airflow                  | Select an ambient airflow in meter per second (m/s):  
  • 1.0 m/s  
  • 2.5 m/s  
  This field is enabled only when Estimated $T_J$ and Estimated Theta JA options are selected. The junction temperature is reduced if the ambient airflow is increased. |
| Custom $\theta_{SA} \left( ^\circ C/W \right)$ | If a custom heat sink is selected, enter the heat sink-to-ambient thermal resistance from the heat sink datasheet.  
  This field is enabled only when Estimated $T_J$ and Estimated Theta JA options are selected. |
| Board Thermal Model      | Select one of the following options:  
  • None (Conservative)  
  • JEDEC (2s2p)  
  This field is enabled only when Estimated $T_J$ and Estimated Theta JA options are selected. If None (Conservative) option is selected, the thermal model assumes that no heat is dissipated through the board. If JEDEC (2s2p) option is selected, the thermal model assumes that the characteristics is of the JEDEC 2s2p test board specified in standard JESD51-9. |
Step - 2: Active Mode Configuration

In this section, enter design specific information that can be used to compute dynamic power. It contains the following subsections:

- "Initialize Power Estimator Wizard" on page 13
- "FPGA Fabric Components" on page 14
- "I/O" on page 20
- "Built-in Blocks" on page 23

Initialize Power Estimator Wizard

The Summary worksheet has an integrated power estimator wizard. Click Initialize Power Estimator at the top left of the worksheet to invoke the Initialize Power Estimator wizard. This wizard enables the user to select design specific information. Upon running the wizard, it populates the Power Estimator spreadsheet with design specific information and estimates power for the design. Change the wizard populated entries to provide more accurate inputs to the Power Estimator.

Figure 5 shows the Initialize Power Estimator wizard.

---

**Figure 5**  
**Power Estimator Wizard**

The Power Estimator wizard provides following fields depending on the product family selected:

- **FDDR**  
  Select the memory type, width, ECC, ODT, and FDDR_CLK. Maximum frequency of FDDR_CLK is 333 MHz.

- **SERDES_IF**  
  Select PCIE sub-system (PCIES), non-PCIE sub-system (NPSS), Protocol, Number of Lanes, AXI/AHB_CLK (PCIe) clock, and Ref Clk Freq.

- **FPGA Fabric**  
  - System Clock
Specify the Fabric clock frequency. By default, it is set to 100 MHz. Valid entries are between 0 and 300 MHz.

- **Design Utilization**
  Use the drop-down menu against Set all FPGA Fabric Resources to set a percentage value for all the resources at one go. Percentage value for each resource to be utilized can be set using the slide bar against the resources.

  Following are the available resources:
  * Flip-Flops
  * LUTs
  * uSRAM
  * LSRAM
  * MACC

- **I/O**
  Select the I/O technology and enter the number of inputs and outputs.

- **Default Toggle Rate**
  Enter a toggle rate in percentage. This toggle rate applies to all logic module and I/Os.

- **Default RAM Enable Rate**
  Enter an enable rate in percentage. This enable rate applies to uSRAM and LSRAM.

*Note:* When the slider thumb moves between the end points of the slider track, the value is updated in the corresponding text field.

To populate the Power Estimator spreadsheet with the entered values, click **OK**.

**FPGA Fabric Components**

This section describes the design specific information for FPGA Fabric components that are used to calculate dynamic power. The RTG4 Power Estimator workbook provides separate worksheets for each FPGA Fabric component. These worksheets are described in the following subsections:

- "Clock" on page 14
- "Logic" on page 15
- "LSRAM" on page 16
- "uSRAM" on page 17
- "Math Block" on page 18
- "CCC" on page 19

**Clock**

The RTG4 devices support only global clock networks. Each row in the Clock worksheet represents a separate clock domain.

Enter the following parameters for each clock domain:

- Name
- Clock Frequency (MHz)
- Fanout
- Global Enable Rate
Figure 6 shows the Clock worksheet.

![Clock Worksheet](image)

**Figure 6 • Clock Worksheet**

Table 4 shows the parameters to be entered in the Clock worksheet.

**Table 4 • Clock Worksheet Parameters**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Enter a name for each clock domain (optional).</td>
</tr>
<tr>
<td>Clock Frequency (MHz)</td>
<td>Enter the clock frequency of the domain. The maximum frequency of the FPGA Fabric is 300 MHz.</td>
</tr>
<tr>
<td>Fanout</td>
<td>Enter the number of registers and other synchronous elements (LSRAM, uSRAM, Math Block and I/O) clocked.</td>
</tr>
<tr>
<td>Global Enable Rate</td>
<td>Enter the average percentage of time that clock enable is high for each clock domain.</td>
</tr>
</tbody>
</table>

For more information about the clock networks of the supported device families, refer to *RTG4 FPGA Clocking Resources User Guide*.

**Logic**

Each row in the Logic worksheet represents a separate clock domain. Enter the following parameters for each clock domain:

- Name
- Clock Frequency (MHz)
- Number of Registers
- Number of LUTs
- Fanout
- Toggle Rate
Figure 7 shows the Logic worksheet.

Table 5 shows the parameters to be entered in the Logic worksheet.

### Table 5 • Logic Worksheet Parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Enter a name for each clock domain (optional).</td>
</tr>
<tr>
<td>Clock Frequency (MHz)</td>
<td>Enter the clock frequency of the domain. The maximum frequency of the FPGA Fabric is 300 MHz.</td>
</tr>
<tr>
<td>Number of Registers</td>
<td>Enter the number of registers for each clock domain.</td>
</tr>
<tr>
<td>Number of LUTs</td>
<td>Enter the number of regular LUT (combinatorial) modules.</td>
</tr>
<tr>
<td>Average Fanout</td>
<td>Enter the average fanout of the nets driven by the registers and LUTs.</td>
</tr>
<tr>
<td>Toggle Rate</td>
<td>Enter the toggle rate of register and LUTs outputs.</td>
</tr>
</tbody>
</table>

For more information about the Logic Element of the supported device families, refer to RTG4 FPGA Fabric User Guide.

**LSRAM**

Each row in the LSRAM worksheet represents a separate clock domain.

Enter the following parameters for each clock domain:

- Name
- Number of LSRAM blocks
- Port A - Clock Frequency (MHz)
- Port A - Write Rate
- Port A - Enable Rate
- Port B - Clock Frequency (MHz)
- Port B - Write Rate
- Port B - Enable Rate
Figure 8 shows the LSRAM worksheet.

Table 6 shows the parameters to be entered in the LSRAM worksheet.

**Table 6 • LSRAM Worksheet Parameters**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Enter the name of the module or clock domain containing the LSRAM.</td>
</tr>
<tr>
<td>Number of LSRAM blocks</td>
<td>Enter the number of LSRAM blocks.</td>
</tr>
<tr>
<td>Port A - Clock Frequency (MHz)</td>
<td>Enter the clock frequency for Port A of the LSRAM blocks. It supports a maximum frequency of up to 300 MHz.</td>
</tr>
<tr>
<td>Port A - Write Rate</td>
<td>Enter the percentage of time that Port A is used for write operations. The remaining time is used for read operations.</td>
</tr>
<tr>
<td>Port A - Enable Rate</td>
<td>Enter the percentage of time that Port A is enabled.</td>
</tr>
<tr>
<td>Port B - Clock Frequency (MHz)</td>
<td>Enter the clock frequency for Port B of the LSRAM blocks. It supports a maximum frequency of up to 300 MHz.</td>
</tr>
<tr>
<td>Port B - Write Rate</td>
<td>Enter the percentage of time that Port B is used for write operations. The remaining time is used for read operations.</td>
</tr>
<tr>
<td>Port B - Enable Rate</td>
<td>Enter the percentage of time that Port B is enabled.</td>
</tr>
</tbody>
</table>

For more information about the LSRAM of the supported device families, refer to *RTG4 FPGA Fabric User Guide*.

**uSRAM**

Each row in the uSRAM worksheet represents a separate clock domain. Enter the following parameters for each clock domain:

- Name
- Number of uSRAM blocks
- Port A - Read Clock Frequency (MHz)
- Port A - Enable Rate
- Port B - Read Clock Frequency (MHz)
- Port B - Enable Rate
- Port C - Write Clock Frequency (MHz)
- Port C - Enable Rate
Figure 9 shows the uSRAM worksheet.

Table 7 shows the parameters to be entered in the uSRAM worksheet.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Enter the name of the module or clock domain containing the uSRAM.</td>
</tr>
<tr>
<td>Number of uSRAM blocks</td>
<td>Enter the number of uSRAM blocks.</td>
</tr>
<tr>
<td>Port A - Read Clock Frequency (MHz)</td>
<td>Enter the read clock frequency for Port A of the uSRAM blocks. It supports a maximum frequency of up to 300 MHz.</td>
</tr>
<tr>
<td>Port A - Enable Rate</td>
<td>Enter the percentage of time that Port A is enabled.</td>
</tr>
<tr>
<td>Port B - Read Clock Frequency (MHz)</td>
<td>Enter the read clock frequency for Port B of the uSRAM blocks. It supports a maximum frequency of up to 300 MHz.</td>
</tr>
<tr>
<td>Port B - Enable Rate</td>
<td>Enter the percentage of time Port B is enabled.</td>
</tr>
<tr>
<td>Port C - Write Clock Frequency (MHz)</td>
<td>Enter the write clock frequency for Port C of the uSRAM blocks. It supports a maximum frequency of up to 300 MHz.</td>
</tr>
<tr>
<td>Port C - Enable Rate</td>
<td>Enter the percentage of time that Port C is enabled.</td>
</tr>
</tbody>
</table>

For more information about the uSRAM of the supported device families, refer to RTG4 FPGA Fabric User Guide.

Math Block
Each row in the Math Block worksheet represents a separate clock domain.
Enter the following parameters for each clock domain:

- Name
- Clock Frequency (MHz)
- Number of Math Blocks
- Data Toggle Rate
Figure 10 shows the *Math Block* worksheet.

![Math Block Worksheet](image)

**Table 8 • Math Block Worksheet Parameters**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Enter the name of the module or clock domain containing Math Block.</td>
</tr>
<tr>
<td>Clock Frequency (MHz)</td>
<td>Enter the clock frequency of the domain. The maximum frequency of the Math Block is 300 MHz.</td>
</tr>
<tr>
<td>Number of Math Blocks</td>
<td>Enter the number of math blocks for each clock domain.</td>
</tr>
<tr>
<td>Data Toggle Rate</td>
<td>Enter the average data bus toggle rate.</td>
</tr>
</tbody>
</table>

For more information about the Math Block of the supported device families, refer to *RTG4 FPGA Fabric User Guide*.

**CCC**

The RTG4 devices have eight CCCs. Each CCC enables flexible clocking schemes for the logic implemented in the FPGA Fabric and can provide the base clock for on-chip hard IP blocks such as FDDR and SERDESIF.

Enter the following parameters for each CCC:

- Name
- Reference Clock Frequency (MHz)
- PLL Output Frequency (MHz)
- Output1 Frequency (MHz)
- Output2 Frequency (MHz)
- Output3 Frequency (MHz)
- Output4 Frequency (MHz)
Figure 11 shows the CCC Power section in the CCC worksheet.

**Table 9 • CCC Section Parameters**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Enter the name of the CCC module.</td>
</tr>
<tr>
<td>Reference Clock Frequency (MHz)</td>
<td>Enter the reference clock frequency.</td>
</tr>
<tr>
<td>PLL Output Frequency (MHz)</td>
<td>Enter the PLL output frequency.</td>
</tr>
<tr>
<td>Output1 Frequency (MHz)</td>
<td>Enter the output1 (GL0/Y0) frequency.</td>
</tr>
<tr>
<td>Output2 Frequency (MHz)</td>
<td>Enter the output2 (GL1/Y1) frequency.</td>
</tr>
<tr>
<td>Output3 Frequency (MHz)</td>
<td>Enter the output3 (GL2/Y2) frequency.</td>
</tr>
<tr>
<td>Output4 Frequency (MHz)</td>
<td>Enter the output4 (GL3/Y3) frequency.</td>
</tr>
</tbody>
</table>

For more information about the CCC of the supported device families, refer to *RTG4 FPGA Clocking Resources User Guide*.

**I/O**

Design specific information are entered in the I/O worksheet for the I/Os used to calculate dynamic power. Each row represents a clock frequency and an I/O domain. Enter the following parameters for each row:

- Name
- Bank Type
- I/O standard
- I/P Pins
- O/P Pins
- Bidir Pins
- ODT
- Output Drive (mA)
- Output Load (pF)
- Clock (MHz)
- Data Rate
- Toggle Rate
- Output Enable
- ODT Enable

Figure 12 shows the I/O worksheet.

<table>
<thead>
<tr>
<th>Name</th>
<th>Bank Type</th>
<th>I/O Standard</th>
<th>IP Pins</th>
<th>QOP Pins</th>
<th>Bidir Pins</th>
<th>ODT</th>
<th>Output Drive (mA)</th>
<th>Output Load (pF)</th>
<th>Clock (MHz)</th>
<th>Data Rate</th>
<th>Toggle Rate</th>
<th>Output Enable</th>
<th>ODT Enable</th>
<th>VOIO</th>
<th>VOII</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>MS0</td>
<td>LVCMOS25</td>
<td>2, 5</td>
<td>3</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0</td>
<td>0, 0</td>
<td>0, 0</td>
</tr>
<tr>
<td>MS0</td>
<td>LVCMOS25</td>
<td>2, 5</td>
<td>3</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0</td>
<td>0, 0</td>
<td>0, 0</td>
</tr>
<tr>
<td>MS0</td>
<td>LVCMOS25</td>
<td>2, 5</td>
<td>3</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0, 0</td>
<td>0, 0</td>
<td>0, 0</td>
<td>0, 0</td>
</tr>
</tbody>
</table>
Table 10 shows the parameters to be entered in the I/O worksheet. The advanced I/O settings, Schmitt trigger, Pre-emphasis, and Slew are not visible by default. Select Show Advanced I/O Settings to unhide these columns.

**Table 10 • I/O Worksheet Parameters**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Enter a name for each I/O, bus or module.</td>
</tr>
<tr>
<td>I/O Settings</td>
<td></td>
</tr>
<tr>
<td>Bank Type</td>
<td>Select the bank type.</td>
</tr>
<tr>
<td></td>
<td>Supports the followings types of banks:</td>
</tr>
<tr>
<td></td>
<td>• MSIO</td>
</tr>
<tr>
<td></td>
<td>• MSIOD</td>
</tr>
<tr>
<td></td>
<td>• DDRIO</td>
</tr>
<tr>
<td>I/O standard</td>
<td>Select the appropriate I/O standard.</td>
</tr>
<tr>
<td>I/P Pins</td>
<td>Enter the number of input pins or differential pair used for each I/O, bus</td>
</tr>
<tr>
<td></td>
<td>or module. The differential pair must be considered as a single pin.</td>
</tr>
<tr>
<td>O/P Pins</td>
<td>Enter the number of output pins or differential pair used for each I/O, bus</td>
</tr>
<tr>
<td></td>
<td>or module. The differential pair must be considered as a single pin.</td>
</tr>
<tr>
<td>Bidir Pins</td>
<td>Enter the number of bidirectional pins or differential pair used for each</td>
</tr>
<tr>
<td></td>
<td>I/O, bus or module. The differential pair must be considered as single pin.</td>
</tr>
<tr>
<td>ODT</td>
<td>Select the Input On-die termination impedance.</td>
</tr>
<tr>
<td>Output Drive (mA)</td>
<td>Select the output drive current.</td>
</tr>
<tr>
<td>Output Load (pF)</td>
<td>Enter the board and other external capacitance.</td>
</tr>
<tr>
<td>Schmitt Trigger</td>
<td>Configure (Yes/No) Schmitt trigger.</td>
</tr>
<tr>
<td>Pre-emphasis</td>
<td>The choices for Pre Emphasis depends on the I/O type (MSIO/MSIOD/DDRIO) and</td>
</tr>
<tr>
<td></td>
<td>I/O standard. Configure (No/Low/Medium/High) Pre-emphasis.</td>
</tr>
<tr>
<td>Slew</td>
<td>Configure (Slow/Medium/Medium_Fast/Fast) Slew. The choices for Slew</td>
</tr>
<tr>
<td></td>
<td>depends on the I/O type (MSIO/MSIOD/DDRIO) and the I/O standard.</td>
</tr>
<tr>
<td>I/O Activity</td>
<td></td>
</tr>
<tr>
<td>Clock (MHz)</td>
<td>Enter the clock frequency of the domain. It supports a maximum frequency of</td>
</tr>
<tr>
<td></td>
<td>up to 300 MHz.</td>
</tr>
<tr>
<td>Data Rate</td>
<td>For I/Os used as clocks, select clock as Data Rate. For others, select data</td>
</tr>
<tr>
<td>Toggle Rate</td>
<td>Enter the average percentage of input, output, and bidirectional pins</td>
</tr>
<tr>
<td>Output Enable</td>
<td>Enter the percentage of time output pins are enabled. For bidirectional I/O</td>
</tr>
<tr>
<td></td>
<td>s are active when the output pins are disabled.</td>
</tr>
<tr>
<td>ODT Enable</td>
<td>ODT Enable is applicable only:</td>
</tr>
<tr>
<td></td>
<td>• For DDRIO Inputs and Bidirectional pins (if they are connected for FDDR or</td>
</tr>
<tr>
<td></td>
<td>MDDR)</td>
</tr>
<tr>
<td></td>
<td>• For the standards: LPDDR, SSTL18, and SSTL15</td>
</tr>
<tr>
<td></td>
<td>• If ODT is enabled</td>
</tr>
</tbody>
</table>

For more information about the I/Os of the supported device families, refer to [RTG4 FPGA Fabric User Guide](#).
Built-in Blocks

Design specific information for built-in blocks (SERDES and FDDR) are entered to calculate the dynamic power. This section contains the following subsections:

- "SERDES" on page 23
- "FDDR" on page 25

SERDES

The RTG4 devices have up to 6 SERDES blocks (2 PCIeSS and 4 NPSS). It depends on the device selected. Each row in the SERDES worksheet represents a single (X1) or multiple (X2/X4) SERDES lane.

Enter the following parameters for each SERDES block:

- Name
- Location
- Protocol
- Number of Lanes
- Speed (Gbps)
- PCIe F AXI/AHB (MHz)
- Data Rate (Mbps)

Figure 13 shows the SERDES worksheet.
Table 11 shows the parameters to be entered in the SERDES worksheet.

**Table 11 • SERDES Worksheet Parameters**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Enter a name for each SERDES block. Name is optional. Each SERDES block can be configured as X1, X2, or X4 lanes. Configurations can be:</td>
</tr>
<tr>
<td></td>
<td>• Four X1s</td>
</tr>
<tr>
<td></td>
<td>• two X2s, or</td>
</tr>
<tr>
<td></td>
<td>• single X4</td>
</tr>
<tr>
<td></td>
<td>Depending on the configuration of lanes in SERDES block, the number of rows varies.</td>
</tr>
<tr>
<td>Location</td>
<td>Select the SERDES location. Each SERDES can use up to 4 lanes and it depends on the device selected.</td>
</tr>
<tr>
<td></td>
<td>When NPSS is selected, only non PCIe protocols (XAUI and EPCS) are available in the protocol column.</td>
</tr>
<tr>
<td></td>
<td>When PCIESS is selected, all protocols (PCIe, XAUI, and EPCS) are available.</td>
</tr>
<tr>
<td>Protocol</td>
<td>Select the protocol. It supports PCIe, XAUI, and EPCS protocols.</td>
</tr>
<tr>
<td></td>
<td>Figure 14 shows the supported speed list when EPCS protocol is chosen.</td>
</tr>
<tr>
<td></td>
<td>Custom speed and data width can be selected from the Data Rate (Mbps) drop-down list. VCO Rate and FPGA Interface Frequencies are populated based on the data rate selected.</td>
</tr>
<tr>
<td>Number of Lanes</td>
<td>Select the number of lanes. It supports X1, X2, and X4.</td>
</tr>
<tr>
<td>Speed (Gbps)</td>
<td>Select the data rate for the selected protocol.</td>
</tr>
<tr>
<td>PCIe F AXI/AHB (MHz)</td>
<td>Enter the clock frequency of the AXI/AHB interface. It supports a maximum frequency of up to 200 MHz.</td>
</tr>
<tr>
<td>Data Rate (Mbps)</td>
<td>Select the custom speed and data width. This field is enabled only when EPCS protocol is selected.</td>
</tr>
<tr>
<td>Reference Clock Frequency (MHz)</td>
<td>This is a fixed value for all protocols except EPCS custom speed. In this case, enter any value between 100 MHz and 160 MHz.</td>
</tr>
<tr>
<td>VCO Rate (MHz)</td>
<td>Read-only fixed value for all protocols except EPCS custom speed. The displayed values is computed and updated based on the Reference Clock Frequency and Data Rate.</td>
</tr>
</tbody>
</table>

![Figure 14 • Custom EPCS Speed](image-url)
For more information about the SERDES of the supported device families, refer to *RTG4 FPGA High Speed Serial Interfaces User Guide*.

**FDDR**

*Figure 15* shows the FDDR Power section in the *FDDR* worksheet. Enter the following parameters for FDDR:

- **Name**
- **F AXI/AHB (MHz)**
- **DDR Clock Multiplier**

*Table 12* shows the parameters to be entered in the FDDR Power section of the *FDDR* worksheet.

**Table 12 • FDDR Power Section Parameters**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Enter the name of the module containing FDDR.</td>
</tr>
<tr>
<td>F AXI/AHB (MHz)</td>
<td>Enter the clock frequency of AXI/AHB interface. It supports a maximum frequency of up to 200 MHz.</td>
</tr>
</tbody>
</table>
| DDR Clock Multiplier | Select the frequency multiplication factor of DDR.  
                        | DDR clock frequency (FDDR_CLK) must be less than 334 MHz (for example, if F AXI/AHB is 167, DDR clock multiplier must not be more than F AXI/AHB*2). |

For more information about FDDR, refer to *RTG4 FPGA High Speed DDR Interfaces User Guide*.

**Step - 3: Scenarios**

In this section, enter the device operational modes during its operational time, for instance, 50% of the time Active and 50% in Standby. Enter the percentage of time the device is expected to be in Active and Standby modes. This section is available in the *Summary* worksheet. It is optional to provide these details.

*Figure 16* shows the **Modes and Scenarios** section in the *Summary* worksheet.
Step - 4: Power Estimation Summary

The Power Summary section provides the total power and power breakdown based on the power sources and rails. It also provides the Thermal Margin (Maximum Ta and Maximum Power) summary. Figure 17 shows Current Summary, Power Summary, and Modes and Scenarios sections in the Summary worksheet.

Table 13 shows the acceptable rail voltage range.

Table 13 • Acceptable Rail Voltage Range

<table>
<thead>
<tr>
<th>Rail Name</th>
<th>Voltage Range (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
</tr>
<tr>
<td>VDD</td>
<td>1.14</td>
</tr>
<tr>
<td>VDDI 1.2</td>
<td>1.14</td>
</tr>
<tr>
<td>VDDI 1.5</td>
<td>1.425</td>
</tr>
<tr>
<td>VDDI 1.8</td>
<td>1.71</td>
</tr>
<tr>
<td>VDDI 2.5</td>
<td>2.375</td>
</tr>
<tr>
<td>VDDI 3.3</td>
<td>3.15</td>
</tr>
<tr>
<td>SERDES_[01]_L[0123]_VDDAIIO</td>
<td>1.14</td>
</tr>
<tr>
<td>SERDES_[01]_L[0123]_VDDAPLL</td>
<td>2.375</td>
</tr>
<tr>
<td>PLL_VDDA (3.3 V)</td>
<td>3.135</td>
</tr>
</tbody>
</table>

1. PLL Analog Supply includes SERDES_x_PLL_VDDA (x: 0 to 6), FDDR_x_PLL_VDDA (x: 0 to 2) and CCC_x_PLL_VDDA (x = NE0, NE1, NW0, NW1, SW0, SW1, SE0, SE1).
Figure 18 shows the Device Utilization section displayed at the bottom of the Summary worksheet.

![Device Utilization Section](image)

Figure 18 • Device Utilization Section

Figure 19 shows the Errors section in the Summary worksheet.

![Errors Section](image)

Figure 19 • Errors Section
### A – List of Changes

The following table lists critical changes that were made in each revision.

<table>
<thead>
<tr>
<th>Date</th>
<th>Changes</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revision 1 (January 2015)</td>
<td>Initial release.</td>
<td>NA</td>
</tr>
</tbody>
</table>
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