AN08 Surface-mount QFN Package – Handling and Assembly

Use of the plastic QFN (JEDEC MO-220 quad flat no-lead) package now constitutes a major portion of packaged IC applications. The QFN with exposed thermal paddle is a compact, reliable, inexpensive plastic package with excellent RF and thermal characteristics. However, due to the small size and tight assembly tolerance of this package, proper handling and assembly is required to optimize reliability and performance.

QFN Handling

Be sure to handle QFNs only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling; do not handle QFN's with fingers as this can contaminate the package lands and interfere with solder reflow.

Maintain the QFNs in the original packaging until ready for use. Small, thin plastic packages are susceptible to moisture-related cracking during assembly if the parts are allowed to absorb an appreciable amount of moisture; maintain the parts in an environment of <10-20% humidity if possible. If the parts arrive packaged with desiccant packets, keep the packaging tight by folding or taping it. This will greatly extend the effectiveness of the desiccant. Moisture sensitivity level (MSL) definitions for typical package sizes are shown in *Table 1.*

Table 1 · Package Size

Package Size	Change	Effect
3 x 3 mm (16L VQFN)	1	Unlimited humidity exposure 30C 85% RH
4 x 4 mm (24L VQFN)	2	One year maximum exposure 30C 60% RH
6 x 6 mm (40L VQFN)	3	One week maximum exposure 30C 60% RH
10 x 10 mm (72L VQFN)	4	Three days maximum exposure 30C 60% RH

Board Design

The QFN package with exposed paddle (EP) depends upon good thermal contact between the paddle and the PC board heatsink. The heatsink is integrated into the PC board as a top thermal pad and an array of thermal vias connecting to one or more ground planes, which act as heat spreaders. This is shown schematically in the side view illustration in *Figure 1*.

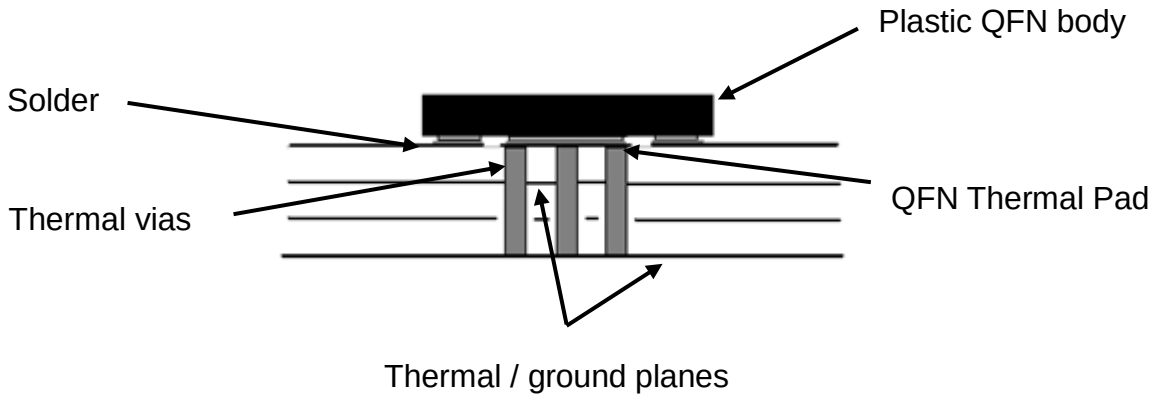

Figure 1. QFN Side View

The recommended package land layout is provided in the individual product datasheets. Use of small or filled vias under the thermal paddle prevents wicking of the solder from under the part; open vias larger than .010" - .012" in diameter will wick solder away from the PC board thermal pad and should be avoided.

Solder Attach

The need for good solder attach of the exposed thermal paddle adds some requirements to the solder paste / attach / reflow process[2,3]. To achieve the required >90% filling of the solder area under the thermal paddle, use a screen print that fills about 60-80% of the PC board land area.

Printed paste thickness can be adjusted to achieve complete solder filling of the thermal paddle area after reflow while avoiding excess solder or shorts in the I/O pad areas. The part should stand off of the PC board about .001" - .002" to provide strain relief from thermal mismatch-related stress while still providing a good heatsink for the thermal paddle.

Parts should be placed using automated placement equipment. Reflow is performed using a programmable IR ramp / soak. Manual reflow is not recommended due to the difficulty of controlling the temperature profile.

Microsemi QFNs are Pb-free and compatible with either Sn/Pb or Pb-free assembly techniques. After paste print and part placement, solder attach is achieved by ramping the part to pre-heat, thermal soak, solder reflow and then cool as shown in *Table 2* and *Table 4* , and *Figure 2* for Pb-free solder attach, or in *Table 2* and *Table 3*, and *Figure 2* for Sn/Pb solder attach. Use of a no-clean (NC) flux is required since removal of all flux under the QFN is very difficult.

Table 2 · Soldering Reflow Profiles, (per IPC/JEDEC J-STD-020D.1[4], Table 5-2)

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 150°C 200°C 60-120 seconds	 150°C 200°C 60-120 seconds
Ramp-up rate (T_L to T_p)	3°C/second max	3°C/second max
Liquidous temperature (T_L)	183°C	217°C
Peak package body temperature (T_p)	For users, T_p must not exceed the temperature in *Table 3* . For suppliers, T_p must equal or exceed the temperature in *Table 3* .	For users, T_p must not exceed the temperature in *Table 4*. For suppliers, T_p must equal or exceed the temperature in *Table 4*.
Time (t_p)[1] within 5°C of the	20[1] seconds	30[1] seconds
Ramp-down rate (T_p to T_L)	6°C/second max	6°C/second max
Time 25°C to peak	6 minutes max	8 minutes max

1. Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
2. All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), T_p shall be within ± 2°C of the live-bug T_p and still meet the T_c requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperature, refer to JEP140 for recommended thermocouple use.
3. Reflow profiles in this document are for classification/preconditioning and are not mean to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters given above.

   For example, if T_c is 260°C and time t_p is 30 seconds, this means the following for the supplier and the user.

   For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.

   For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.
4. The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processer reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Table 3 · SnPb Eutectic Process – Reflow Peak Temperature (Tc)

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	235°C	220°C
≥ 2.5 mm	220°C	220°C

Table 4 · Pb-Free Process – Reflow Peak Temperature (Tc)

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 ≥ 2000
< 1.6 mm	260°C (see note 5)	260°C (see note 5)	260°C (see note 5)
1.6 mm – 2.5 mm	260°C (see note 5)	250°C	245°C
≥ 2.5 mm	250°C	245°C	245°C

5. Note: Microsemi recommends maximum soldering reflow peak temperature of no greater than 250°C.

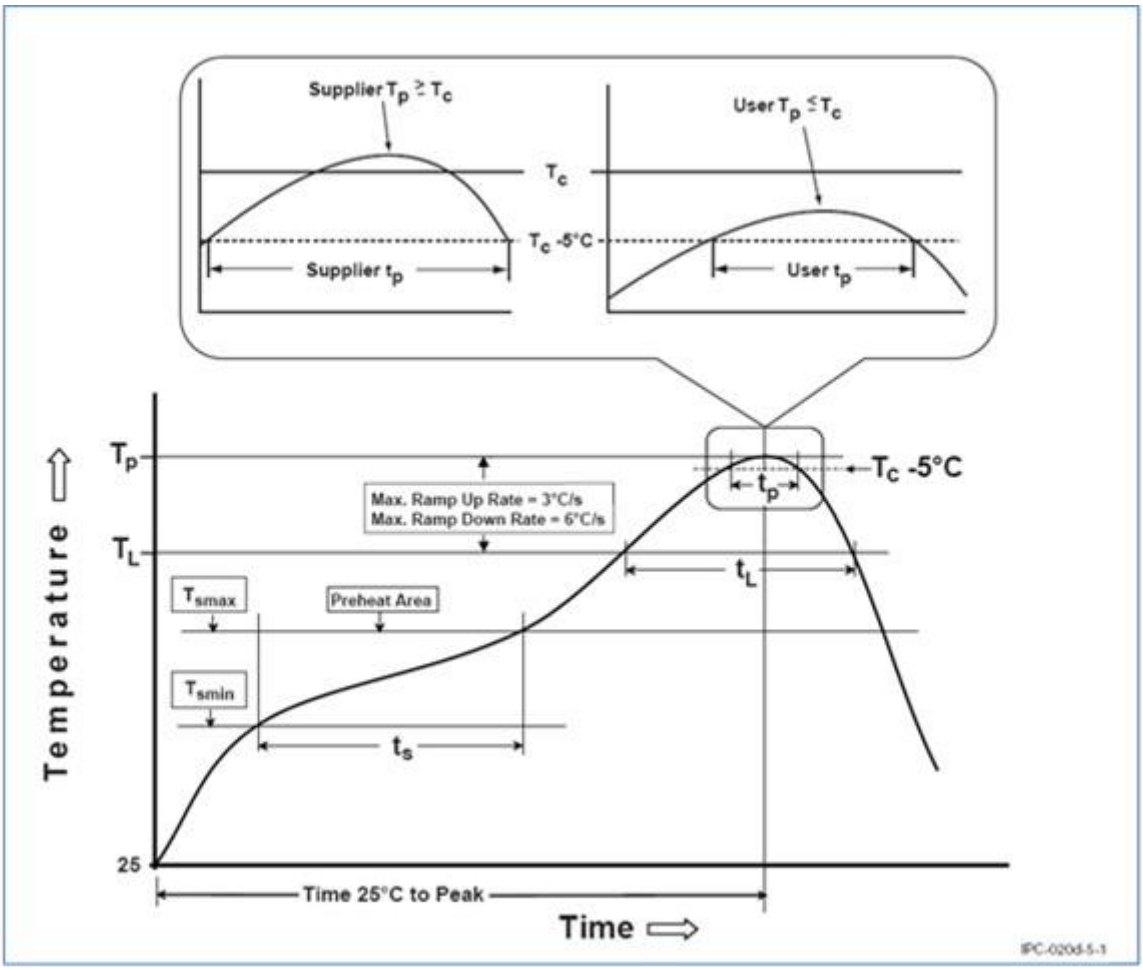

Figure 2. Soldering reflow profile

Thermal Considerations

The electrical performance and reliability of the QFN are highly dependent upon the PC board heatsink design[5,6] efficient removal of heat from the exposed paddle is required to maintain the device below the absolute maximum operating temperature as specified in the product datasheet.

To estimate the device channel or junction temperature (T_J) a thermal model is constructed as shown in *Figure 3*.

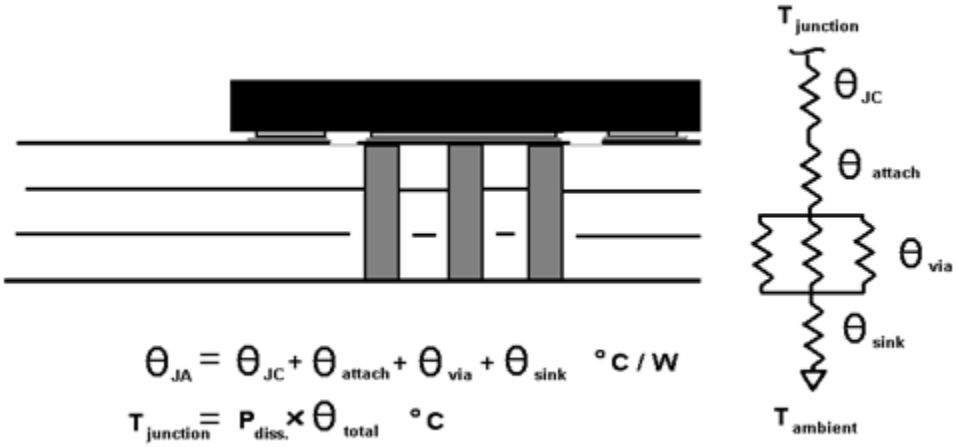

Figure 3. PC board heatsink thermal model

Each thermal resistance is estimated or calculated, and then combined together to calculate the total thermal resistance from the device junction to ambient: The device thermal resistance, Θ_{JC} is provided on the product datasheet. Θ_{attach} is calculated from the thermal conductivity, attach area and thickness of the solder attach; Θ_{attach} = thickness / (cond. x area).

Similarly, Θ_{via} is calculated using the thermal conductivity of the copper wall, the cross-sectional area and the height of one via. Combine the result for n vias in parallel by dividing the resulting thermal resistance for a single via by n.

Finally, the thermal resistance of the PC board to an additional heat sink, Θ_{sink} is estimated. The total thermal resistance to ambient, Θ_{JA} is the series / parallel combination of each of the thermal resistances shown in *Figure 3*.

Typical values of Θ_{JA} range from ~ 20 - 30ºC / W depending upon the IC size and material, the number and diameter of thermal vias, and the size, thickness and number of thermal ground planes in the PC board. Typical absolute maximum junction temperatures, T_j are 125-150ºC.

So for example a QFN may dissipate 1W to a PC board backside maintained at 85ºC and still readily meet the requirement to remain below 125ºC (85ºC + 30ºC/W x 1W = 115ºC).

Accurate knowledge of Θ_{JA} is especially important for QFN devices which dissipate 2 watts or more; for these devices, an ambient temperature of 60ºC at the board backside can easily lead to T_j ~ 125ºC or more. In these cases, careful consideration of the thermal environment is required, and an additional heatsink may be needed below the PC board to maintain a more stable ambient for higher power dissipation.

References:

1. JESD22-A112: Preconditioning of Non-Hermetic Surface-Mount Devices Prior to Reliability Testing
2. Application Note: “Application Notes for Surface Mount Assembly of Amkor’s Thermally / Electrically Enhanced Leadframe Based Packages” Amkor Technology, December, 2001
3. Product Note: “Board Level Assembly and Reliability Considerations for QFN Type Packages” Amkor Technology

4. IPC/JEDEC J-STD-020D.1: Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
5. JESD51-3: Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
6. JESD51-7: High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

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