UG0594
User Guide
SmartFusion2 Security Evaluation Kit

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Power Matters.™

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

- In Figure 3, page 8, corrected the Bank 5 and Bank 7 voltage (VDDI).
- Added a new section ETM Trace Header, page 16.

1.2 Revision 3.1

Libero SoC software license information was updated from Platinum to Gold. For more information, see Table 1, page 2 and Software Settings, page 6.

1.3 Revision 3.0

The following was a summary of the changes in revision 3.0 of this document.

- Throughout the document, figures were updated in accordance with revision E of the SmartFusion2 M2S090TS-EVAL-KIT.
- Information about jumper settings was updated. For more information, see Jumper Settings, page 6 and Validating Power Supply, page 41.
- Information about the LPDDR SDRAM interface was updated. For more information, see LPDDR SDRAM, page 11.
- Information about programming the device for the manufacturing test was updated. For more information, see Programming the FPGA Using Embedded FlashPro5, page 41.

1.4 Revision 2.0

Updated LPDDR resolution changes (SAR 52540, SAR 57285, SAR 61490, SAR 53271).

1.5 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Introduction

The RoHS-compliant SmartFusion®2 SoC FPGA Security Evaluation Kit (M2S090TS-EVAL-KIT) enables you to develop the following types of applications:

- Data security
- Motor control
- System management
- Industrial automation
- High-speed serial I/O applications:
  - Peripheral component interconnect express (PCIe)
  - Serial-gigabit media independent interface (SGMII)
  - User-customizable serial interfaces

2.1 Kit Contents

The following table lists the contents of the M2S090TS-EVAL-KIT.

Table 1 • **Kit Contents**

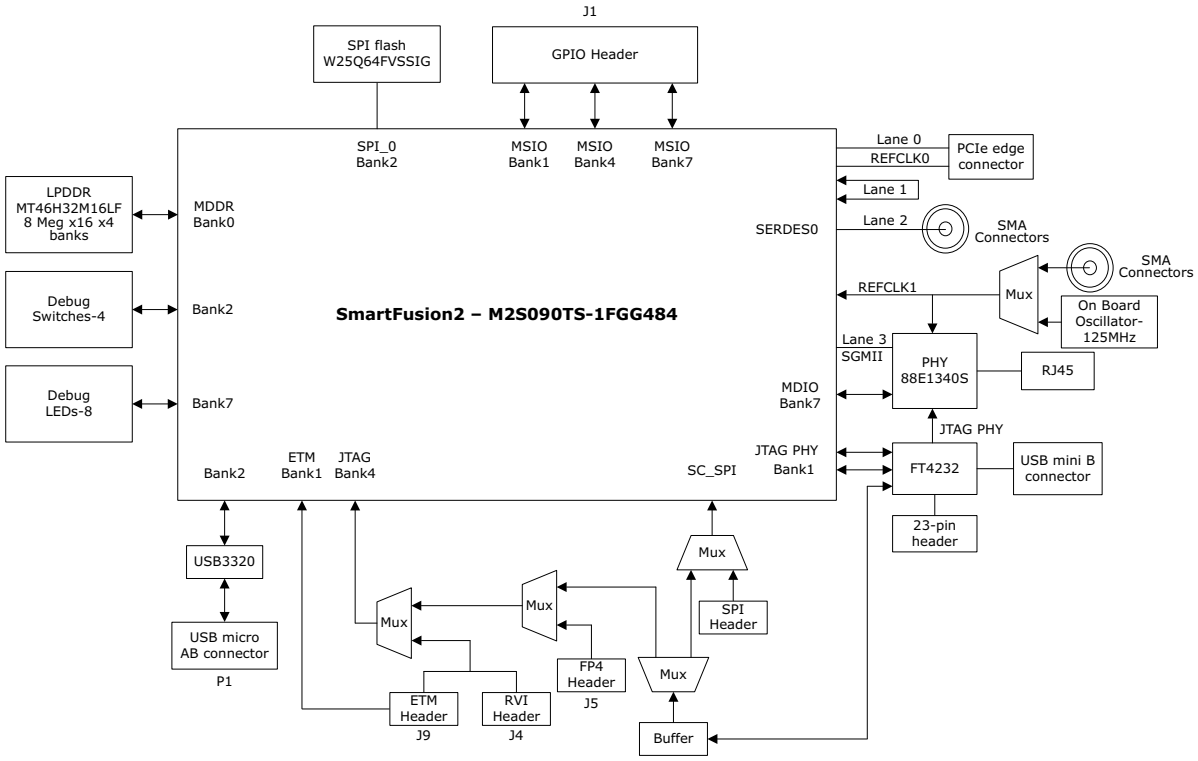
Item	Quantity
SmartFusion2 Security Evaluation Board with the 90 K LE M2S090TS-1FGG484 device	1
12 V/2 A wall-mounted power adapter	1
FlashPro4 JTAG programmer	1
USB 2.0 A male to mini-USB B cable for UART/power interface (up to 1 A) to PC	1
Quickstart card	1
Free one-year Libero SoC Gold software license	1
PCIe control plane demo design pre-programmed on the device	1

Note: The SmartFusion2 device can be programmed either using the on-board SPI slave (FlashPro5) programmer or using the external FlashPro4 programmer. SoftConsole debugging cannot be performed in SPI slave mode. FlashPro4 is required to develop and debug embedded applications using SoftConsole, Identity, or SmartDebug.

2.2 Block Diagram

The following figure is the block diagram of the SmartFusion2 Security Evaluation Kit.

Figure 1 • **SmartFusion2 Security Evaluation Kit Block Diagram**



2.3 Web Resources

For more information about the M2S090TS-EVAL-KIT, see *www.microsemi.com/products/fpga-soc/design-resources/dev-kits/SmartFusion2/smartfusion2-evaluation-kit#overview*.

2.4 Board Description

The M2S090TS-EVAL-KIT offers a full-featured evaluation board for SmartFusion2 SoC FPGAs. The board integrates the following features on a single chip.

- Reliable flash-based FPGA fabric
- 166 MHz ARM Cortex-M3 processor
- Advanced security processing accelerators
- Digital signal processing (DSP) blocks
- Static random-access memory (SRAM)
- Embedded non-volatile memory (eNVM)
- High-performance communication interfaces

The SmartFusion2 Security Evaluation Board has several standard interfaces, including.

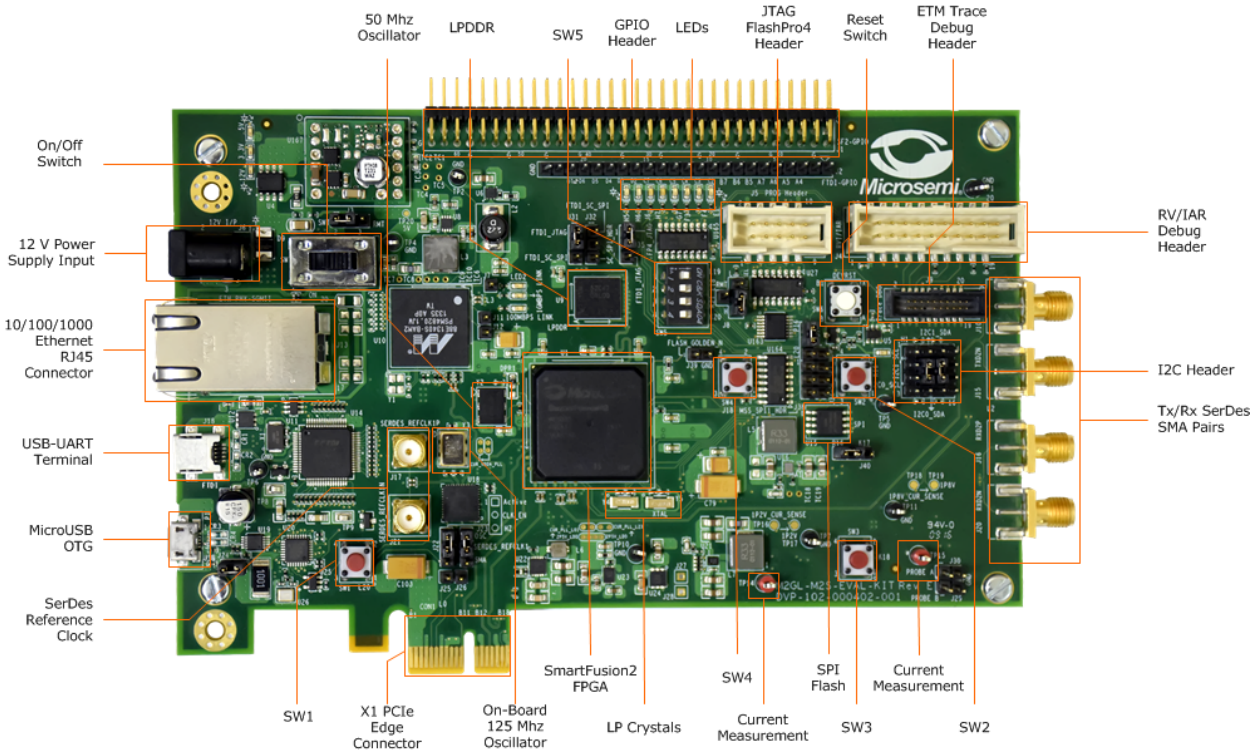
- An RJ45 connector for 10/100/1000 Mbps Ethernet
- A full-duplex serializer/deserializer (SerDes) lane connected through sub-miniature version A (SMA) connectors
- A 64-bit GPIO header
- Various connectors for serial peripheral interface (SPI) support

The SmartFusion2 memory management system supports 512 Mb on-board low-power double data rate (LPDDR) SDRAM memory and 64 Mb SPI flash memory. The SerDes block can either be accessed using the PCIe edge connector or using high-speed SMA connectors.

The printed circuit board (PCB) supports the M2S090TS device in an FGG484 package. It has eight layers and is manufactured with FR4 dielectric material.

The following figure is a snapshot of the SmartFusion2 Security Evaluation Board with its engineering silicon.

Figure 2 • **SmartFusion2 Security Evaluation Board**



Note: Microsemi recommends using a 12-inch SMA Male to SMA Male Precision Cable using the RoHS-compliant PE-SR405FLJ coax with the SmartFusion2 Security Evaluation Kit. For more information, see *www.pasternack.com/sma-male-sma-male-pe-sr405flj-cable-assembly-pe39429-12-p.aspx*.

2.5 Board Key Components

The following table lists key components of the SmartFusion2 Security Evaluation Kit.

Table 2 • **SmartFusion2 Security Evaluation Kit Components**

Name	Description
SmartFusion2 FPGA	M2S090TS-1FGG484 FPGA with data security feature.
On-board 125 MHz clock oscillator	125 MHz clock oscillator with differential output.
x1 PCIe edge connector	PCIe edge connector with one lane.
Switches (SW1, SW2, SW3, and SW4)	Push-button switches for user interface debugging applications.
SerDes reference clock connectors	J17 and J21. External clock is sourced through SMA connectors.
Micro-USB OTG	P1. Micro-AB USB connector, interfacing with the high-speed USB 2.0 ULPI transceiver chip, USB3320, which, in turn, interfaces with FPGA pins of the SmartFusion2 MSS.

Table 2 • **SmartFusion2 Security Evaluation Kit Components *(continued)***

Name	Description
USB-UART terminal	J18. FTDI programmer interface to program the external SPI flash.
10/100/1000 Ethernet RJ45 connector	J13. RJ45 connector (Ethernet jack with built-in magnetics) interfacing with Marvell 10/100/1000 BASE-T PHY chip, 88E1340S, in SGMII mode. 88E1340S, which, in turn, interfaces with the Ethernet port of the SmartFusion2 MSS (on-chip MAC and external PHY).
12 V power supply input	J6. The board is powered by a 12 V power source using an external +12 V/2 A DC jack.
On/Off switch	SW7. Power ON or OFF switch from +12 V external DC jack.
50 MHz oscillator	50 MHz clock oscillator.
Low-power DDR (LPDDR)	512 Mb (MT46H32M16LF - 8 Meg × 16 × 4 banks) for storing data bits.
GPIO header	J1. General purpose input/output (GPIO) header for multi-standard I/O (MSIO) signals to be routed.
SW5	Four DIP switches for testing and navigation.
Light-emitting diodes (LEDs)	Eight active-low LEDs connected to some of the user I/Os for debugging, and three active high LEDs used for indicating power supply.
JTAG programming header	J5.The SmartFusion2 device in the evaluation kit can be programmed using FlashPro4. J5 is the programming header for FlashPro4 to program and debug the SmartFusion2 device.
Reset switch	SW6. Push-button system reset for the SmartFusion2 device.
Embedded trace macro (ETM) debug header	J9. ETM header for debugging.
RVI/IAR debug header	J4. RVI header for application programming and debugging with Keil ULINK or IAR J-Link.
Tx/Rx SerDes SMA pairs	J10. SERDES0 TXD2 P. J15. SERDES0 TXD2 N. J16. SERDES0 RXD2 P. J20. SERDES0 RXD2 N.
I2C header	H1. Two I2C ports routed to header.
Current measurement	TP14. 1.2 V current sensing test point (TP).
SPI flash	64 Mb SPI flash Winbond Electronics W25Q64FVSSIG connected to SPI port 0 of the SmartFusion2 microcontroller subsystem (MSS).
LP crystals	Y4 and Y5. 32.768 KHz crystal oscillators.

3 Installation and Settings

This section provides information about the software and hardware settings required to run the pre-programmed demo design in the SmartFusion Security Evaluation Kit.

3.1 Software Settings

Download and install the latest release of Microsemi Libero® SoC software v11.5 or later from the Microsemi website, and register for a free one-year Gold license to the software. The Libero SoC v11.5 or later installer has FlashPro4 drivers. For instructions on how to install Libero SoC and SoftConsole, see the *Libero Installation and Licensing Guide*.

For instructions about how to download and install Microsemi DirectCores, SGCores, and driver firmware cores, which must be installed on the PC where Libero SoC is installed, see *Installing IP Cores and Drivers User Guide*.

3.2 Hardware Settings

This section provides information about jumper settings, switches, LEDs, and DIP switches in the pre-programmed demo design in the M2S090TS-EVAL-KIT.

3.2.1 Jumper Settings

Connect the jumpers with the settings specified in the following table to evaluate the pre-programmed demo design.

Table 3 • **Jumper Settings for Pre-Programed Demo Design**

Jumper	Description	Pin	Default Setting
J23	Jumper to select switch-side MUX inputs of A or B to the line side	Pin 1-2 (Input A to the line side) that is on board 125 MHz differential clock oscillator output will be routed to line side	Closed
		Pin 2-3 (Input B to the line side) that is external clock required to source through SMA connectors to the line side	Open
J22	Jumper to select the output enable control for the line side outputs	Pin 1-2 (line-side output enabled)	Closed
		Pin 2-3 (line-side output disabled)	Open
J24	Jumper to provide the VBUS supply to USB when using in host mode	–	Open
J8	JTAG selection jumper to select between RVI header or FlashPro4 header for application debug	Pin 1-2 FP4 for SoftConsole/FlashPro	Closed
		Pin 2-3 RVI for Keil ULINK/IAR J-Link	Open
		Pin 2-4 for toggling JTAG_SEL signal remotely using the GPIO capability of the FT4232 chip	Open
J3	Jumpers to select either the SW2 input or the ENABLE_FT4232 signal from the FT4232H chip	Pin 1-2 for manual power switching using **SW7**	Closed
		Pin 2-3 for remote power switch using the GPIO capability of the FT4232 chip	Open
J31	Jumper to select between FTDI JTAG programming and FTDI slave programming	Pin 1-2 for FlashPro FTDI JTAG programming	Closed
		Pin 2-3 for SPI slave programming	Open

Table 3 • **Jumper Settings for Pre-Programed Demo Design *(continued)***

Jumper	Description	Pin	Default Setting
J32	Jumper to select between FTDI SPI and SC_SCI header	Pin 1-2 for programming through the FTDI SPI	Closed
		Pin 2-3 for Programming through the SC_SPI header	Open
J35	Jumper to select between FP4 header and FTDI JTAG	Pin 1-2 for programming through the FP4 header	Closed
		Pin 2-3 for programming through FTDI JTAG	Open

For locations of various jumpers and test points on the SmartFusion2 Security Evaluation Board, see Figure 19, page 38 and Figure 20, page 39.

3.2.2 LEDs

The following table lists the power supply and Ethernet LEDs in the pre-programmed demo design.

Table 4 • **LEDs in the Pre-Programmed Demo Design**

LED	Description
DS1 - Green	5 V rail
DS2 - Green	3.3 V rail
DS3 - Green	12 V power source
DS5 - Green	Connected to parallel LED output port 0 (P0_LED[0]) of Marvell PHY
DS4 - Green	Connected to parallel LED output port 0 (P0_LED[2]) of Marvell PHY
DS6 - Green	Connected to parallel LED output port 0 (P0_LED[3]) of Marvell PHY

3.2.3 Test Points

The following table lists USB, ground, and other test points for the pre-programmed demo design.

Table 5 • **Test Points for the Pre-Programmed Demo Design**

Test Point	Description
TP8	USB switch I/O for DP signal
TP9	USB switch I/O for DM signal
TP1, TP2, TP4, TP5, TP6, TP7, TP10, TP11	Ground
TP3	Test point for DDR_VTT
TP12	Test point to measure the voltage at TP12 with reference to ground
TP14	1.2 V current-sensing test point
TP15	1.8 V current-sensing test point
TP16, TP17	Test points across current sense resistor 0.05 Ω for 1.2 V
TP18, TP19	Test points across current sense resistor 0.05 Ω for 1.8 V

3.3 Power Sources

All the power supply devices used in the SmartFusion2 Security Evaluation Kit are Microsemi devices. For more information about power supply devices, go to *www.microsemi.com/product-directory/ics/853-power-management*.

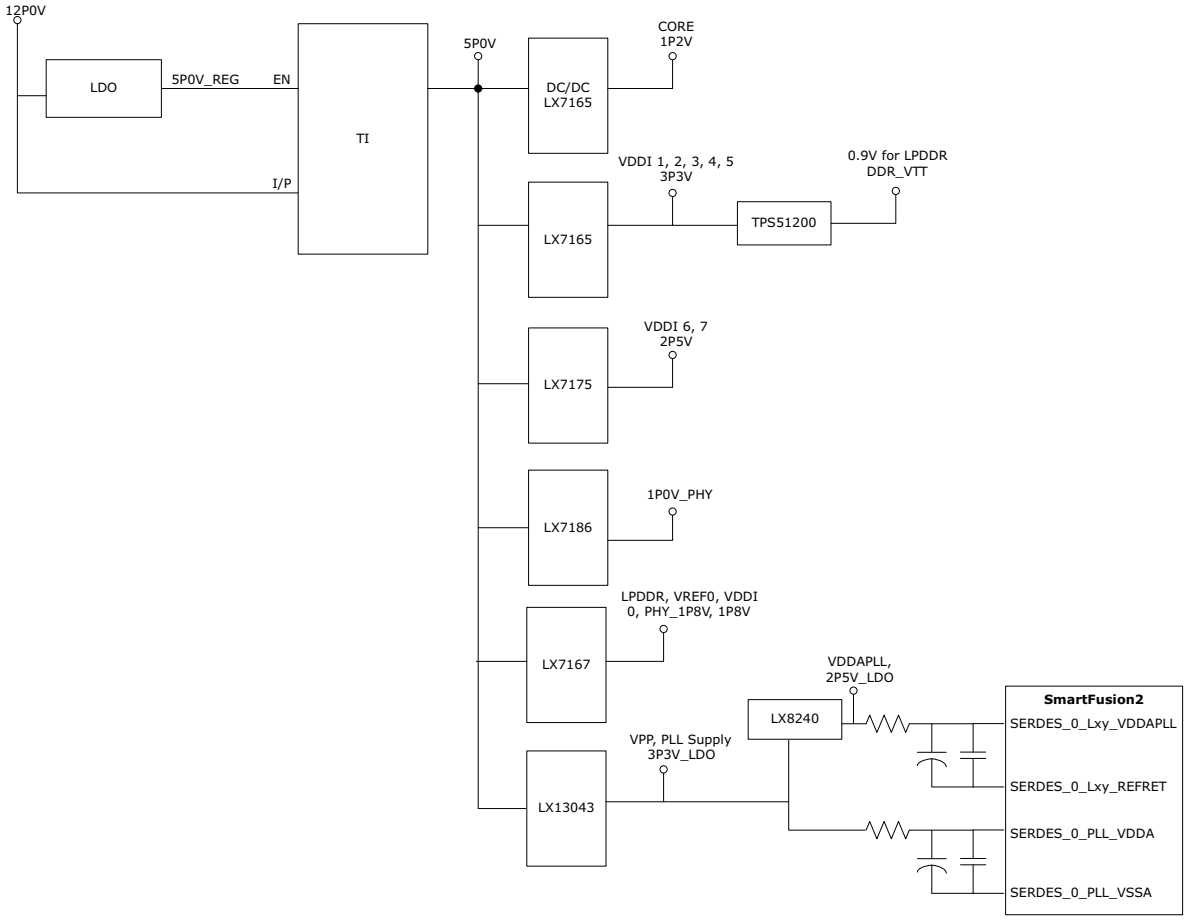
The following table lists the key power supplies required for normal operation of the SmartFusion2 Security Evaluation Kit.

Table 6 • **I/O Voltage Rails**

SmartFusion2 Bank	I/O Rail	Voltage
Bank 0	VDDI0	1.8 V
Bank 2	VDDI2	3.3 V
Bank 3	VDDI3	3.3 V
Bank 4	VDDI4	3.3 V
Bank 5	VDDI5	3.3 V
Bank 6	VDDI6	2.5 V
Bank 7	VDDI7	2.5 V
Bank 8	VDDI8	3.3 V

The following figure shows voltage rails (12 V, 5 V, 3.3 V, 2.5 V, 1.8 V, 1.5 V, and 1.0 V) available in the SmartFusion2 Security Evaluation Kit.

Figure 3 • **Voltage Rails in SmartFusion2 Security Evaluation Kit**



4 Key Components Description and Operation

This section describes the key component interfaces of the SmartFusion2 Security Evaluation Kit. For device datasheets, go to *http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/smartfusion2-kits*.

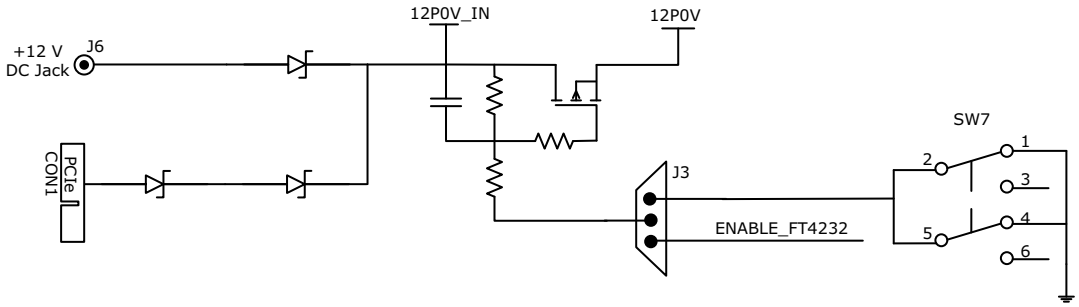
4.1 Powering Up the Board

The SmartFusion2 Security Evaluation Board is powered using either of the two 12 V power sources— the external +12 V/2 A DC jack or the PCIe connector, as shown in the following figure. Protection mechanism enables the external DC jack supply.

When both the power sources are ON, the board draws power from the external DC jack as diode D3 becomes reverse-biased and the path is let open for 12P0_PCIE. When external DC voltage is not present, the board can be powered up using the PCIe connector.

The following figure shows then power-up flow for the SmartFusion2 Security Evaluation Board.

Figure 4 • **Powering Up the Board**



4.2 Current Measurement

This section provides information about current sensing in various modes.

4.2.1 1.2 V Current Sensing for Normal Operation

For applications that require current measurement, high-precision operational amplifier circuitry (U31 with gain 100) is provided on the board to measure the output voltage at the **TP14** test point.

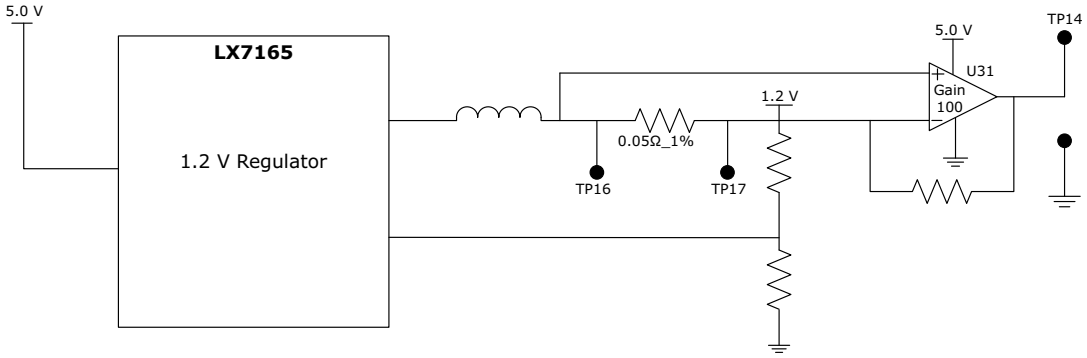
The following steps describe how to measure the core power:

1. Measure the output voltage (V_{OUT}) at TP14.
2. I = (V_{OUT}/5).
3. Core power consumed (P) = (1.2 V) × I.

For example, when the voltage measured across TP14 is 0.5 V, the core power consumed is 0.12 W.

The following figure shows the on-board core power measurement circuitry.

Figure 5 • **Core Power Measurement Circuitry**



4.2.2 1.2 V Current Sensing for Flash*Freeze

The SmartFusion2 device consumes very less power in Flash*Freeze mode. The voltage across the sense resistor (0.05 Ω) must be measured directly using a precision digital multimeter that can read sub-millivolts. The **TP16** and **TP17** test points can be used to directly measure the voltage across the 1.2 V sense resistor.

To convert the voltage measured across a sense resistor to power, use the following equation:

$$\text{Power} = \left(\frac{\text{voltage_in_millivolts}}{0.05}\right) \times 1.2$$

Note: Accuracy is ± 10%.

4.2.3 1.8 V Current Sensing

For applications that require current measurement, high-precision operational amplifier circuitry (U32 with gain 100) is provided on the board to measure the output voltage at the **TP15** test point.

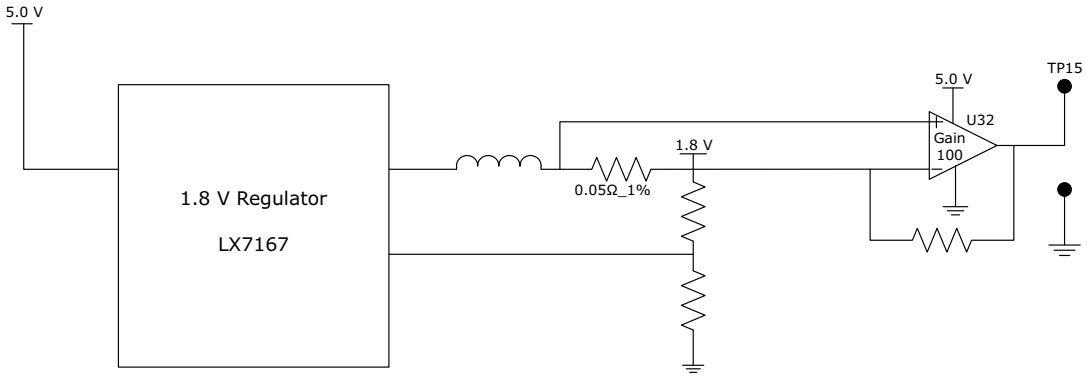
The following steps describe how to measure the core power:

1. Measure the output voltage (V_{OUT}) at TP15.
2. I = (V_{OUT}/5).
3. Core power consumed (P) = (1.8 V) × I.

For example, when the voltage measured across TP15 is 0.5 V, the power consumed is 0.18 W.

The following figure shows the on-board 1.8 V power measurement circuitry.

Figure 6 • **1.8 V Power Measurement Circuitry**

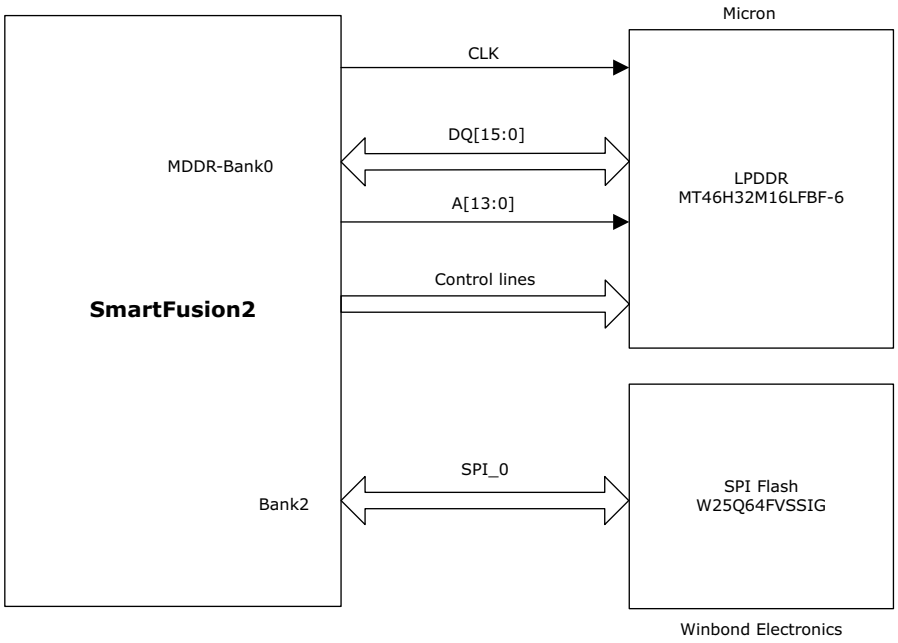


Note: Accuracy is ± 10%.

4.3 Memory Interface

Dedicated I/Os for MSS DDR and fabric DDR are available in the SmartFusion2 device. In addition to dedicated I/Os, regular I/Os can also be used to connect to other memory devices, as shown in the following figure.

Figure 7 • **SmartFusion2 Memory Interface**



4.3.1 LPDDR SDRAM

An individual chip with 512 Mb LPDDR SDRAM is provided in the SmartFusion2 device to serve as flexible volatile memory for user applications. The LPDDR interface is implemented in bank 0.

LPDDR SDRAM specifications for the SmartFusion2 device are as follows:

- MT46H32M16LF: 8 Meg × 16 × 4 banks
- Density: 512 Mb
- Data rate: LPDDR 16-bit at 166 MHz clock rate

The SmartFusion2 Security Evaluation Kit design uses the LPDDRI and LVCMOS18 standards for the LPDDR interface. The default board assembly available for the LPDDRI standard has RC terminations. The LVCMOS18 I/O standard has lower power characteristics than the LPDDRI (SSTL18) standard for the LPDDR memories. To achieve low power characteristics (LPDDR in LVCMOS18 mode), change the I/O type in the design example to LVCMOS18.

For more information, see the Board Level Schematics document (provided separately).

4.3.2 SPI Serial Flash

SPI flash specifications for the SmartFusion2 device are as follows:

- Density: 64 Mb
- Voltage: 2.7 V to 3.6 V
- Frequency: 104 MHz
- SPI mode support: Modes 0 and 3
- SmartFusion2 MSS: SPI0 interfaced to SPI flash

For more information, see the Board Level Schematics document (provided separately).

4.4 SERDES0 Interface

The SERDES0 interface has four lanes, connected as follows:

1. Lane 0 is directly routed to the PCIe connector.
    - TX pad > trace > AC coupling > trace > via (to bottom layer) > trace > PCIe connector pad
    - RX pad > trace > PCIe connector pad
2. Lane 1 is used for loopback testing. This path is routed between the TX and RX pads with a 6-inch trace and two vias.
    - TX pad > via (to bottom layer) > trace > AC coupling > trace > via (to top layer) > RX pad
3. Lane 2 is routed to SMA connectors.
    - TX pad > trace > AC coupling > trace > SMA connector pad
    - RX pad > trace > via (to bottom layer) > trace > via (to top layer) > SMA connector pad
4. Lane 3 is routed to Marvell PHY 88E1340S.
    - TX pad > trace > AC coupling > trace > via > trace routed in sixth layer > via (to top layer) > Marvel PHY pin
    - RX pad > via > trace routed in sixth layer > via (to top layer) > trace > AC coupling > trace > Marvel PHY pin

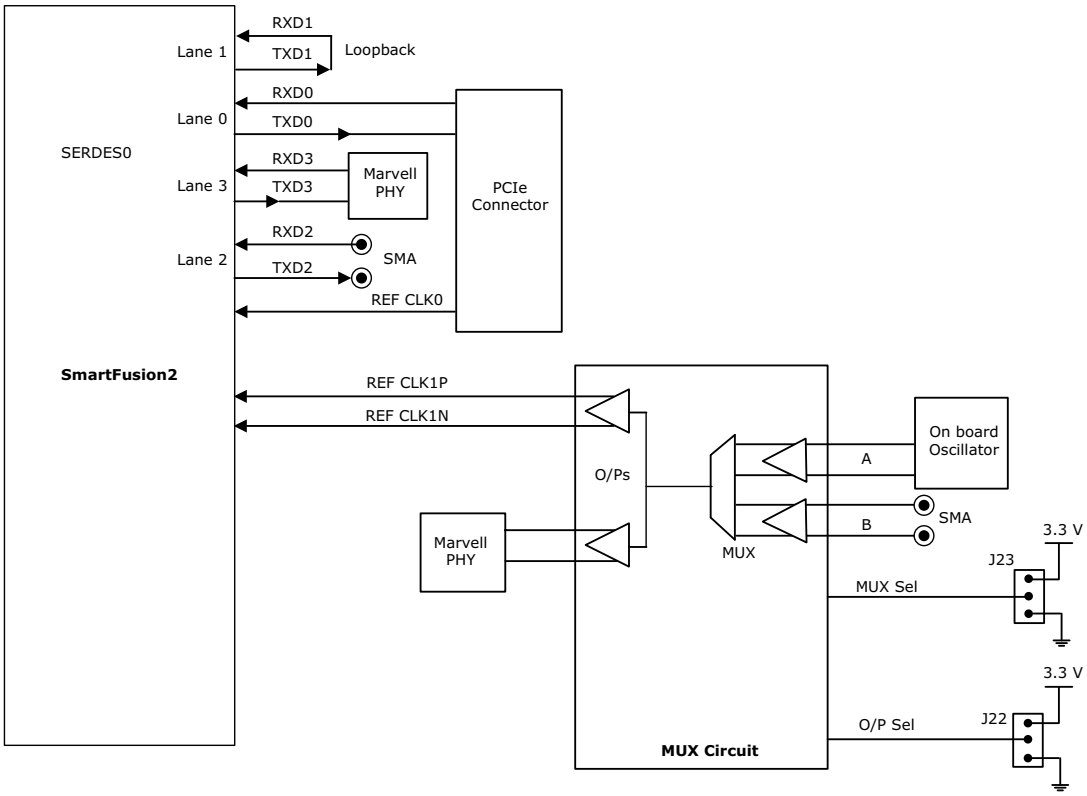
SERDES0 reference clock 0 is routed directly from the PCIe connector to the SmartFusion2 device. SERDES0 reference clock 1 is routed from the on-board 125 MHz clock oscillator, and optionally routed from SMA connectors through an LVDS MUX or buffer chip.

The expected SerDes reference clock specifications are as follows:

- Voltage level: 3.3 (± 0.3) V
- Differential LVDS
    - Symmetry: 50% (± 10%)
    - Rise/fall time: Maximum 1 ns @ 20% to 80% of supply (3.3 V)
    - Output Voltage Levels: 0 = 0.90 minimum, 1.10 typical; 1 = 1.43 typical, 1.60 maximum
    - Differential output voltage: 247 mV minimum, 454 mV maximum

The following figure shows the SERDES0 interface of the SmartFusion2 Security Evaluation Board.

Figure 8 • **SERDES0 Interface**



For information about the **J22** and **J23** jumpers, see Table 3, page 6.

Notes:

- SERDES0 TXD pairs are capacitively coupled to the SmartFusion2 device. Serial AC-coupling capacitors are used to provide common-mode voltage independence.
- AC-coupling capacitors are not provided for SERDES0 RXD signals. The mating board must have the AC-coupling capacitors.

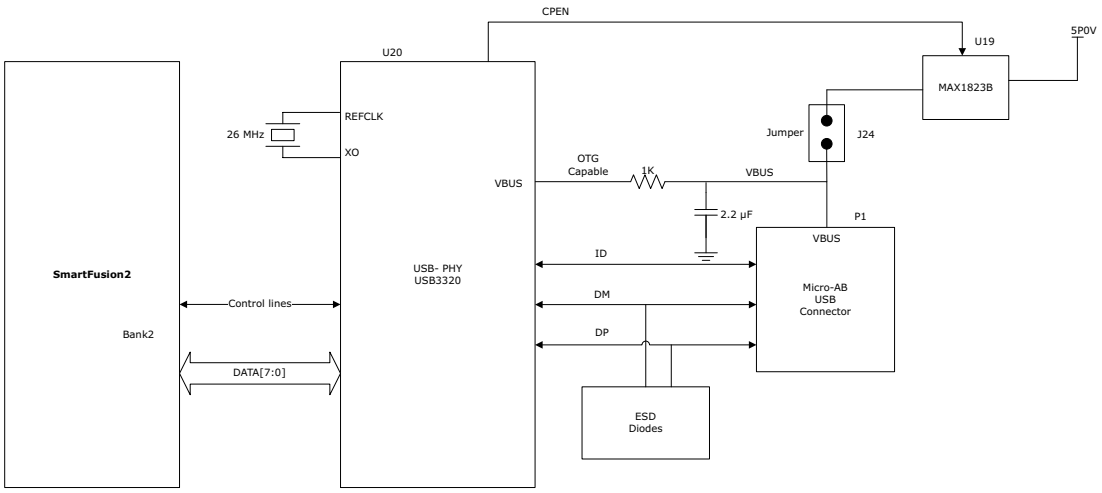
For more information, see the Board Level Schematics document (provided separately).

4.5 USB Interface

The following figure shows the USB interface of the SmartFusion2 Security Evaluation Board. The SMSC USB3320 shown in the figure is a high-speed USB 2.0 ULPI transceiver that supports the optional OTG protocol.

The following figure shows the USB interface of the SmartFusion2 Security Evaluation Board.

Figure 9 • **USB Interface**



For more information, see the Board Level Schematics document (provided separately).

4.6 Marvell PHY (88E1340S)

The SmartFusion2 Security Evaluation Kit uses Marvell Alaska physical layer (PHY) device 88E1340S for Ethernet communications at 10/100/1000 Mbps. Device 88E1340S has four independent gigabit Ethernet transceivers; however, the board uses only one of the transceivers. Each transceiver performs all the PHY functions for 10BASE-T, 100BASE-TX, and 1000BASE-T full-duplex or half-duplex Ethernet on a CAT5 twisted-pair cable. The PHY device is connected to a user-provided Ethernet cable through an RJ45 connector with built-in magnetics.

Device 88E1340S supports Quad SGMII for direct connection to a SmartFusion2 chip. It is configured through the CONFIG [3:0] and CLK_SEL [1:0] registers.

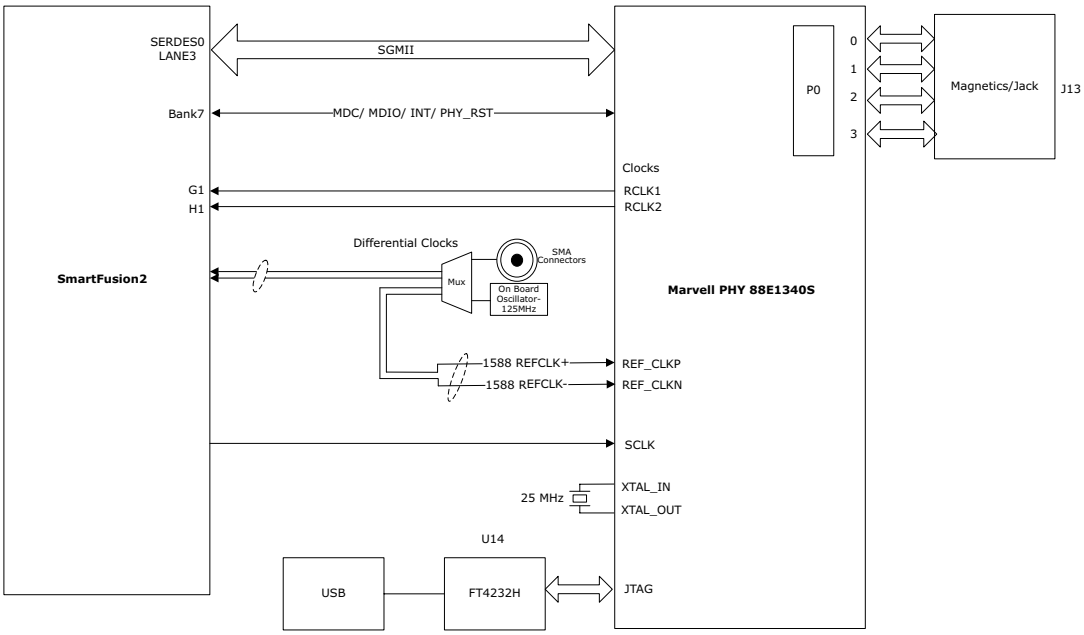
The CLK_SEL [1:0] register is used to select the reference clock input option. On the board, the status of the CLK_SEL0 register is *high* and the status of CLK_SEL1 is *low*. REF_CLK is the 125 MHz reference differential clock input. It consists of LVDS differential inputs with a 100 Ω differential internal termination resistor.

Key features of Marvell PHY 88E1340S are as follows:

- RCLK: Gigabit recovered clock
- SCLK: 25 MHz synchronous input reference clock
- Expected reference clock (REF_CLK) specifications:
  - Voltage level: 3.3 (± 0.3) V
  - Differential LVDS
    - Symmetry: 50% (± 10%)
    - Rise/fall time: Maximum 1 ns @ 20% to 80% of supply (3.3 V)
    - Output voltage levels: 0 = 0.90 minimum, 1.10 typical; 1 = 1.43 typical, 1.60 maximum
    - Differential output voltage: 247 mV minimum, 454 mV maximum

The following figure shows the SmartFusion2 Marvell PHY interface.

Figure 10 • **Marvell PHY Interface**



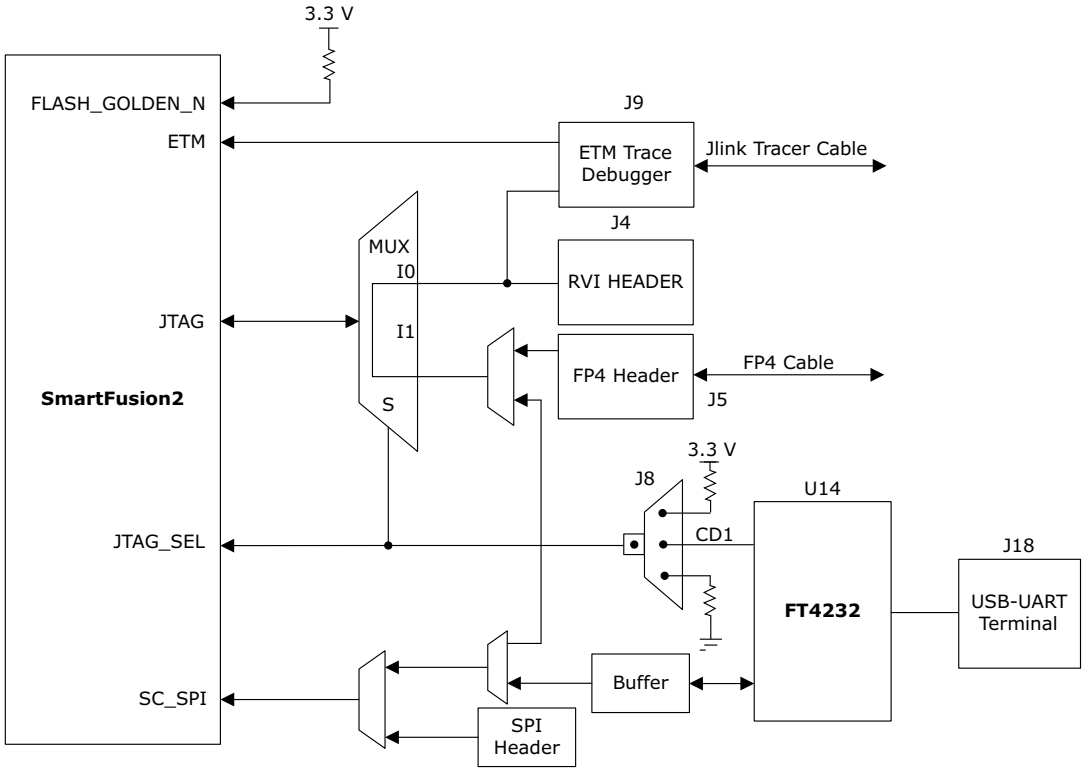
For more information, see the Board Level Schematics document (provided separately).

4.7 Programming

The SmartFusion2 device can be programmed through the SPI slave interface or the JTAG interface. The following figure shows various ways of programming the device.

See Appendix: FPGA Programming Using FlashPro4, page 68 for detailed information about how to program the device using the JTAG interface.

Figure 11 • **SmartFusion2 Programming Interface**



JTAG_SEL: JTAG_SEL is used to switch between the FlashPro4 header (high) and the RVI header or ETM header (low). For more information about the **J8** jumper, see Table 3, page 6.

RVI header: A 10 × 2 RVI header is provided on the board for debugging. This header allows plugging in the Keil ULINK debugger or IAR J-Link debugger.

FlashPro4 programming header: The SmartFusion2 device in the evaluation kit can be programmed using the on-board SPI slave (FlashPro5) or the external FlashPro4 programmer. FlashPro4 is also used for debugging the software using SoftConsole.

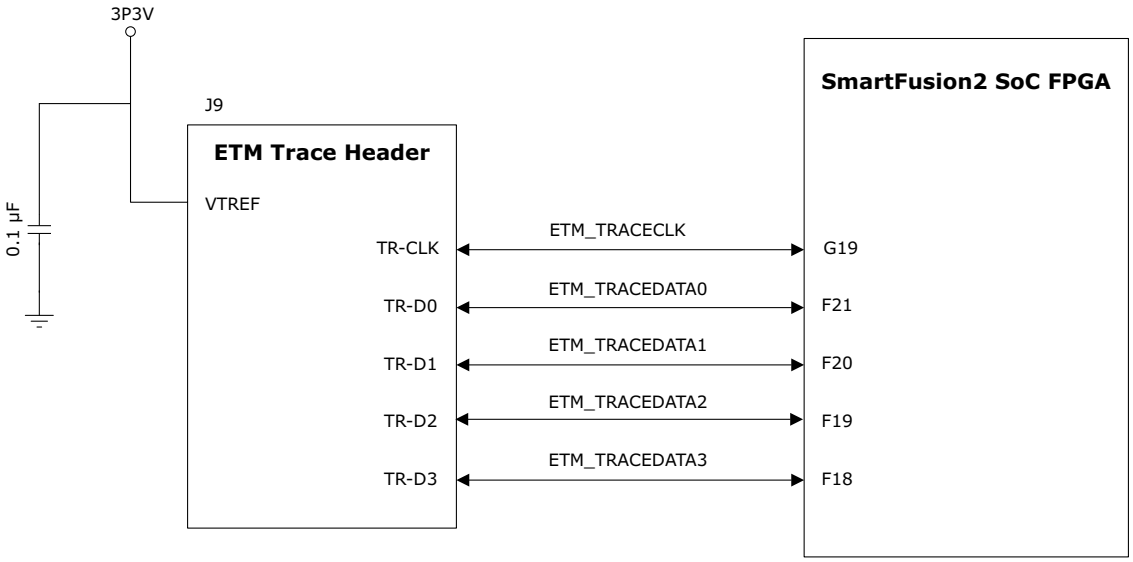
For more information, see the Board Level Schematics document (provided separately) and the *IGLOO2 and SmartFusion2 Programming User Guide.*

4.8 ETM Trace Header

The ETM trace header (J9) on the board can be used to interface a Trace debugger IDE with the Cortex-M3 processor for trace debugging.

The following figure shows the ETM header interface on the SmartFusion2 Security Evaluation Board.

Figure 12 • **ETM Trace Header Interface**



The connection of ETM Header signals is listed in the following table.

Table 7 • **Connection of ETM Trace Signals**

Board Signal Name	SmartFusion2 Pin Name	SmartFusion2 Device Pin Number
ETM_TRACECLK	MSIO55PB2/GB14/VCCC_SE1_CLKI/MMUART_1_CLK/GPIO_25_B/USB_DATA4_C	G19
ETM_TRACEDATA0	MSIO56PB2/MMUART_0_RTS/GPIO_17_B/USB_DATA5_C	F21
ETM_TRACEDATA1	MSIO56NB2/MMUART_0_DTR/GPIO_18_B/USB_DATA6_C	F20
ETM_TRACEDATA2	MSIO57PB2/MMUART_0_CTS/GPIO_19_B/USB_DATA7_C	F19
ETM_TRACEDATA3	MSIO57NB2/MMUART_0_DSR/GPIO_20_B	F18

To enable the ETM Trace header ports, the **MSS_CM3 Configurator > Expose TRACE ports to the FPGA Fabric** option must be selected in the Libero design.

For more information, see the Board Level Schematics document (provided separately).

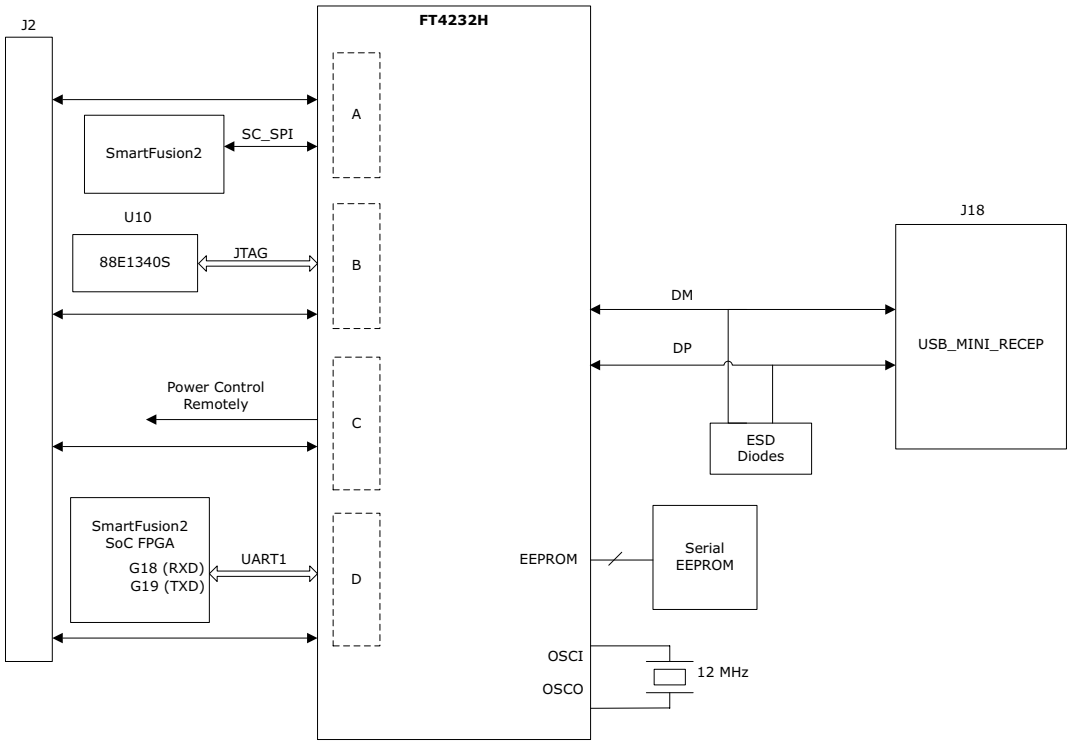
4.9 FTDI Interface

Key features of the FT4232H chip are as follows:

- USB 2.0 high-speed (480 Mbps) to UART/MPSSE IC
- Single-chip USB-to-quad serial ports in various configurations
- Entire USB protocol handled on the chip without requiring USB-specific firmware programming
- USB 2.0 high-speed (480 Mbps) and full-speed (12 Mbps) compatibility
- Two multi-protocol synchronous serial engines (MPSSE) on channel A and channel B to simplify synchronous serial protocol (USB to JTAG, I2C, SPI, or bit-bang) design
- Fully assisted hardware handshaking and X-On/X-Off software handshaking
- +1.8 V (chip core) and +3.3 V I/O interfacing with +5 V tolerance

The following figure shows the FTDI interface of the SmartFusion2 Security Evaluation Board.

Figure 13 • **FTDI Interface**



For more information, see the Board Level Schematics document (provided separately).

4.10 I2C Port Header

The following table lists the two I2C ports routed to header H1.

Table 8 • **I2C Port Header**

Board Signal Name	SmartFusion2 Pin Name	Pin Number	Header H1
I2C0_SCL	MSIO61NB2/I2C_0_SCL/GPIO_31_B/USB_DATA1_C	G16	10, 14
I2C0_SDA	MSIO61PB2/I2C_0_SDA/GPIO_30_B/USB_DATA0_C	G17	11, 15
I2C1_SCL	MSIO11NB3/CCC_NE1_CLKI0/I2C_1_SCL/GPIO_1_A/USB_DATA4_A	R22	2, 6
I2C1_SDA	MSIO11PB3/CCC_NE0_CLKI0/I2C_1_SDA/GPIO_0_A/USB_DATA3_A	P22	3, 7

For more information, see the Board Level Schematics document (provided separately).

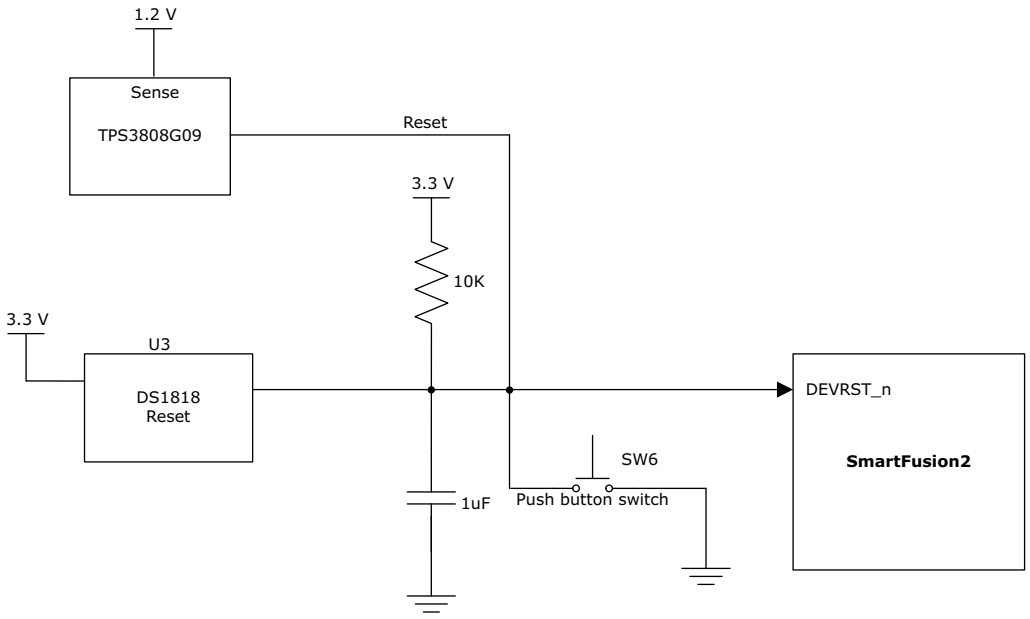
4.11 System Reset

DEVRST_N is an input-only reset pad that allows assertion of a full reset to the chip at any time. The DEVRST_N signal (active-low) is asserted in the following cases:

- When the **SW6** push-button switch is pressed
- When the 3.3 V or 1.2 V supplies fall below the threshold level

The following figure shows the system reset interface of the SmartFusion2 Security Evaluation Board.

Figure 14 • **System Reset Interface**



For more information, see the Board Level Schematics document (provided separately).

4.12 Clock Sources

This section provides information about the clock sources available in the SmartFusion2 Security Evaluation Kit.

4.12.1 50 MHz Oscillator

A 50 MHz clock oscillator with an accuracy of +/-50 ppm is available on the board. This clock oscillator is connected to the FPGA fabric to provide a system reference clock.

An on-chip SmartFusion2 PLL can be configured to generate a wide range of high-precision clock frequencies.

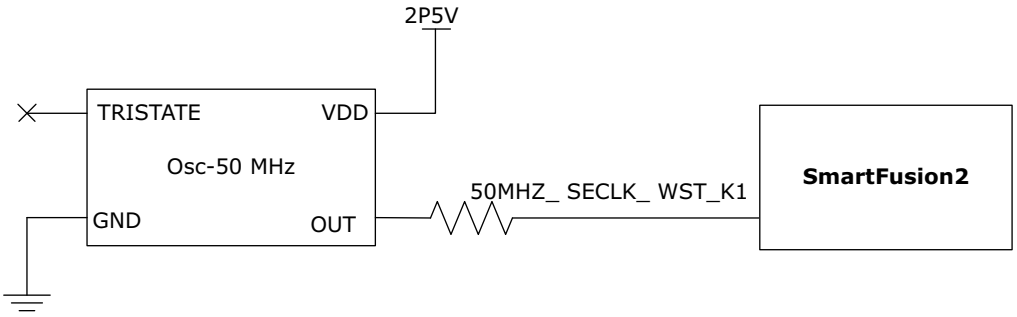
The following table provides package and pin details of the 50 MHz oscillator.

Table 9 • **50 MHz Clock**

SmartFusion2 Security Evaluation Kit Pin Name	SmartFusion2 Package Number	SmartFusion2 Device Pin Name
50MHZ_ SECLK_ WST_K1	K1	MSIOD178PB7/CCC_SW 0_CLKI0

The following figure shows the 50 MHz clock oscillator interface.

Figure 15 • **50 MHz Clock Oscillator Interface**



For more information, see the Board Level Schematics document (provided separately).

4.12.2 Other Clock Sources

The following additional clock sources are used in the SmartFusion2 Security Evaluation Kit:

- A 125 MHz clock oscillator for the SerDes0 interface. For more information, see SERDES0 Interface, page 12.
- 32.768 KHz crystal oscillators for the main and auxiliary oscillators of the SmartFusion2 device.

4.13 User Interface

The SmartFusion2 Security Evaluation Board UI has user LEDs as well as push-button switches.

4.13.1 User LEDs

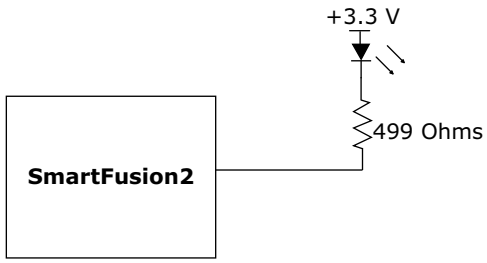
The board has eight active-low LEDs that are connected to the SmartFusion2 device. The following table lists the on-board user LEDs.

Table 10 • **LEDs**

SmartFusion2 Security Evaluation Board Pin	SmartFusion2 Package Pin Number	SmartFusion2 Device Pin Name
LED0 – Yellow	E1	MSIO143PB8
LED1 – Yellow	F4	MSIO145NB8
LED2 – Green	F3	MSIO145PB8
LED3 – Green	G7	MSIO146NB8
LED4 – Red	H7	MSIO146PB8
LED5 – Red	J6	MSIO148NB8
LED6 – Blue	H6	MSIO148PB8
LED7 – Blue	H5	MSIO150NB8

The following figure shows the LED interface of the SmartFusion2 Security Evaluation Board.

Figure 16 • **LED Interface**



For more information, see the Board Level Schematics document (provided separately).

4.13.2 Push-Button Switches

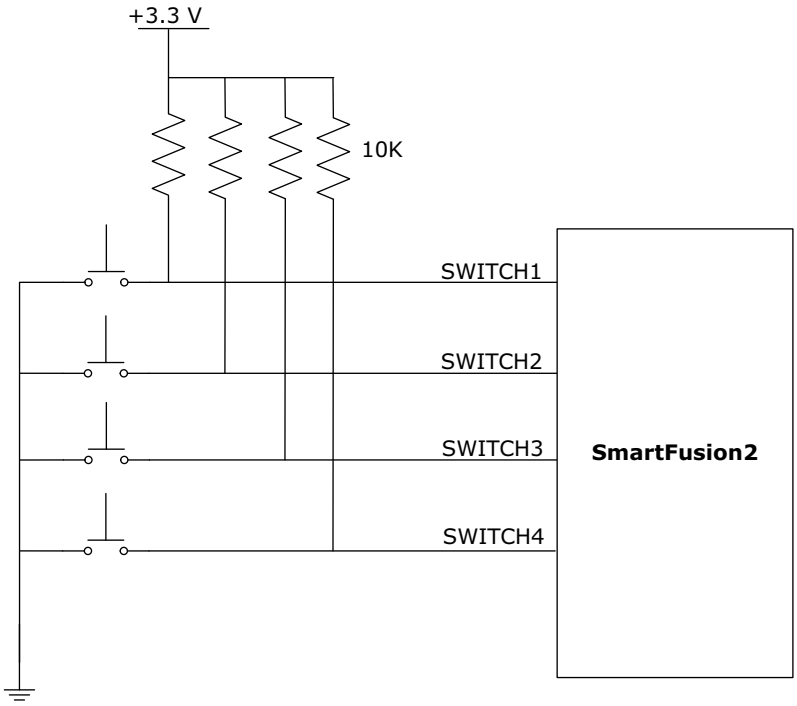
The SmartFusion2 Security Evaluation Kit comes with five push-button tactile switches that are connected to the SmartFusion2 device. The following table lists the on-board push-button switches.

Table 11 • **Push-Button Switches**

SmartFusion2 Security Evaluation Board Pin	SmartFusion2 Package Pin Number	SmartFusion2 Device Pin Name
SWITCH1	L20	MSIO17NB3/SPI_1_SS0/GPIO_13_A
SWITCH2	K16	MSIO23NB3/SPI_1_SS1/GPIO_14_A
SWITCH3	K18	MSIO24PB3/SPI_1_SS2/GPIO_15_A
SWITCH4	J18	MSIO24NB3/SPI_1_SS3/GPIO_16_A
SW6	R15	DEVRST_N

The following figure shows the switches interface of the SmartFusion2 Security Evaluation Board.

Figure 17 • **Switches Interface**



For more information, see the Board Level Schematics document (provided separately).

4.13.3 Slide Switches (DPDT)

The **SW7** slide switch powers the device ON or OFF from +12 V external DC jack.

4.13.4 DIP Switches (SPST)

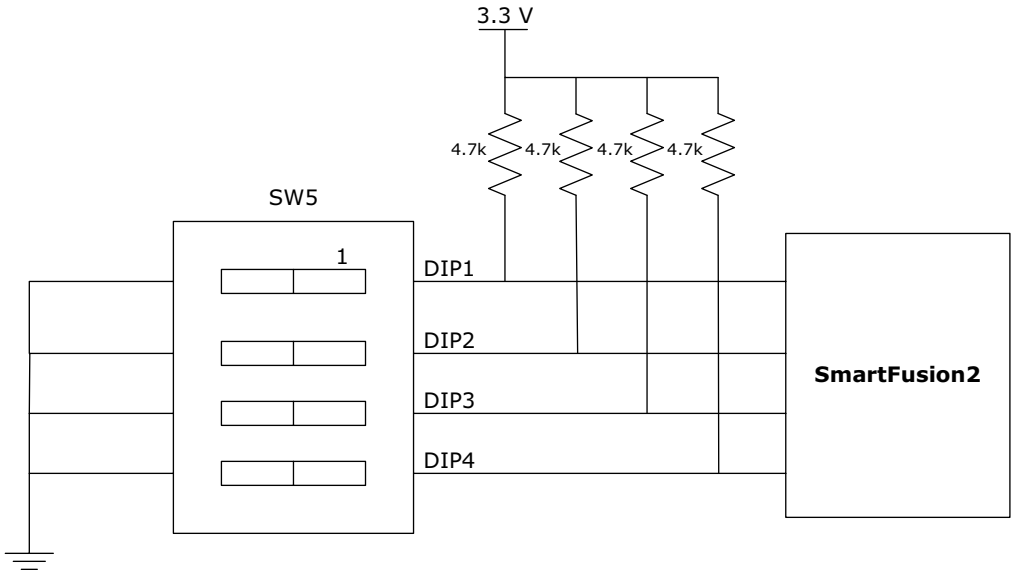
The **SW5** DIP switch has four connections to the SmartFusion2 device. The following table lists the on-board DIP switches.

Table 12 • **DIP Switches**

SmartFusion2 Security Evaluation Board Pin	SmartFusion2 Package Pin Number	SmartFusion2 Device Pin Name
DIP1	L19	MSIO18PB3/SPI_1_SS4/GPIO_17_A
DIP2	L18	MSIO18NB3/SPI_1_SS5/GPIO_18_A
DIP3	K21	MSIO19PB3/SPI_1_SS6/GPIO_23_A
DIP4	K20	MSIO19NB3/SPI_1_SS7/GPIO_24_A

The following figure shows the SPST interface of the SmartFusion2 Security Evaluation Board.

Figure 18 • **SPST Interface**



For more information, see the Board Level Schematics document (provided separately).

4.14 GPIO Header Pinout

Bank 4, bank 7, and bank 1 signals are routed to the GPIO header for user applications. The following table provides GPIO header pinout details.

Table 13 • **GPIO Header Pinout**

GPIO Header-J1	SmartFusion2 - U1		GPIO Header-J1	SmartFusion2 - U1	
Pin Number	**Package Number**	**Pin Name**	**Pin Number**	**Package Number**	**Pin Name**
1	AB15	MSIO213PB5/VCCC_SE1_CLKI	2		3P3V
3	AA15	MSIO213NB5	4		VSS
5		VSS	6	AA16	MSIO222PB5
7	AB18	MSIO230PB5	8	AA17	MSIO222NB5
9	AB19	MSIO230NB5	10		VSS
11		VSS	12	AB17	MSIO221PB5
13	Y18	MSIO228PB5	14	AA18	MSIO221NB5
15	Y19	MSIO228NB5	16		VSS
17		VSS	18	Y17	MSIO226PB5
19	W16	MSIO224PB5	20	W17	MSIO226NB5
21	V16	MSIO224NB5	22		VSS
23		VSS	24	U14	MSIO218PB5
25	C22	MSIO60PB2/MMUART_0_RXD/GPIO_28_B/USB_STP_C	26	U15	MSIO218NB5

Table 13 • **GPIO Header Pinout *(continued)***

GPIO Header-J1	SmartFusion2 - U1		GPIO Header-J1	SmartFusion2 - U1	
Pin Number	**Package Number**	**Pin Name**	**Pin Number**	**Package Number**	**Pin Name**
27	B22	MSIO60NB2/MMUART_0_CLK/GPIO_29_B/USB_NXT_C	28		VSS
29		VSS	30	V13	MSIO211PB5
31	Y15	MSIO216PB5	32	V14	MSIO211NB5
33	W15	MSIO216NB5	34		VSS
35		VSS	36	G5	MSIO98PB8
37	F5	MSIO132PB8	38	G6	MSIO131NB8
39	F6	MSIO132NB8	40		VSS
41		VSS	42	E4	MSIO138PB8
43	C4	MSIO127PB8	44	E5	MSIO138NB8
45	D5	MSIO127NB8	46		VSS
47		VSS	48	C3	MSIO129PB8
49	B2	MSIO136PB8	50	B3	MSIO129NB8
51	A2	MSIO136NB8	52		VSS
53		VSS	54	C1	MSIO140PB8
55	D1	MSIO142PB8	56	B1	MSIO140NB8
57	D2	MSIO142NB8	58		VSS
59		VSS	60	D3	MSIO134PB8
61		3P3V	62	D4	MSIO134NB8
63		3P3V	64		VSS

5 Pin List

The following table lists all the package pins in the SmartFusion2 M2S090TS-FGG484 device.

Table 14 • **M2S090TS-FGG484 Device Pin List**

Package Pin	Device Pin Name
A1	VSS
A2	MSIO136NB8
A3	DDRIO99NB1
A4	DDRIO99PB1
A5	DDRIO98NB1
A6	DDRIO92NB1/GB4/CCC_NW1_CLKI2
A7	DDRIO89PB1/MDDR_DQ_ECC1
A8	DDRIO89NB1/MDDR_DQ_ECC0
A9	DDRIO87NB1/MDDR_DQ1
A10	DDRIO84PB1/MDDR_DM_RDQS0
A11	DDRIO84NB1/MDDR_DQ4
A12	DDRIO81PB1/MDDR_DQ8
A13	DDRIO81NB1/MDDR_DQ9
A14	DDRIO77PB1/GB12/CCC_NE1_CLKI2/MDDR_DQ12
A15	DDRIO77NB1/MDDR_DQ13
A16	DDRIO72PB1/MDDR_CLK
A17	DDRIO72NB1/MDDR_CLK_N
A18	DDRIO71PB1/MDDR_BA0
A19	DDRIO71NB1/MDDR_BA1
A20	DDRIO67NB1/MDDR_ADDR6
A21	DDRIO64PB1/MDDR_ADDR10
A22	VSS
AA1	VSS
AA2	SERDES_0_TXD0_N
AA3	VSS
AA4	SERDES_0_TXD1_N
AA5	VSS
AA6	SERDES_0_TXD2_N
AA7	VSS
AA8	SERDES_0_TXD3_N
AA9	VSS
AA10	MSIO198PB5
AA11	MSIO203PB5
AA12	MSIO204PB5

Table 14 • **M2S090TS-FGG484 Device Pin List** ***(continued)***

AA13	MSIO209PB5/VCCC_SE0_CLKI
AA14	VSS
AA15	MSIO213NB5
AA16	MSIO222PB5
AA17	MSIO222NB5
AA18	MSIO221NB5
AA19	VDDI5
AA20	XTLOSC_AUX_EXTAL
AA21	XTLOSC_MAIN_EXTAL
AA22	JTAGSEL
AB1	VSS
AB2	SERDES_0_TXD0_P
AB3	VSS
AB4	SERDES_0_TXD1_P
AB5	VSS
AB6	SERDES_0_TXD2_P
AB7	VSS
AB8	SERDES_0_TXD3_P
AB9	VSS
AB10	MSIO198NB5
AB11	MSIO203NB5
AB12	VDDI5
AB13	MSIO208PB5/CCC_SW1_CLKI3
AB14	MSIO208NB5
AB15	MSIO213PB5/VCCC_SE1_CLKI
AB16	VSS
AB17	MSIO221PB5
AB18	MSIO230PB5
AB19	MSIO230NB5
AB20	XTLOSC_AUX_XTAL
AB21	XTLOSC_MAIN_XTAL
AB22	VSS
B1	MSIO140NB8
B2	MSIO136PB8
B3	MSIO129NB8
B4	VSS
B5	DDRIO98PB1
B6	DDRIO92PB1/GB0/CCC_NW0_CLKI3
B7	DDRIO91NB1/MDDR_DQS_ECC_N

Table 14 • **M2S090TS-FGG484 Device Pin List** ***(continued)***

B8	VDDI1
B9	DDRIO87PB1/MDDR_DQ0
B10	VSS
B11	DDRIO85PB1/MDDR_DQS0
B12	VDDI1
B13	DDRIO79PB1/GB8/CCC_NE0_CLKI3/MDDR_DQS1
B14	VSS
B15	DDRIO74PB1/MDDR_CKE
B16	VDDI1
B17	DDRIO70NB1/MDDR_ADDR0
B18	VSS
B19	DDRIO67PB1/MDDR_ADDR5
B20	VDDI1
B21	DDRIO64NB1/MDDR_ADDR11
B22	MSIO60NB2/MMUART_0_CLK/GPIO_29_B/USB_NXT_C
C1	MSIO140PB8
C2	VDDI8
C3	MSIO129PB8
C4	MSIO127PB8
C5	DDRIO97PB1
C6	VDDI1
C7	DDRIO91PB1/MDDR_DQS_ECC
C8	VSS
C9	DDRIO88NB1
C10	VDDI1
C11	DDRIO85NB1/MDDR_DQS0_N
C12	VSS
C13	DDRIO79NB1/MDDR_DQS1_N
C14	VDDI1
C15	DDRIO74NB1/MDDR_CS_N
C16	DDRIO70PB1/MDDR_BA2
C17	DDRIO68PB1/MDDR_ADDR3
C18	DDRIO68NB1/MDDR_ADDR4
C19	DDRIO66NB1/MDDR_ADDR7
C20	DDRIO66PB1/MDDR_ODT
C21	VSS
C22	MSIO60PB2/MMUART_0_RXD/GPIO_28_B/USB_STP_C
D1	MSIO142PB8
D2	MSIO142NB8

Table 14 • **M2S090TS-FGG484 Device Pin List** ***(continued)***

D3	MSIO134PB8
D4	MSIO134NB8
D5	MSIO127NB8
D6	DDRIO97NB1
D7	MDDR_IMP_CALIB
D8	DDRIO90NB1/MDDR_DM_RDQS_ECC
D9	DDRIO88PB1/CCC_NW1_CLKI3
D10	DDRIO83PB1/MDDR_DQ5
D11	DDRIO83NB1/MDDR_DQ6
D12	DDRIO80PB1/MDDR_DQ10/CCC_NE0_CLKI2
D13	DDRIO80NB1/MDDR_DQ11
D14	DDRIO76PB1/CCC_NE1_CLKI3/MDDR_DQ14
D15	VSS
D16	DDRIO69PB1/MDDR_ADDR1
D17	VDDI1
D18	DDRIO62PB1/MDDR_ADDR14
D19	VSS
D20	DDRIO63NB1/MDDR_ADDR13
D21[1]	MSI59NB2/MMUART_0_TXD/GPIO_27_B/USB_DIR_C
D22	FLASH_GOLDEN_N
E1	MSIO143PB8
E2	MSIO143NB8
E3	VSS
E4	MSIO138PB8
E5	MSIO138NB8
E6	VSS
E7	DDRIO93PB1/MDDR_TMATCH_ECC_OUT
E8	DDRIO90PB1/MDDR_TMATCH_ECC_IN
E9	VSS
E10	DDRIO86NB1/MDDR_DQ3
E11	VDDI1
E12	DDRIO82PB1/MDDR_DQ7
E13	DDRIO76NB1/MDDR_DQ15
E14	VSS
E15	DDRIO73PB1/MDDR_RESET_N
E16	DDRIO69NB1/MDDR_ADDR2
E17	DDRIO65PB1/MDDR_ADDR8
E18	DDRIO62NB1/MDDR_ADDR15
E19	DDRIO63PB1/MDDR_ADDR12

Table 14 • **M2S090TS-FGG484 Device Pin List *(continued)***

E20	VDDI2
E21	MSIO58NB2/MMUART_0_DCD/GPIO_22_B
E22	MSIO58PB2/MMUART_0_RI/GPIO_21_B
F1	VDDI8
F2	MSIO152NB8
F3	MSIO145PB8
F4	MSIO145NB8
F5	MSIO132PB8
F6	MSIO132NB8
F7	VDDI1
F8	DDRIO93NB1/CCC_NW0_CLKI2
F9	VDDI1
F10	DDRIO86PB1/MDDR_DQ2
F11	VSS
F12	DDRIO82NB1/MDDR_TMATCH_0_OUT
F13	VDDI1
F14	DDRIO75PB1/MDDR_RAS_N
F15	DDRIO73NB1/MDDR_CAS_N
F16	VSS
F17	DDRIO65NB1/MDDR_ADDR9
F18	MSIO57NB2/MMUART_0_DSR/GPIO_20_B
F19	MSIO57PB2/MMUART_0_CTS/GPIO_19_B/USB_DATA7_C
F20	MSIO56NB2/MMUART_0_DTR/GPIO_18_B/USB_DATA6_C
F21	MSIO56PB2/MMUART_0_RTS/GPIO_17_B/USB_DATA5_C
F22	VDDI2
G1	MSIO156NB8
G2	MSIO152PB8
G3	MSIO154NB8
G4	VDDI8
G5	MSIO131PB8
G6	MSIO131NB8
G7	MSIO146NB8
G8	CCC_NW1_PLL_VSSA
G9	CCC_NW1_PLL_VDDA
G10	VREF
G11	VREF
G12	DDRIO78PB1/MDDR_TMATCH_0_IN
G13	DDRIO78NB1/MDDR_DM_RDQS1
G14	DDRIO75NB1/MDDR_WE_N

Table 14 • M2S090TS-FGG484 Device Pin List *(continued)*

G15	VREF
G16	MSIO61NB2/I2C_0_SCL/GPIO_31_B/USB_DATA1_C
G17	MSIO61PB2/I2C_0_SDA/GPIO_30_B/USB_DATA0_C
G18	MSIO55NB2/MMUART_1_RXD/GPIO_26_B/USB_DATA3_C
G19	MSIO55PB2/GB14/VCCC_SE1_CLKI/MMUART_1_CLK/GPIO_25_B/USB_DATA4_C
G20	VSS
G21	MSIO53NB2/MMUART_1_DCD/GPIO_16_B
G22	MSIO53PB2/CCC_NE1_CLKI1/MMUART_1_RI/GPIO_15_B
H1	MSIO156PB8/GB6/CCC_NW1_CLKI1
H2	VSS
H3	MSIO154PB8
H4	MSIO150PB8
H5	MSIO150NB8
H6	MSIO148PB8
H7	MSIO146PB8
H8	CCC_NW0_PLL_VDDA
H9	VSS
H10	VDD
H11	VSS
H12	VDDI1
H13	VSS
H14	VDDI1
H15	CCC_NE0_PLL_VDDA
H16	MSS_MDDR_PLL_VDDA
H17	MSS_MDDR_PLL_VSSA
H18	VDDI2
H19	MSIO54NB2/MMUART_1_TXD/GPIO_24_B/USB_DATA2_C
H20	MSIO54PB2/GB10/VCCC_SE0_CLKI/USB_XCLK_C
H21	MSIO51NB2/MMUART_1_DTR/GPIO_12_B
H22	MSIO51PB2/MMUART_1_RTS/GPIO_11_B
J1	MSIO158PB8/CCC_NW1_CLKI0
J2	MSIO158NB8
J3	MSIO157PB8/GB2/CCC_NW0_CLKI1
J4	MSIO157NB8
J5	VSS
J6	MSIO148NB8
J7	VDDI8
J8	CCC_NW0_PLL_VSSA
J9	VDD

Table 14 • **M2S090TS-FGG484 Device Pin List** ***(continued)***

J10	VSS
J11	VDD
J12	VSS
J13	VDD
J14	VSS
J15	CCC_NE0_PLL_VSSA
J16	CCC_NE1_PLL_VSSA
J17	CCC_NE1_PLL_VDDA
J18	MSIO24NB3/SPI_1_SS3/GPIO_16_A
J19	MSIO52NB2/MMUART_1_DSR/GPIO_14_B
J20	MSIO52PB2/CCC_NE0_CLKI1/MMUART_1_CTS/GPIO_13_B
J21	VDDI2
J22	MSIO20NB3/GB13/VCCC_SE1_CLKI/GPIO_26_A
K1	MSIOD178PB7/CCC_SW0_CLKI0
K2	MSIOD178NB7
K3	VDDI7
K4	MSIOD175PB7/GB5/CCC_SW1_CLKI1
K5	MSIOD175NB7
K6	MSIO159PB8/CCC_NW0_CLKI0
K7	MSIO159NB8
K8	MSIOD176PB7/GB1/CCC_SW0_CLKI1
K9	VSS
K10	VDD
K11	VSS
K12	VDD
K13	VSS
K14	VDD
K15	MSIO22NB3/SPI_0_SS2/GPIO_9_A/USB_DATA6_A
K16	MSIO23NB3/SPI_1_SS1/GPIO_14_A
K17	MSIO23PB3/SPI_0_SS3/GPIO_10_A/USB_DATA7_A
K18	MSIO24PB3/SPI_1_SS2/GPIO_15_A
K19	VSS
K20	MSIO19NB3/SPI_1_SS7/GPIO_24_A
K21	MSIO19PB3/SPI_1_SS6/GPIO_23_A
K22	MSIO20PB3/GB9/VCCC_SE0_CLKI/GPIO_25_A
L1	VSS
L2	MSIOD179PB7
L3	MSIOD179NB7
L4	MSIOD180PB7

Table 14 • **M2S090TS-FGG484 Device Pin List** ***(continued)***

L5	MSIOD180NB7
L6	VDDI7
L7	MSIOD177NB7
L8	MSIOD176NB7
L9	VDD
L10	VSS
L11	VDD
L12	VSS
L13	VDD
L14	VSS
L15	VPP
L16	MSIO22PB3/SPI_0_SS1/GPIO_8_A/USB_DATA5_A
L17	VDDI3
L18	MSIO18NB3/SPI_1_SS5/GPIO_18_A
L19	MSIO18PB3/SPI_1_SS4/GPIO_17_A
L20	MSIO17NB3/SPI_1_SS0/GPIO_13_A
L21	MSIO17PB3/SPI_1_SDO/GPIO_12_A
L22	VSS
M1	MSIOD185NB7
M2	MSIOD183NB7
M3	MSIOD183PB7
M4	VSS
M5	MSIOD181PB7
M6	MSIOD181NB7
M7	MSIOD177PB7/CCC_SW1_CLKI0
M8	MSIOD188NB7
M9	VSS
M10	VDD
M11	VSS
M12	VDD
M13	VSS
M14	VDD
M15	VPPNVM
M16	MSIO14PB3/SPI_0_SS4/GPIO_19_A
M17	MSIO14NB3/SPI_0_SS5/GPIO_20_A
M18	MSIO15PB3/SPI_0_SS6/GPIO_21_A
M19	MSIO15NB3/SPI_0_SS7/GPIO_22_A
M20	VDDI3
M21	MSIO16PB3/SPI_1_CLK

Table 14 • **M2S090TS-FGG484 Device Pin List** ***(continued)***

M22	MSIO16NB3/SPI_1_SDI/GPIO_11_A
N1	MSIOD185PB7
N2	VDDI7
N3	MSIOD184PB7
N4	MSIOD184NB7
N5	MSIOD182PB7
N6	MSIOD182NB7
N7	VSS
N8	MSIOD188PB7
N9	VDD
N10	VSS
N11	VDD
N12	VSS
N13	VDD
N14	VSS
N15	VSSNVM
N16	MSIO8PB3/CAN_RX/GPIO_3_A/USB_DATA1_A
N17	MSIO8NB3/CAN_TX_EN_N/GPIO_4_A/USB_DATA2_A
N18	VSS
N19	MSIO12PB3/SPI_0_CLK/USB_XCLK_A
N20	MSIO12NB3/SPI_0_SDI/GPIO_5_A/USB_DIR_A
N21	MSIO13PB3/SPI_0_SDO/GPIO_6_A/USB_STP_A
N22	MSIO13NB3/SPI_0_SS0/GPIO_7_A/USB_NXT_A
P1	MSIOD187PB7
P2	MSIOD187NB7
P3	MSIOD186NB7
P4	MSIOD186PB7
P5	VDDI7
P6	MSIOD189PB7
P7	MSIOD189NB7
P8	SERDES_0_VDD
P9	VSS
P10	VDD
P11	VSS
P12	VDD
P13	VSS
P14	VDD
P15	VPP
P16	MSIO7NB3/CAN_TX/GPIO_2_A/USB_DATA0_A

Table 14 • **M2S090TS-FGG484 Device Pin List** ***(continued)***

P17	MSIO6PB3/USB_DATA6_B
P18	MSIO6NB3
P19	SC_SPI_SDO
P20	SC_SPI_SS
P21	VSS
P22	MSIO11PB3/CCC_NE0_CLKI0/I2C_1_SDA/GPIO_0_A/USB_DATA3_A
R1	MSIOD190NB7
R2	MSIOD190PB7
R3	MSIOD191PB7
R4	MSIOD191NB7
R5	VSS
R6	CCC_SW0_PLL_VSSA
R7	CCC_SW1_PLL_VDDA
R8	SERDES_0_L01_VDDAIO
R9	VSS
R10	VSS
R11	VDD
R12	VSS
R13	VDD
R14	VSS
R15	DEVRST_N
R16	MSIO7PB3
R17	MSIO1PB3/USB_XCLK_B
R18	MSIO1NB3/USB_DIR_B
R19	VDDI3
R20	SC_SPI_CLK
R21	SC_SPI_SDI
R22	MSIO11NB3/CCC_NE1_CLKI0/I2C_1_SCL/GPIO_1_A/USB_DATA4_A
T1	MSIOD193NB6/SERDES_0_REFCLK0_N
T2	VSS
T3	MSIOD192NB7
T4	MSIOD192PB7
T5	CCC_SW0_PLL_VDDA
T6	SERDES_0_PLL_VSSA
T7	CCC_SW1_PLL_VSSA
T8	SERDES_0_PLL_VDDA
T9	SERDES_0_VDD
T10	SERDES_0_L23_VDDAIO

Table 14 • **M2S090TS-FGG484 Device Pin List** ***(continued)***

T11	NC
T12	NC
T13	MSIO210NB5
T14	VDDI5
T15	VSS
T16	MSIO232NB5
T17	VSS
T18	MSIO2PB3/USB_STP_B
T19	MSIO2NB3/USB_NXT_B
T20	MSIO5PB3/USB_DATA4_B
T21	MSIO5NB3/USB_DATA5_B
T22	VDDI3
U1	MSIOD193PB6/SERDES_0_REFCLK0_P
U2	VDDI6
U3	MSIOD194PB6/SERDES_0_REFCLK1_P
U4	MSIOD194NB6/SERDES_0_REFCLK1_N
U5	SERDES_0_L01_REXT
U6	SERDES_0_L01_REFRET
U7	SERDES_0_L01_VDDAPLL
U8	SERDES_0_L23_VDDAPLL
U9	VPP
U10	MSIO199PB5
U11	MSIO199NB5
U12	VSS
U13	MSIO210PB5/GB11/VCCC_SE0_CLKI
U14	MSIO218PB5
U15	MSIO218NB5
U16	MSIO232PB5
U17	MSIO234NB5
U18	MSIO238NB5
U19	MSIO0PB3
U20	VSS
U21	MSIO4NB3/USB_DATA3_B
U22	MSIO4PB3/USB_DATA2_B
V1	VSS
V2	VSS
V3	VSS
V4	VSS
V5	VSS

Table 14 • **M2S090TS-FGG484 Device Pin List** ***(continued)***

V6	VSS
V7	VSS
V8	SERDES_0_L23_REXT
V9	SERDES_0_L23_REFRET
V10	VDDI5
V11	MSIO201PB5/GB3/CCC_SW0_CLKI3
V12	MSIO206NB5
V13	MSIO211PB5
V14	MSIO211NB5
V15	VSS
V16	MSIO224NB5
V17	MSIO234PB5
V18	MSIO238PB5
V19	MSIO0NB3/USB_DATA7_B
V20	JTAG_TMS/M3_TMS/M3_SWDIO
V21	MSIO3NB3/USB_DATA1_B
V22	MSIO3PB3/USB_DATA0_B
W1	SERDES_0_RXD0_P
W2	VSS
W3	SERDES_0_RXD1_P
W4	VSS
W5	SERDES_0_RXD2_P
W6	VSS
W7	SERDES_0_RXD3_P
W8	VSS
W9	MSIO196PB5
W10	MSIO197PB5/PROBE_A
W11	MSIO201NB5/GB7/CCC_SW1_CLKI2
W12	MSIO206PB5
W13	VDDI5
W14	MSIO212NB5
W15	MSIO216NB5
W16	MSIO224PB5
W17	MSIO226NB5
W18	VSS
W19	MSIO236NB5
W20	JTAG_TCK/M3_TCK
W21	VDDI4
W22	JTAG_TDI/M3_TDI

Table 14 • **M2S090TS-FGG484 Device Pin List *(continued)***

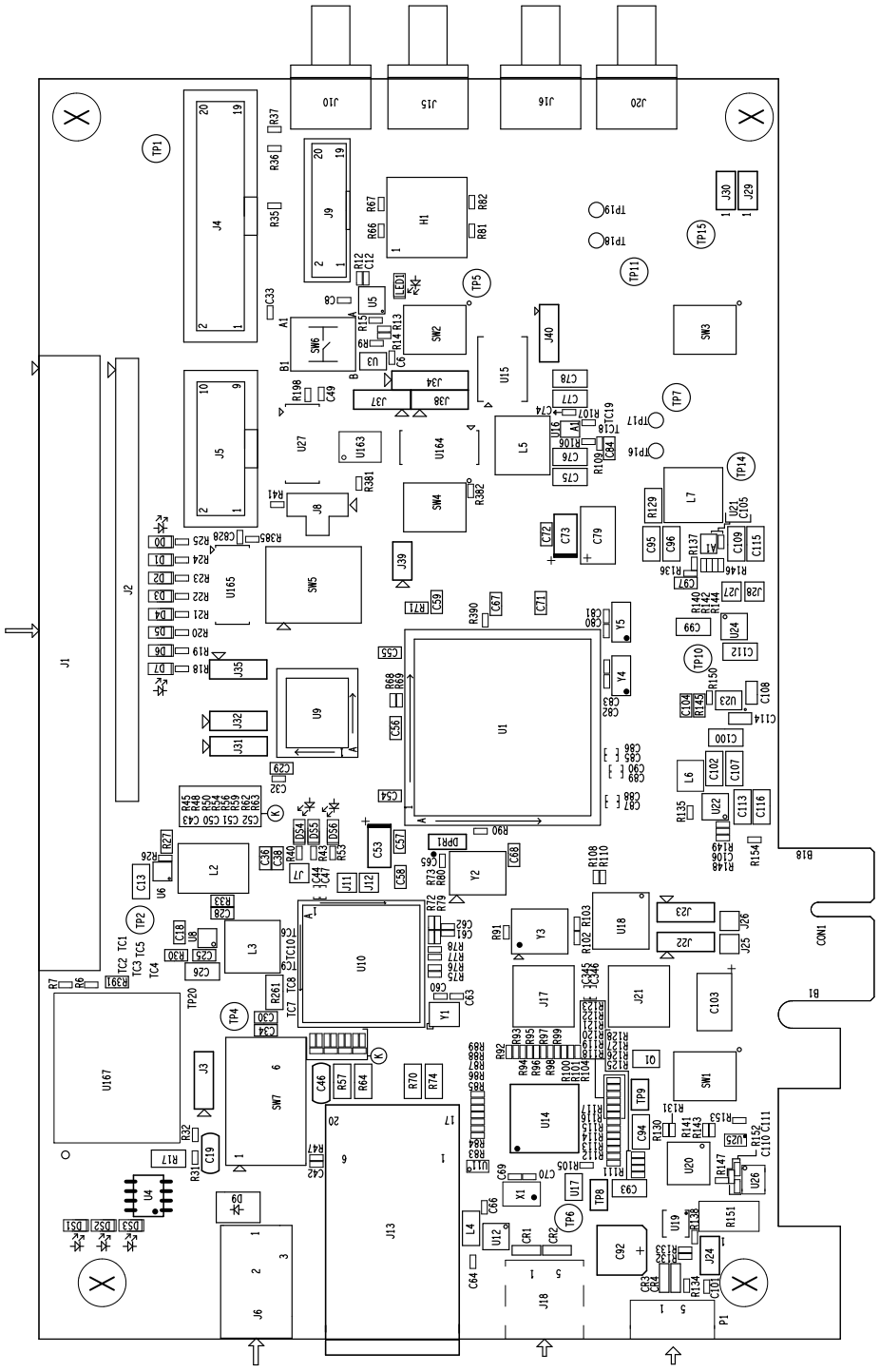
Y1	SERDES_0_RXD0_N
Y2	VSS
Y3	SERDES_0_RXD1_N
Y4	VSS
Y5	SERDES_0_RXD2_N
Y6	VSS
Y7	SERDES_0_RXD3_N
Y8	VSS
Y9	MSIO196NB5/CCC_SW0_CLKI2
Y10	MSIO197NB5/PROBE_B
Y11	VSS
Y12	MSIO204NB5
Y13	MSIO209NB5
Y14	MSIO212PB5/GB15/VCCC_SE1_CLKI
Y15	MSIO216PB5
Y16	VDDI5
Y17	MSIO226PB5
Y18	MSIO228PB5
Y19	MSIO228NB5
Y20	MSIO236PB5
Y21	JTAG_TDO/M3_TDO/M3_SWO
Y22	JTAG_TRSTB/M3_TRSTB

1. This is an input-only pin and cannot be used as a fabric output.

6 Board Components Placement

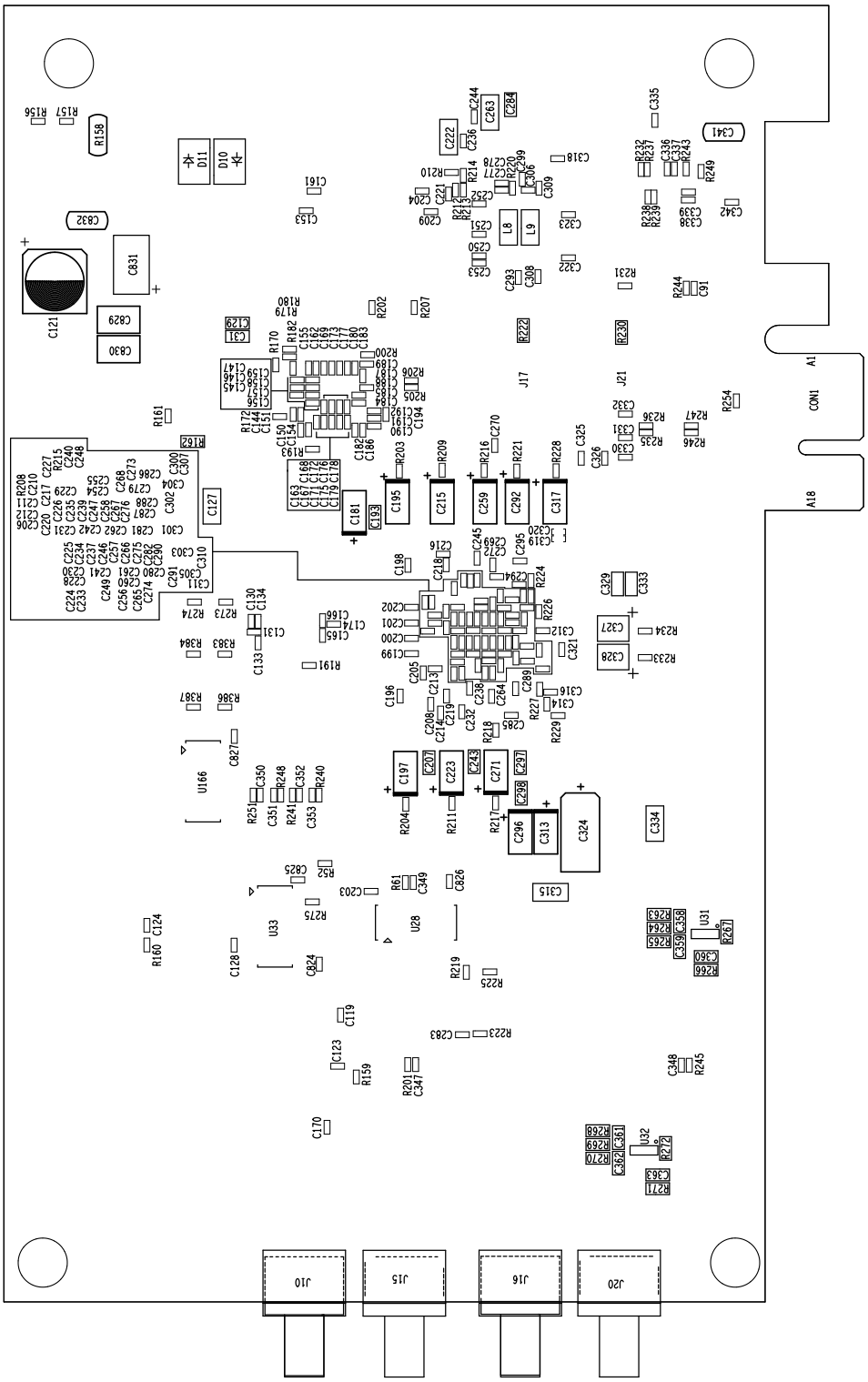
The following figure shows the placement of various components on the SmartFusion2 Security Evaluation Kit silkscreen.

Figure 19 • **Silkscreen Top View**



The following figure shows the bottom view of the SmartFusion2 Security Evaluation Kit silkscreen.

Figure 20 • **Silkscreen Bottom View**



7 Demo Design

The SmartFusion2 M2S090TS-EVAL-KIT comes with a preloaded PCIe control plane design to demonstrate the PCIe interface of the SmartFusion2 device. The following table lists the requirements for running the PCIe demo design.

Table 15 • **PCIe Demo Design Requirements**

Design Requirements	Version
Host PC or laptop with a PCIe 2.0 Gen 1- or Gen 2-compliant slot	64-bit Windows 7 OS or 64-bit Red Hat Linux OS (kernel version 2.6.18-308)
Express card slot and PCIe card adapter for laptop only (not provided with the kit contents)	–
PCIe edge card ribbon cable (not included in the kit)	–
Host PC drivers (provided with the design files)	–
GUI executable (provided with the design files)	–

The design files for this demo can be downloaded from the Microsemi website: *http://soc.microsemi.com/download/rsc/?f=sf2_pcie_control_plane_demo_advanced_and_evaluation_kit_liberov11p4_dg_df*

For information about how to run the demo design, see Appendix: Running the PCIe Demo Design on Windows, page 57.

8 Manufacturing Test

The M2S090TS-EVAL-KIT contains a manufacturing test program that can be run to verify the functionality of the board. The test program contains a list of options that can be run as diagnostics. After the HyperTerminal is set up and the board is powered up, various tests that can be performed on the board are displayed (see Figure 31, page 49). One or more tests can then be selected from the list of available tests.

Before testing the SmartFusion2 Security Evaluation Board:

- Download the `M2S090_EVAL_KIT_MTD_SP1.prjx` file from *http://soc.microsemi.com/download/rsc/?f=M2S090TS_EVAL_KIT_DF*.
- Download and install the FTD drivers from *http://www.ftdichip.com/Drivers/D2XX.htm*.

8.1 Programming M2S090TS-EVAL-KIT

This section provides information about programming the M2S090TS-EVAL-KIT for the manufacturing test.

8.1.1 Installing Libero v11.5 or Later

Before starting the manufacturing test, make sure the Libero SoC software (v11.5 or later) and other required tools are installed (see Software Settings, page 6). After Libero v11.5 or later is installed, connect J18 to the host PC using a mini USB to Type A USB cable.

8.1.2 Validating Power Supply

To test and validate the power supply to the board:

1. Connect the following jumpers on the SmartFusion2 Security Evaluation Board:
   - Short the **J3** jumper to position 1-2
   - Short the **J8** jumper to position 1-2
   - Short the **J22** and J23 jumpers to position 1-2
   - Short the **H1** jumper to position 6-10
   - Short the **H1** jumper to position 7-11
   - Short the **J24** jumper to position 1-2
   - Short the **J31** jumper to position 1-2
   - Short the **J35** jumper to position 2-3

Note: Before making the jumper connections, switch OFF the **SW7** power supply switch.

2. Connect the 12 V/5 A power supply brick to the J6 jumper.
3. Switch ON the power supply switch, **SW7**.
   When the board is successfully set up, the DS1, DS2, and DS3 LEDs start glowing.

8.1.3 Programming the FPGA Using Embedded FlashPro5

The M2S090TS-EVAL-KIT has an embedded FlashPro5 programmer; therefore, an external programmer is not required to program the SmartFusion2 device. The device can be programmed using the embedded FlashPro5, provided the FlashPro software is installed on the host PC.

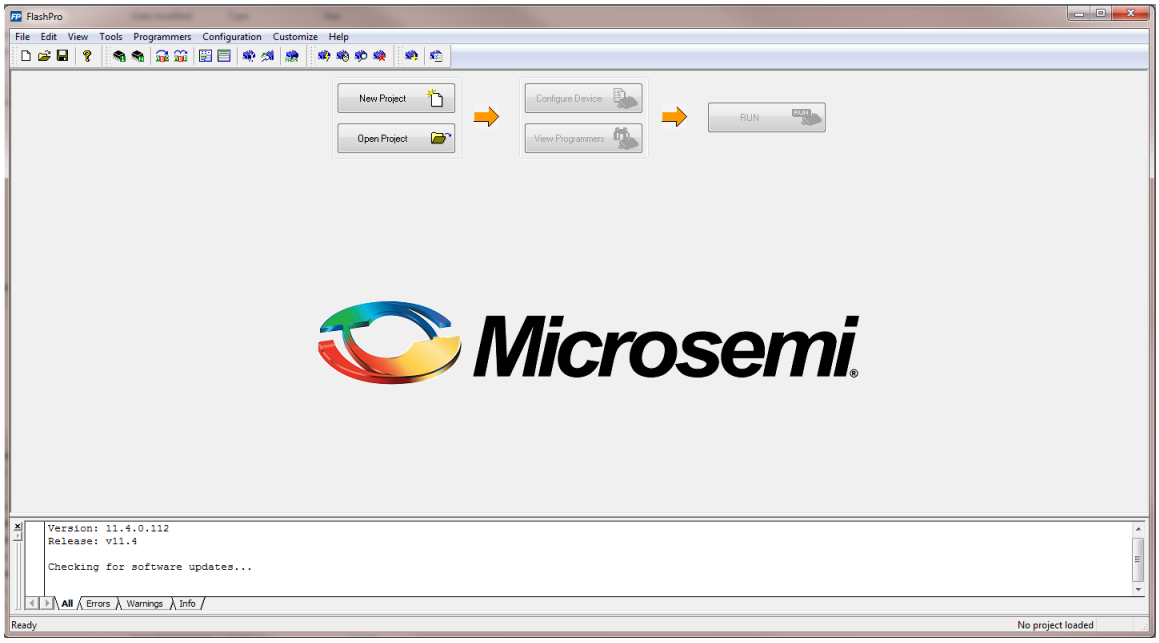
Note: The board can also be programmed using FlashPro4. To program the board using FlashPro4, connect the FlashPro4 header to the **J5** jumper, and change the position of the **J35** jumper to pin 1-2.

To program the device using the embedded FlashPro5:

1. Connect one end of a mini USB to Type A USB cable to the **J18** jumper and the other end to the USB port of the host PC.

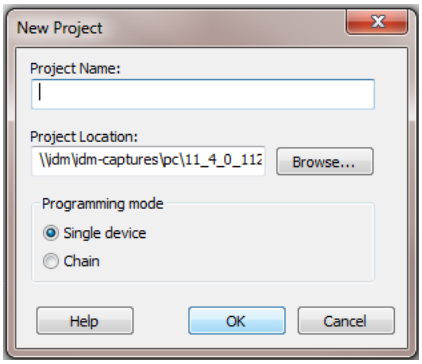
2. Launch the FlashPro software.

Figure 21 • **FlashPro Window**



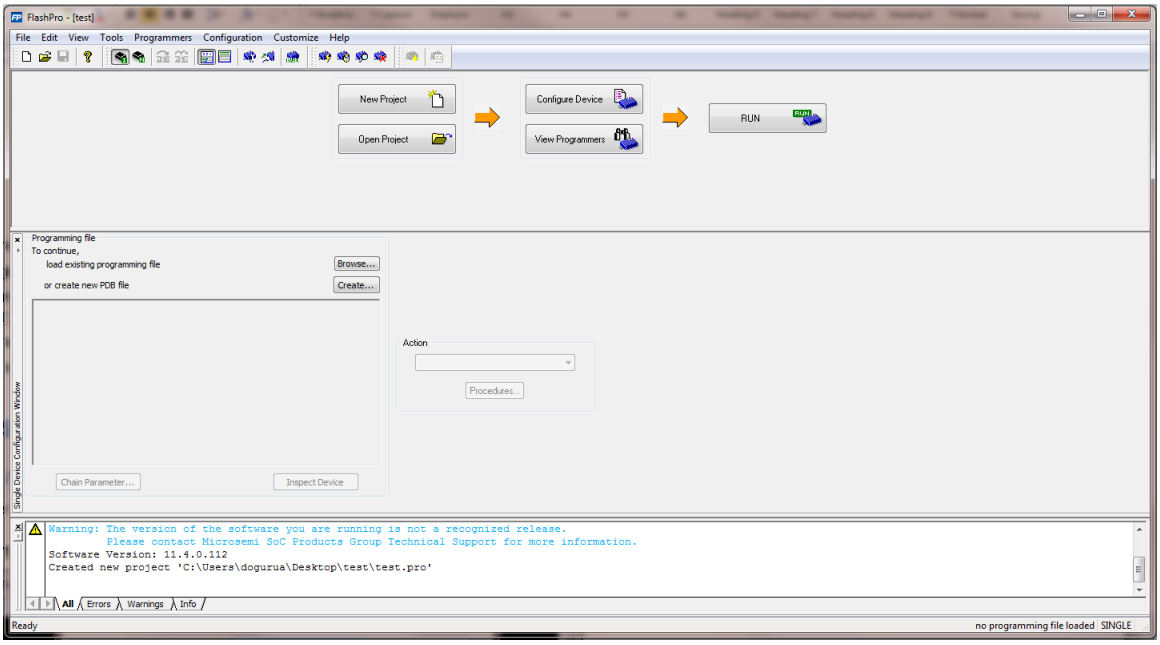
3. Click **New Project** to create a new project.
4. In the **New Project** window, do the following, and click **OK**:
   - Enter a project name.
   - Select **Single device** as the programming mode.

Figure 22 • **New Project Window**



5. Click **Configure Device**.

Figure 23 • **Configuring the Device**



6. Click **Browse**, and select the `SEC_KIT_MTD_top.stp` file from the **Load Programming File** window.
7. Click **Program** to program the device.
   When the device is programmed successfully, a **Run Program PASSED** status is displayed.

8.2 Running the Manufacturing Test

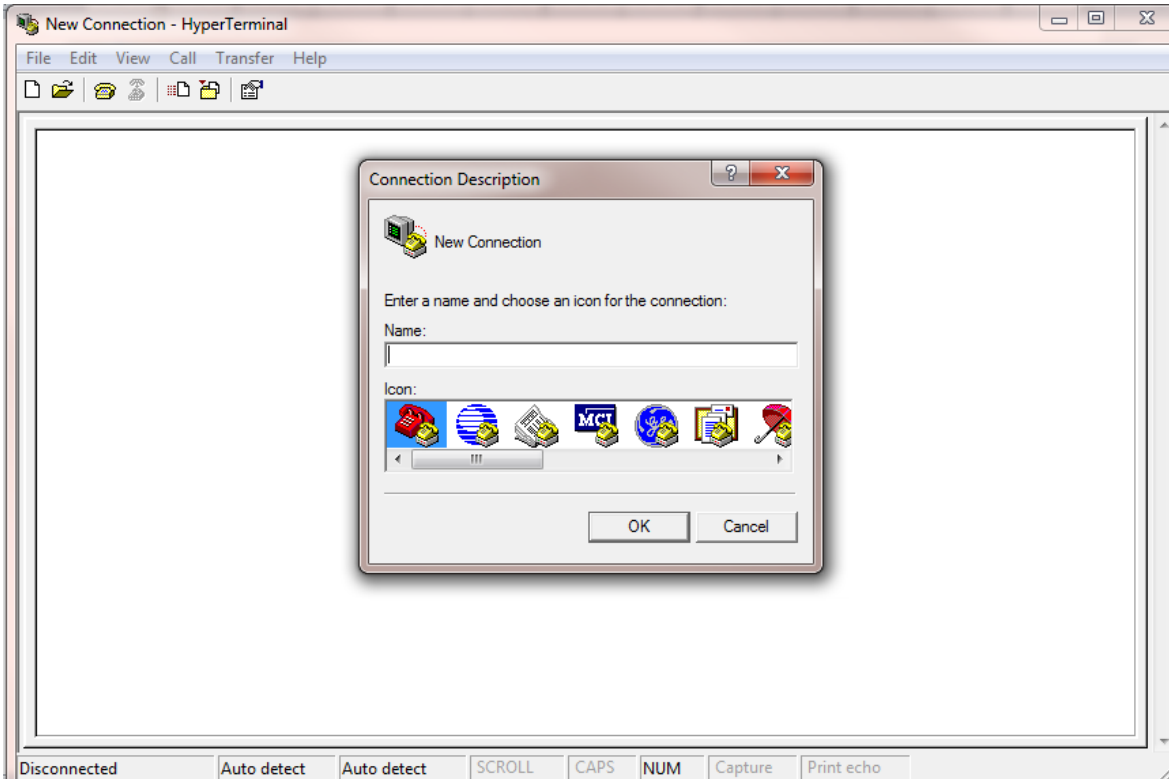
This section describes how to run the manufacturing test for the SmartFusion2 Security Evaluation Board.

8.2.1 Setting Up HyperTerminal

To set HyperTerminal up for the manufacturing test:

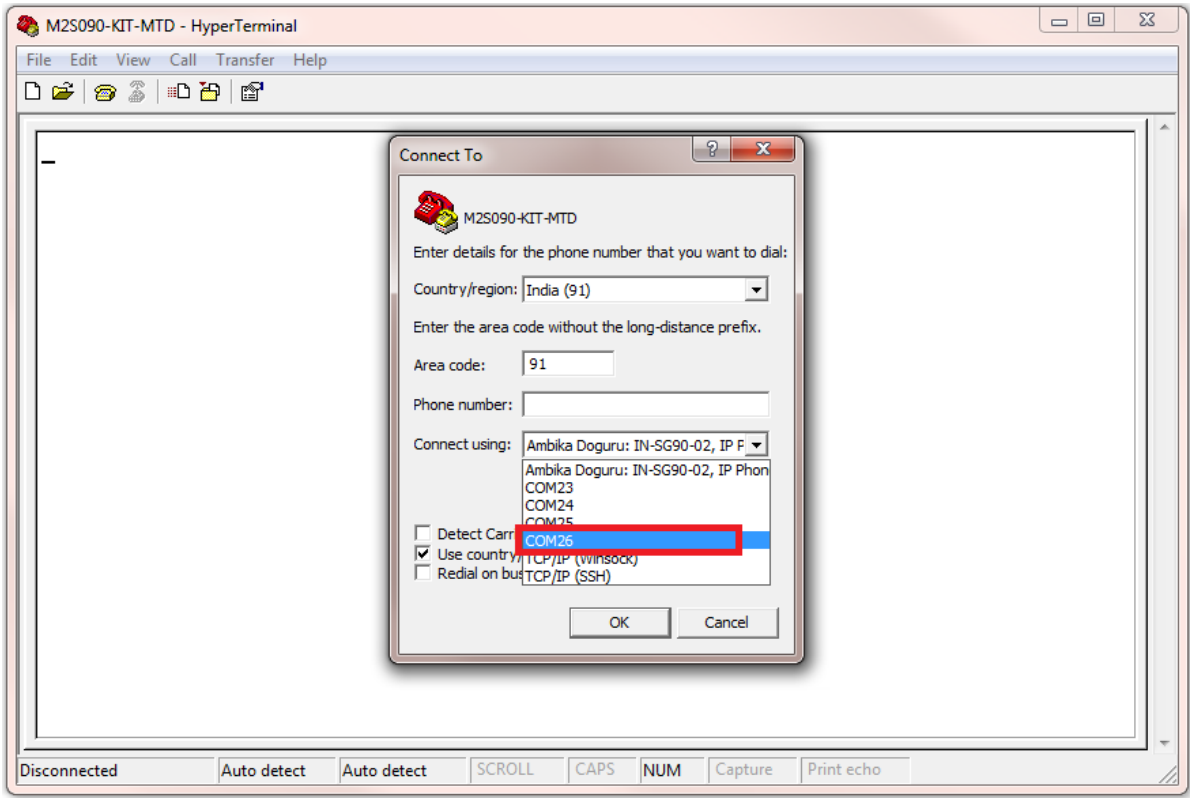
1. Connect **J18** to the host PC using a mini USB to Type A USB cable.
2. Launch **HyperTerminal** from the Start menu.

Figure 24 • **Connection Description Window**



3. Enter **M2S090-KIT-MTD** as the connection name, and click **OK**.
   The **Connect To** dialog-box appears, as shown in the following figure.

Figure 25 • **Connect To Window**



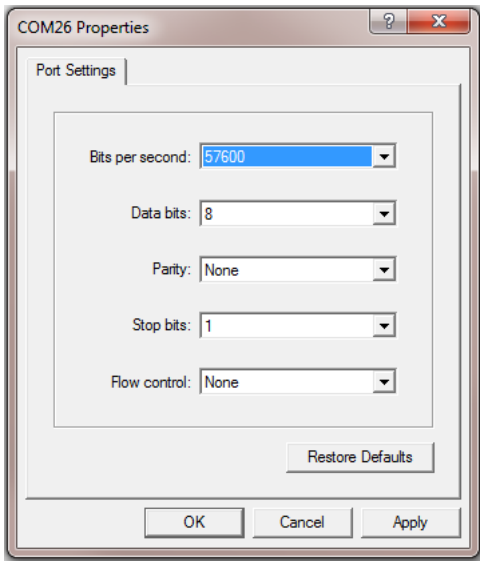
4. Select the highest value COM port from the **Connect using** drop-down list, and click **OK**.

Note: When using a USB cable for HyperTerminal communication, four COM ports are available in the drop-down list.

5. When only one COM port appears, select the COM port to establish connection with the host PC.

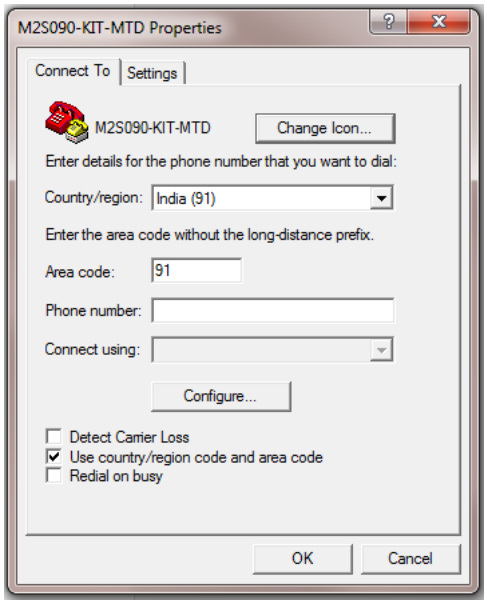
6. In the **Port Settings** window, select the following settings:
   - Bits per second: 57600
   - Data bits: 8
   - Parity: None
   - Stop bits: 1
   - Flow control: None

Figure 26 • **Port Settings Window**



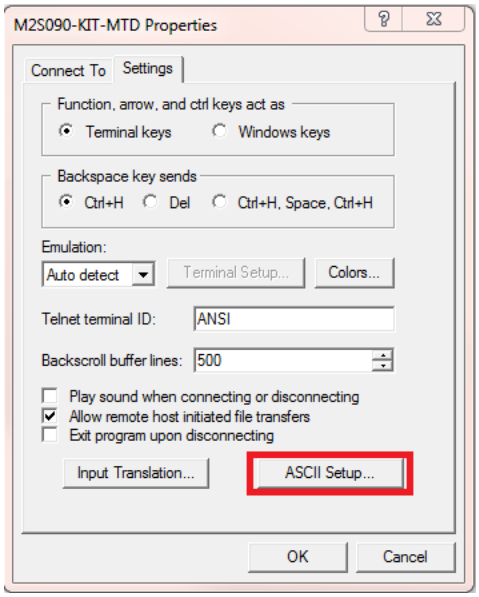
7. Click **Apply**, then click **OK**.
8. Select **Properties** from the **File** menu in the HyperTerminal window.
   The **M2S090-KIT-MTD Properties** window appears, as shown in the following figure.

Figure 27 • **M2S090-KIT-MTD Properties Window**



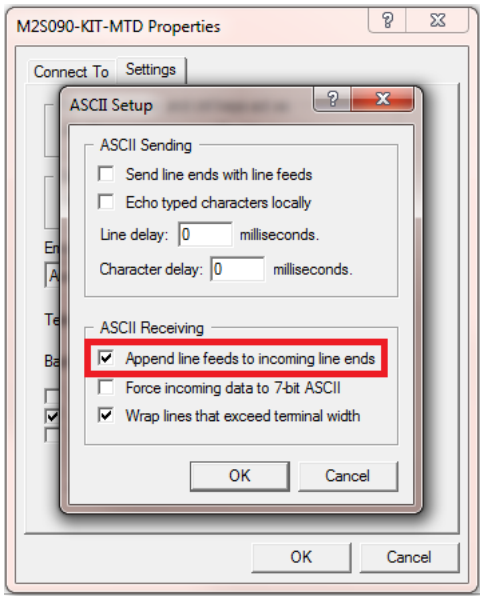
9. Select the **Settings** tab.

Figure 28 • **Settings Tab**



10. Keep the default settings, and click **ASCII Setup**.
    The **ASCII Setup** dialog-box appears, as shown in the following figure.

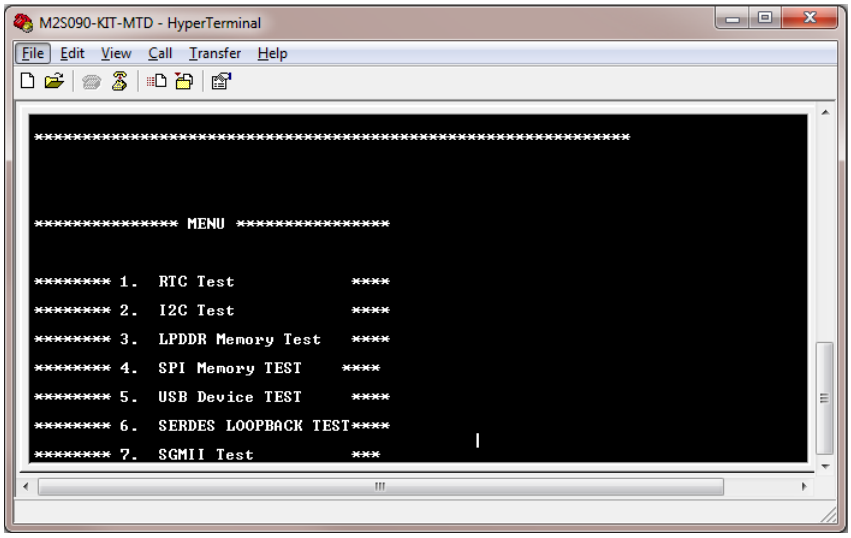
Figure 29 • **ASCII Setup Window**



11. Select the **Append line feeds to incoming line ends** check box, and click **OK**.
12. Click **OK** to save the properties, and close the **M2S090-KIT-MTD Properties** window.

13. Press the **SW6** switch to restart the board with the selected settings. The **HyperTerminal** window appears, as shown in the following figure.

Figure 30 • **HyperTerminal Window**



8.2.2 Setting Up Jumpers

The following table specifies the jumper settings required to perform various tests on the SmartFusion2 Security Evaluation Board.

Table 16 • **Jumper Settings for Manufacturing Test**

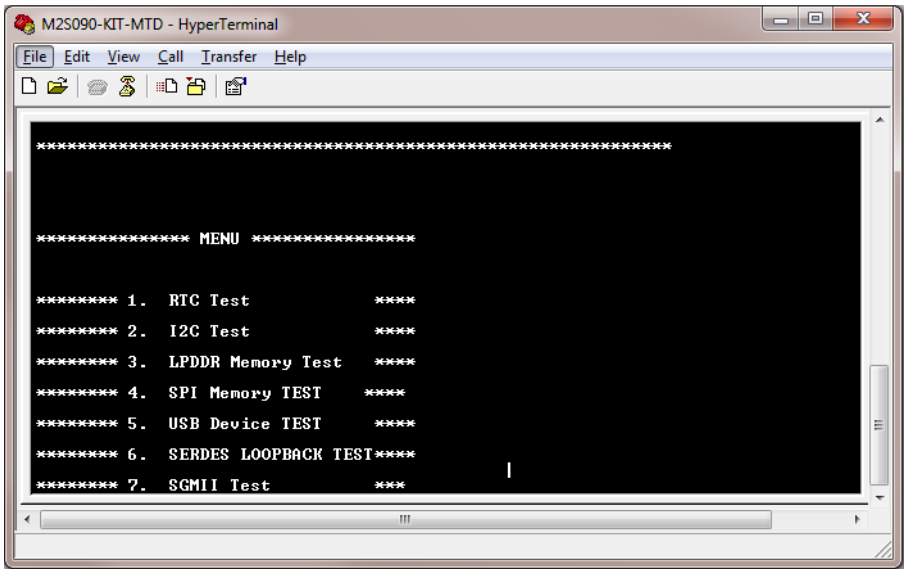
Test	Jumper Settings
HyperTerminal communication test	Connect J18 to the host PC using a mini USB to Type A USB cable).
RTC test	–
I2C test	Short H1 pins 6–10 and 7–11.
LDDR3 memory test	–
SPI memory test	–
USB device test	Connect Micro B to P1, and connect other end of the cable to the host PC (type A).
SerDes loopback test	Connect J20 to J15, and J16 to J10 using an SMA-to-SMA cable.
	Loopback cable (5 Gbps data rate).
SGMII test	Connect an Ethernet cable to J13, and connect the other end of the cable to the 1 Gbps Ethernet switch or network.

8.2.3 Running the Test

After the device is programmed and the jumper settings are applied, follow these steps to run the manufacturing test:

1. Press the **SW6** reset switch on the M2S090TS-EVAL-KIT to reset the board and begin the tests. When the setup is completed, all tests are listed in the **HyperTerminal** window, as shown in the following figure.

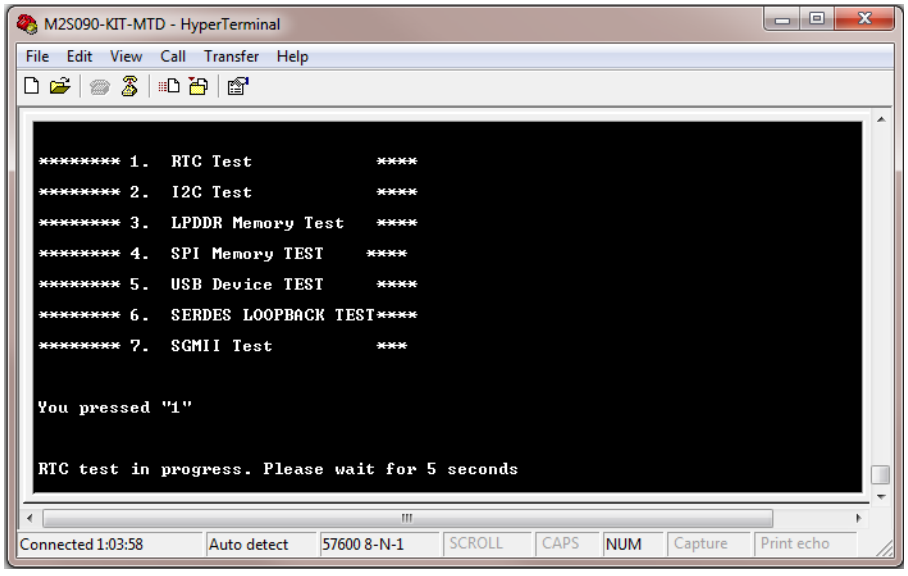
Figure 31 • **Test Menu**



If the list of tests does not appear, press the **SW6** reset switch again. If the list still does not appear, then check all the jumpers, and the HyperTerminal settings.

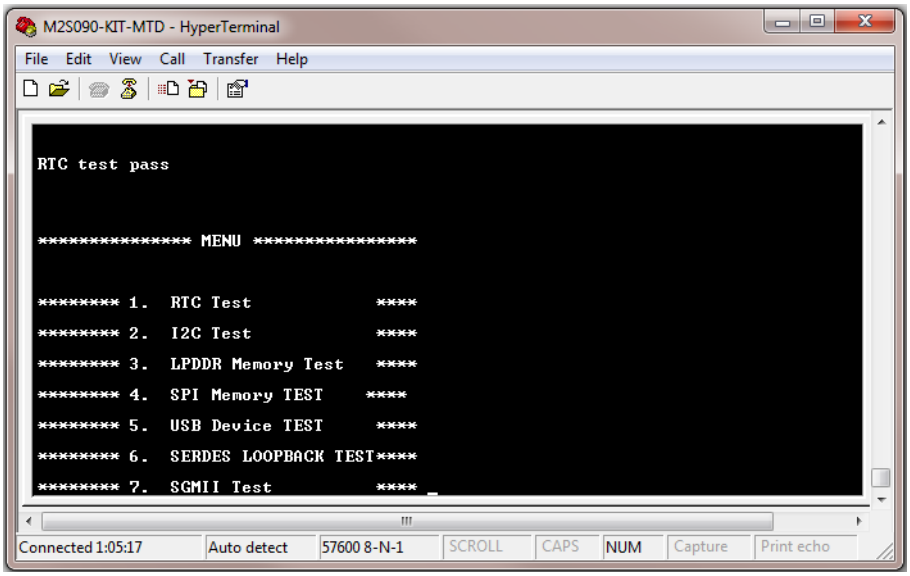
2. Press **1** to run the RTC test. Wait for five seconds for the test to be run.
The following message appears.

Figure 32 • **Running RTC Test**



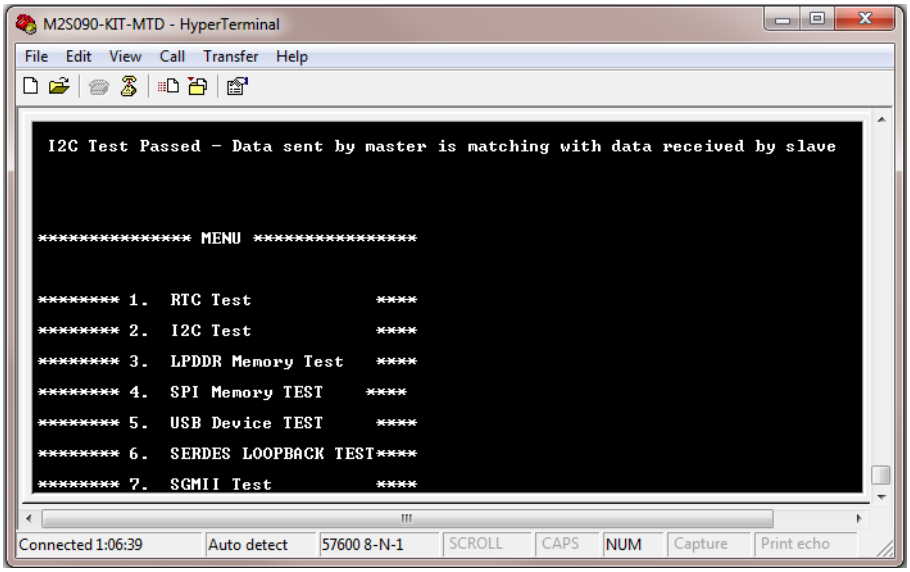
When the test is passed, the following message appears.

Figure 33 • **RTC Test Passed**



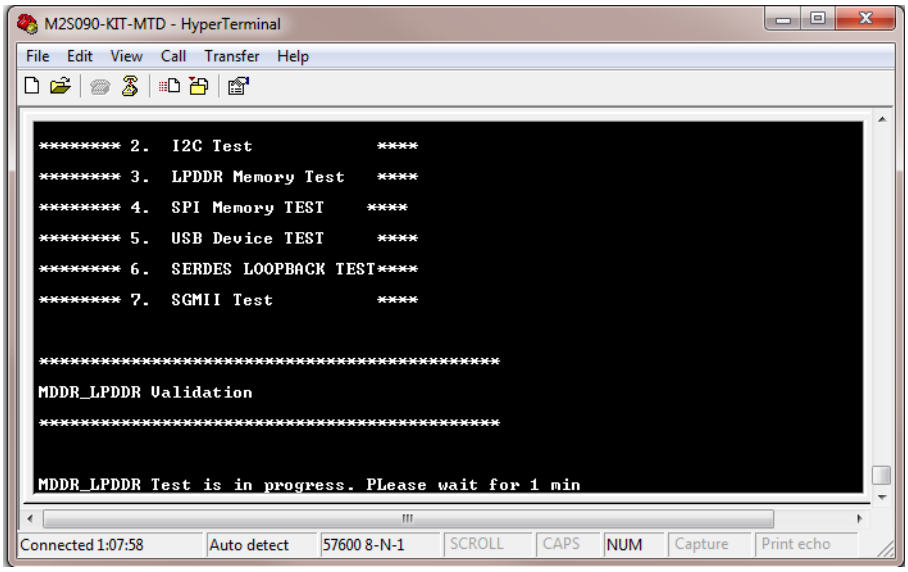
3. Press **2** to run the I2C loopback test.
   When the test is passed, the following message appears.

Figure 34 • **I2C Test Passed**



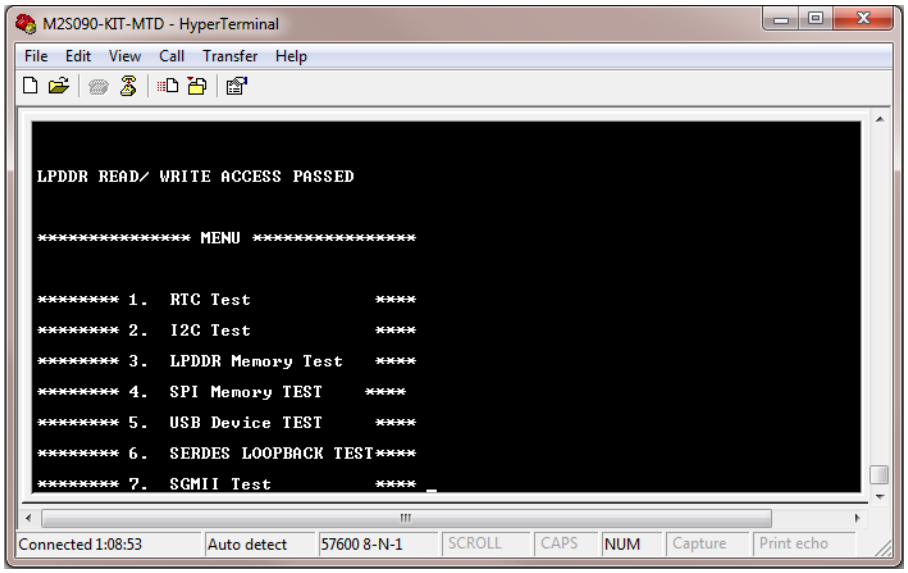
4. Press **3** to run the LPDDR memory test.
   The following message appears.

Figure 35 • **LPDDR Memory Test**



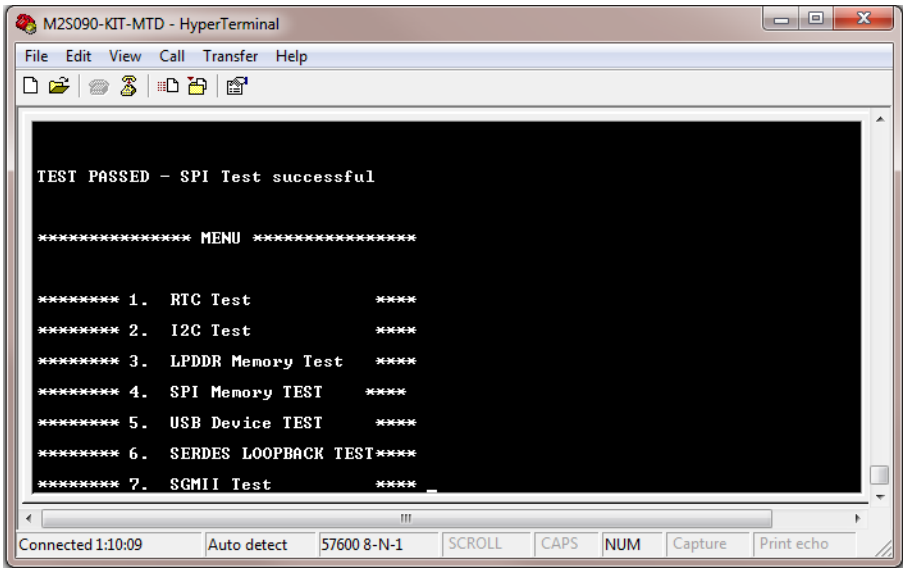
When the test is passed, the following message appears.

Figure 36 • **LPDDR Memory Test Passed**



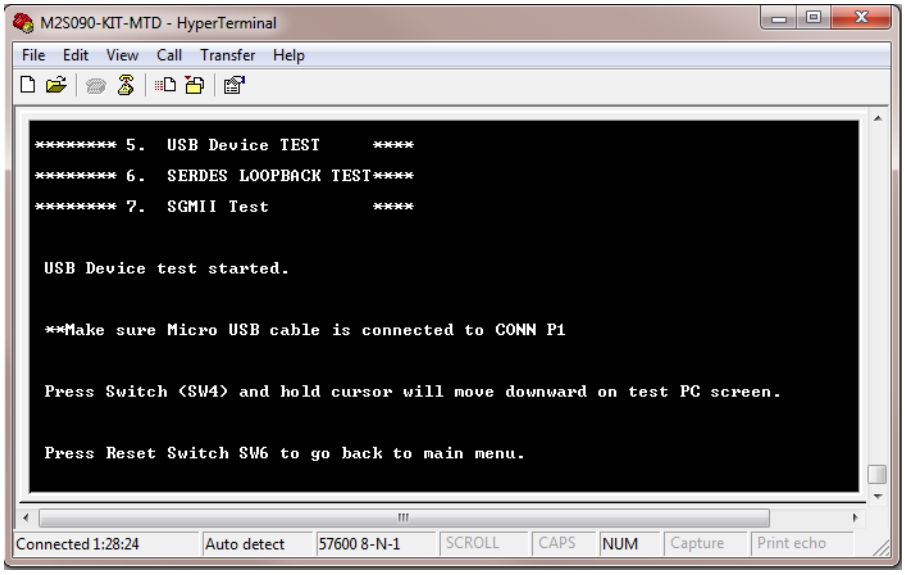
5. Press **4** to run the SPI memory test.
   When the test is passed, the following message appears.

Figure 37 • **SPI Memory Test Passed**



Press **6** to run the USB device test. When the test is passed, the following message appears.

Figure 38 • **USB Device Test Passed**

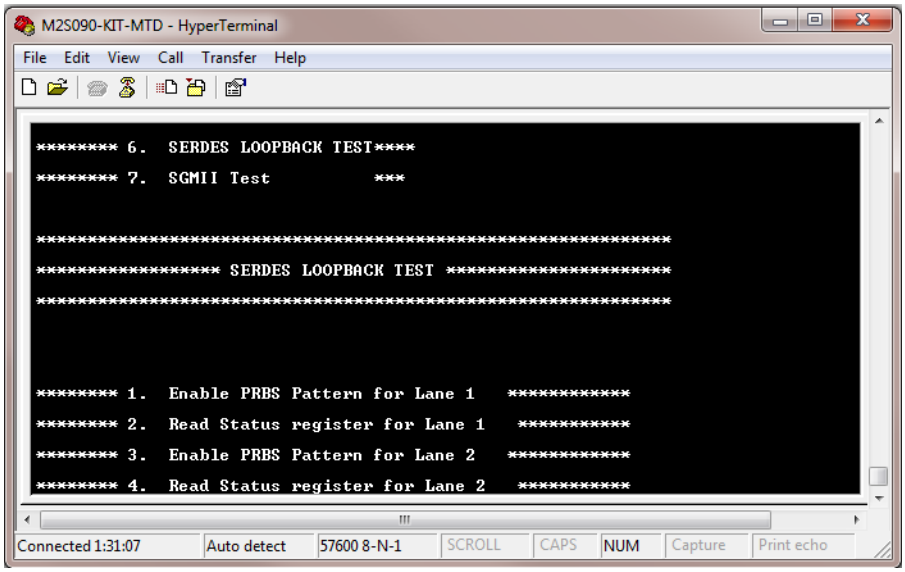


6. Press and hold the **SW2** switch on the board, and observe the mouse cursor moving to the right side.
7. Press the **SW6** reset switch to go back to the main menu.

8. Press **6** to run the SerDes loopback test shown in the following figure.

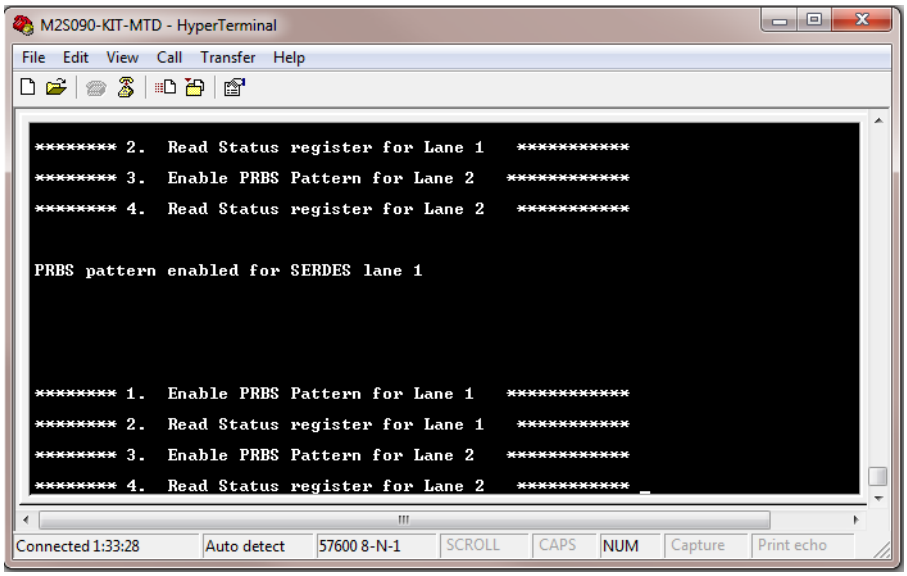
Note: Ensure that the loopback cable is connected. See Setting Up Jumpers, page 48.

Figure 39 • **SerDes Loopback Test**



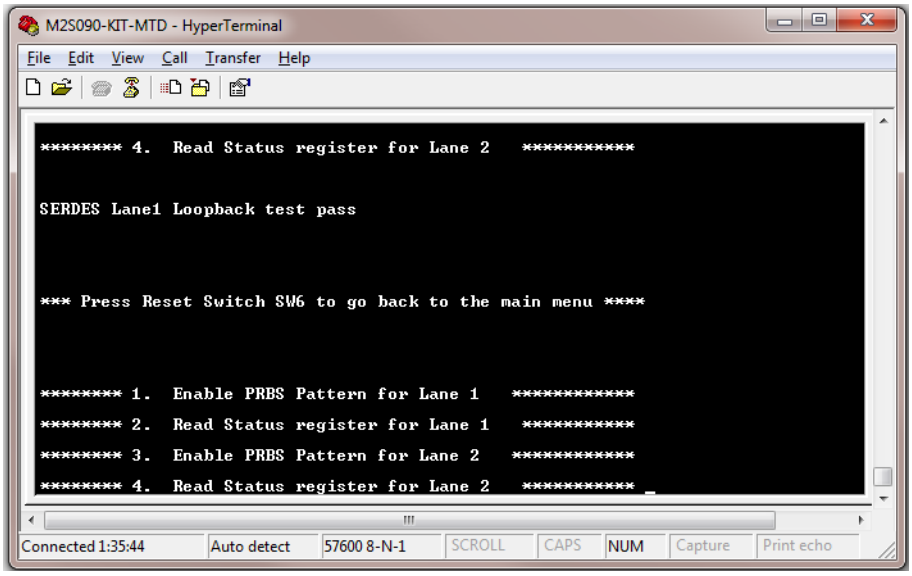
9. Press **1** to enable the PRBS pattern for Lane 1
   When the pattern is enabled, the following message appears.

Figure 40 • **SerDes Lane 1 Loopback Test**



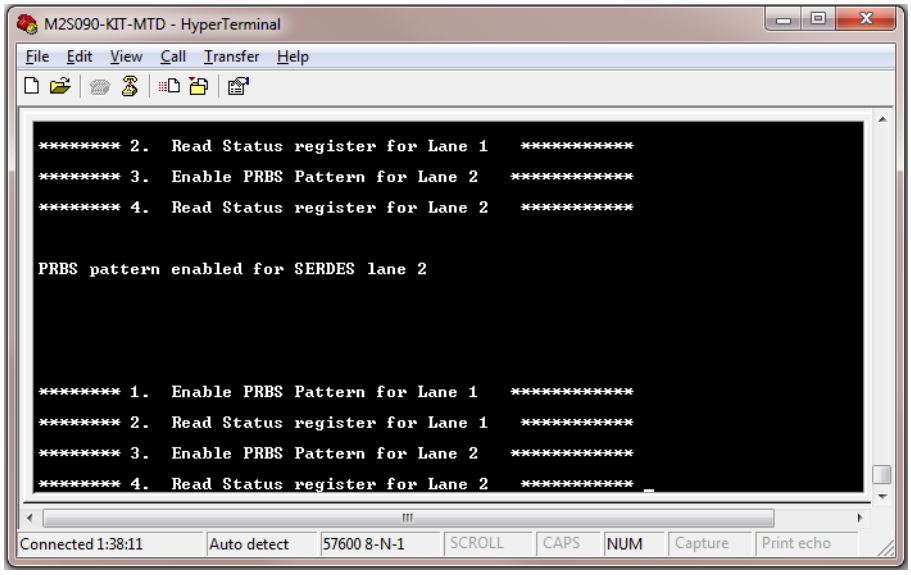
10. Press **2** to read the status register for Lane 1.
    When the test is passed, the following message appears.

Figure 41 • **SerDes Lane1 Loopback Test Passed**



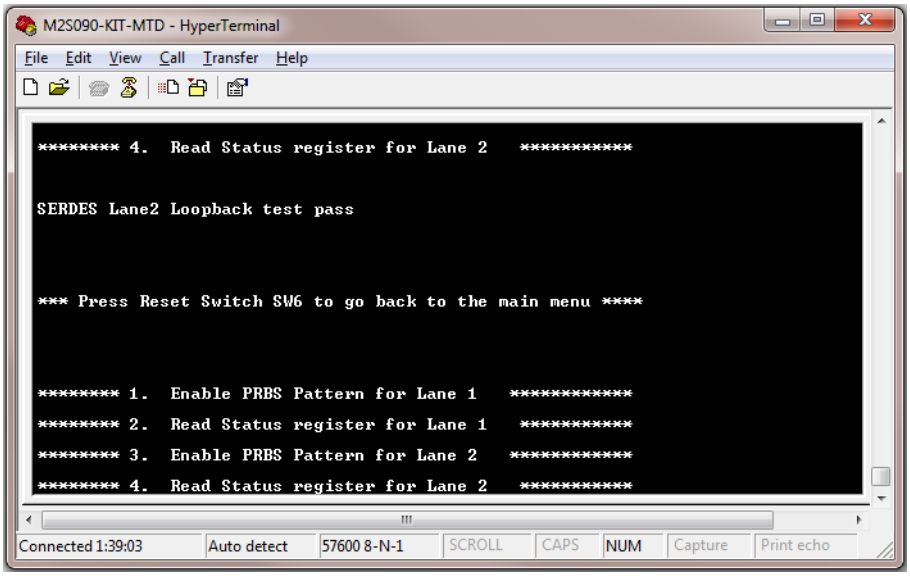
11. Press **3** to enable the PRBS pattern for Lane 2.
    When the pattern is enabled, the following message appears.

Figure 42 • **SerDes Lane 2 Loopback Test**



12. Press **4** to read status register for Lane 2.
    When the test is passed, the following message appears.

Figure 43 • **SerDes Lane 2 Loopback Test Passed**

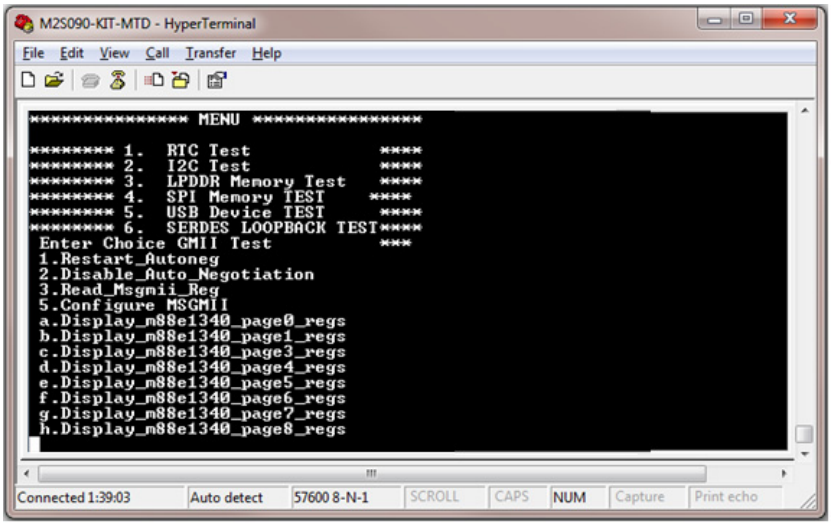


Notes:

- Ensure that SMA connectors J20 and J15 are shorted using one SMA cable, and SMA connectors J16 and J10 are shorted using a different SMA cable.
- The loopback SMA cable used must support 5 Gbps data rate.
- Follow the sequence given in the HyperTerminal.

13. Press **7** to run the SGMII test.
    The following message appears.

Figure 44 • **SGMII Test**

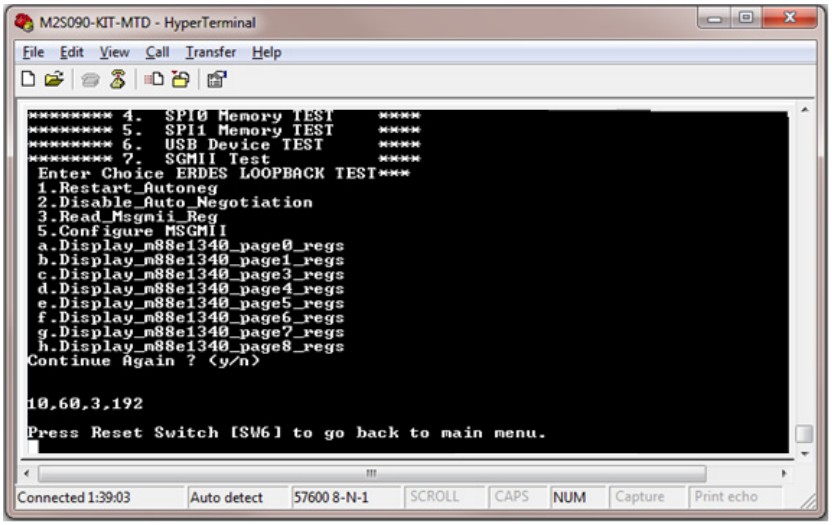


Note: If this message is not displayed, switch ON and OFF the **SW7** power supply on the board.

14. Press **7** to repeat the SGMII test.
    A confirmation message is displayed, Press **n** twice (see Figure 45, page 56).When the test is passed, the IP address of the host PC is displayed.

15. Press **2** on the terminal window, and then press **y** to repeat the SGMII test.
16. Press **n** twice on the **HyperTerminal** window. The host PC's IP address is displayed as shown in the following figure.

Figure 45 • **SGMII Test Passed**



IP address may vary from one PC to another.If the IP address is not displayed,

17. Press **SW6** to go back to the main menu.

9 Appendix: Running the PCIe Demo Design on Windows

The SmartFusion2 M2S090TS-EVAL-KIT comes with a preloaded PCIe control plane demo design. See Appendix: FPGA Programming Using FlashPro4, page 68 for information about how to reprogram the board with the PCIe control plane demo.

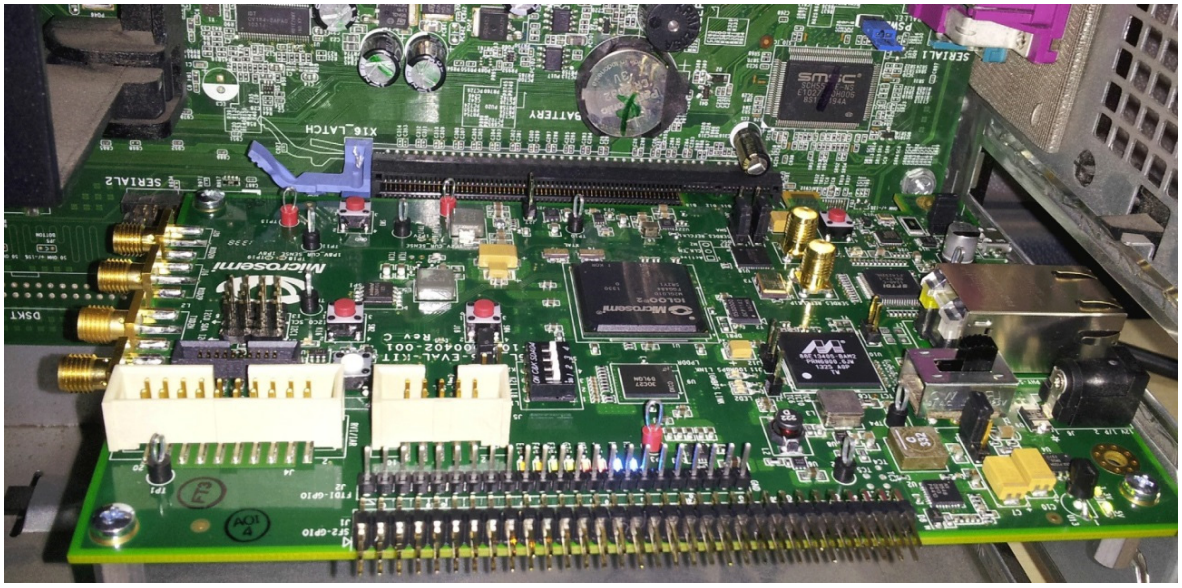
9.1 Connecting the Board to the Host PC

To connect the board to the host PC, follow these steps:

1. After successful programming, power **OFF** the SmartFusion2 Security Evaluation Board and shut down the host PC.
2. Follow these steps to connect the **CON1-PCIe Edge Connector** to a host PC or a laptop:
   - Connect the **CON1** PCIe edge connector to host PC's PCIe Gen 1 or Gen 2 slot as applicable. If the host PC does not support the Gen 2-compliant slot, the design automatically switches to the Gen 1 slot.
   - Connect the **CON1** PCIe edge connector to the laptop PCIe slot using an express card adapter. For laptops, express card adapters typically support only Gen 1, and designs work on the Gen 1 slot.

   CAUTION: The host PC or laptop must be powered OFF while inserting the PCIe edge connector. If the system is not powered OFF, PCIe device detection and selection of the device generation (Gen 1/Gen 2) may not occur properly.

Figure 46 • **SmartFusion2 Security Evaluation Kit Setup for Host PC**

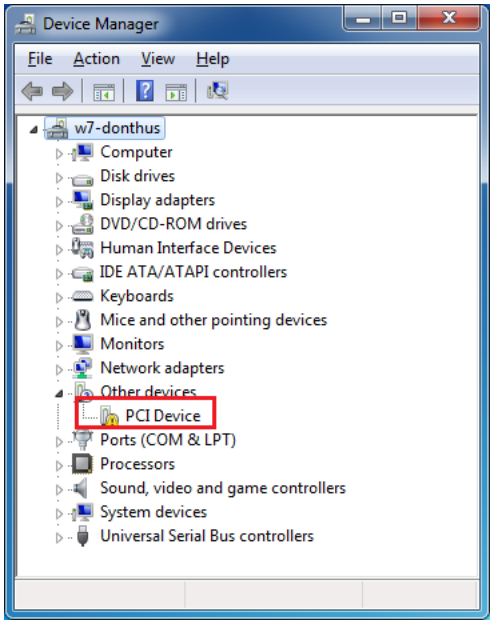


9.2 Running the Demo Design

This section describes how to run the PCIe demo design included in the SmartFusion2 Security Evaluation Kit.

1. Power on the host PC and open the host PC Device Manager for PCIe device, as shown in the following figure.

Figure 47 • **Device Manager**

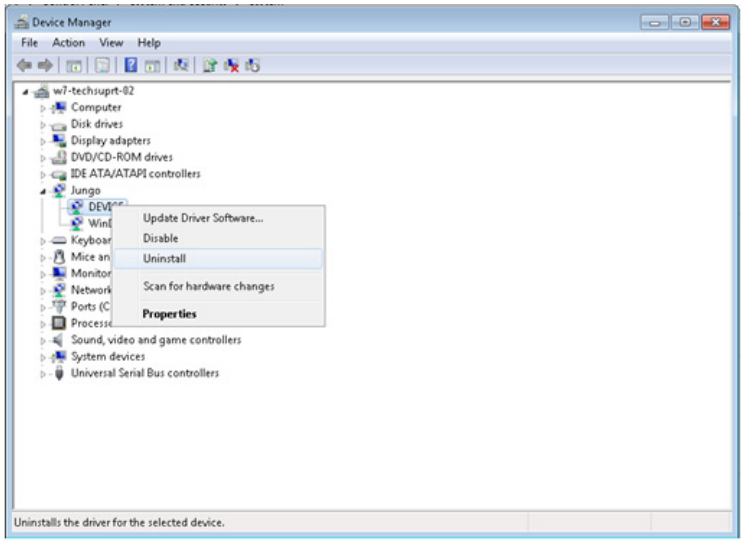


Notes:

- If the PCIe device is not detected, power-cycle the SmartFusion2 Security Evaluation board. To do this, right-click **PCIe Device** > **Scan for hardware changes** in Device Manager.
- If the device is still not detected, check if the BIOS version in host PC is the latest, and if PCIe is enabled in the host PC BIOS.
- If the host PC has any other installed drivers (previous versions of Jungo drivers) for the SmartFusion2 PCIe device, uninstall them.

2. In Device Manager, right-click **DEVICE** and select **Uninstall,** as shown in the following figure.

Figure 48 • **Device Uninstall**



The **Confirm Device Uninstall** dialog box appears.

3. Select the **Delete the driver software for this device** check box, and click **OK**, as shown in the following figure.

Figure 49 • **Confirm Device Uninstall**



After uninstalling previous Jungo drivers, make sure that the PCIe device is detected in the Device Manager window, as shown in Figure 47, page 58.

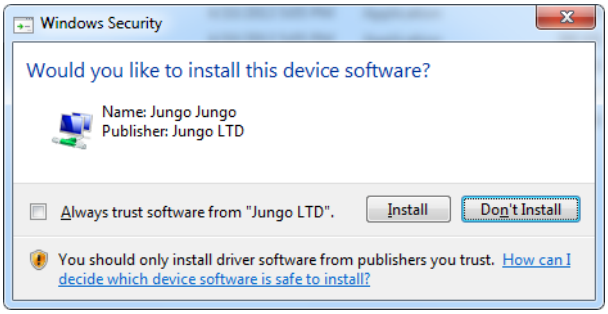
9.2.1 Installing Drivers

The PCIe Demo uses a driver framework provided by Jungo WinDriverPro. To install the latest version of the PCIe drivers for SmartFusion2 Security Evaluation Board on the host PC, follow these steps:

Note: Installation of drivers requires administrative rights on the host PC.

1. Extract the `PCIe_Demo.rar` file to the **C** drive. The file is located in the design files: **M2S150_M2S25_PCIe_Control_Plane_DF\Windows_64bit\Drivers**
2. Run the batch file `C:\PCIe_Demo\DriverInstall\Jungo_KP_install.bat`.In the **Windows Security** dialog box, click **Install**, as shown in the following figure.

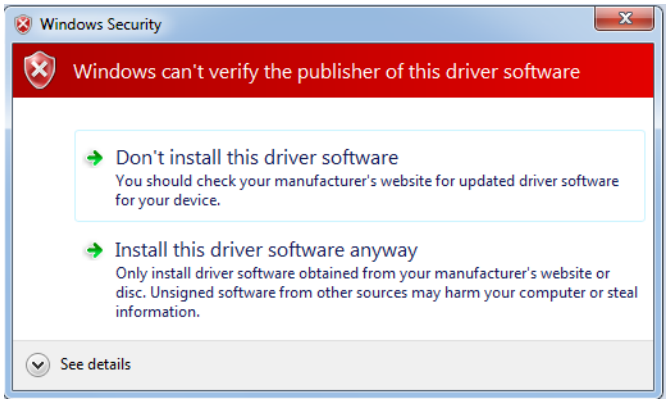
Figure 50 • **Jungo Driver Installation**



Note: If the installation does not begin automatically, right-click **Command Prompt** from the Start menu, select **Run as administrator**, and run the batch file from the command prompt.

3. Click **Install this driver software anyway**, as shown in the following figure.

Figure 51 • **Windows Security**



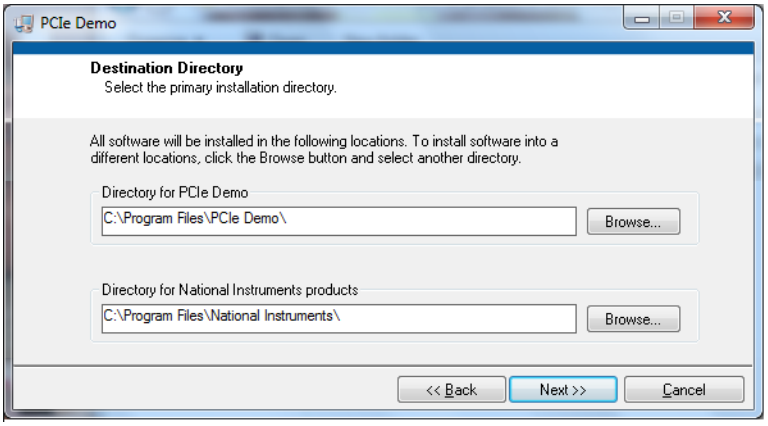
9.2.2 Installing PCIe Demo GUI

The SmartFusion2 PCIe demo GUI is a simple GUI that runs on the host PC and enables communication with the SmartFusion2 PCIe EP device. The GUI provides PCIe link status, driver information, and demo controls. It invokes the PCIe driver installed on the host PC and issues user-selected commands to the driver.

To install the GUI:

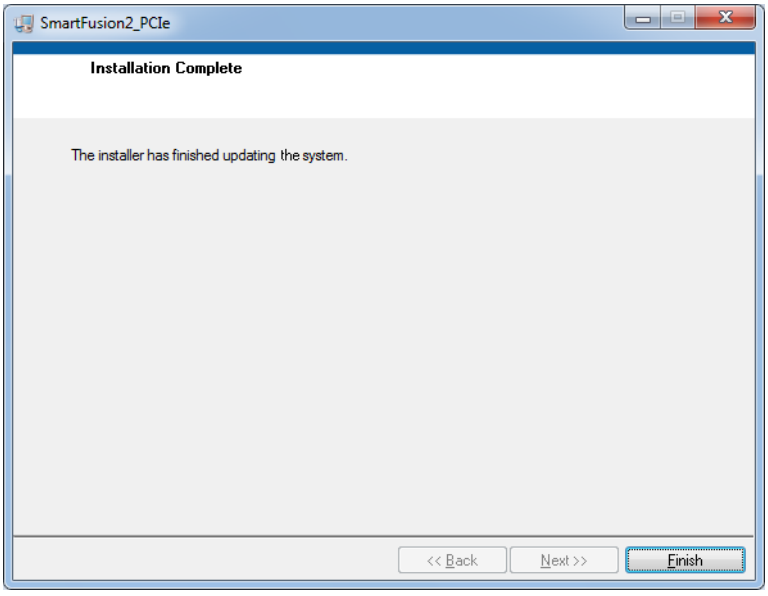
1. Extract the `PCIe_Demo_GUI_Installer.rar` from the design files located at **M2S150_M2S25_PCIe_Control_Plane_DF\Windows_64bit\GUI**.
2. Double-click the `setup.exe` file in the provided GUI installation (**PCIe_Demo_GUI_Installer\setup.exe**).
3. Retain the default directory locations shown in the following figure, and click **Next**.

Figure 52 • **GUI Installation**



4. Click **Finish** to complete the installation.
   The following window appears upon successful installation.

Figure 53 • **Successful GUI Installation**



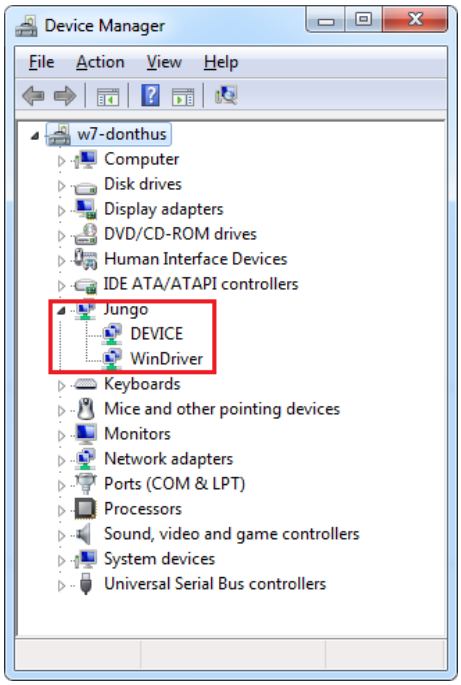
5. Restart the host PC.

9.2.3 Running the PCIe GUI

To launch the PCIe GUI and use the demo controls:

1. Check the host PC's Device Manager for the drivers. If the device is not detected, power-cycle the SmartFusion2 Evaluation Board.
2. Right-click **DEVICE > Scan for hardware changes** in Device Manager. Make sure that the board is switched ON.

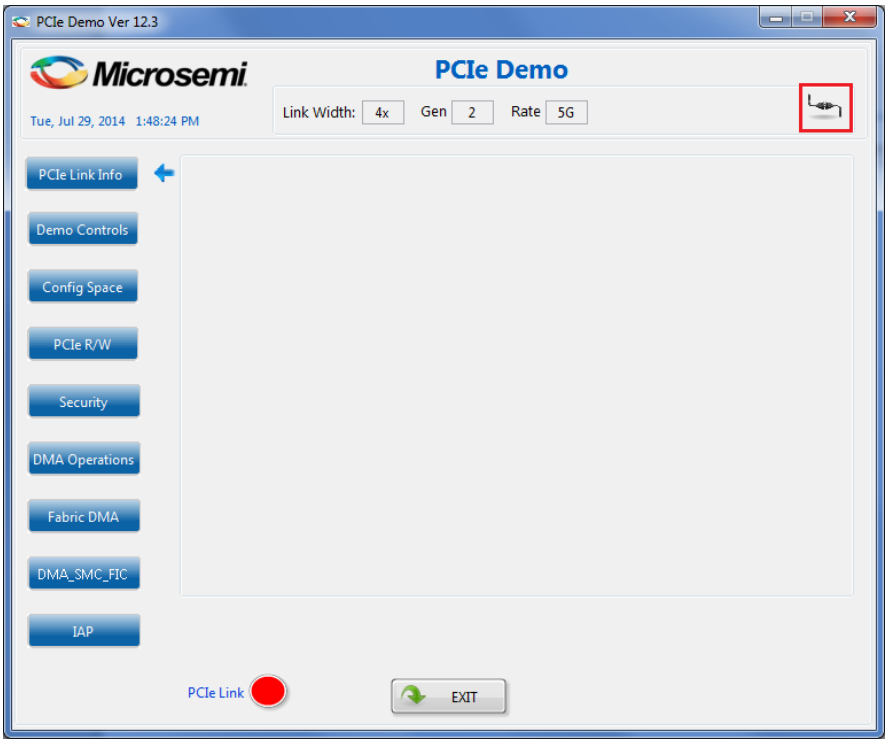
Figure 54 • **PCIe Device Detection in Device Manager**



Note: If a warning symbol is displayed on the **DEVICE** or **WinDriver** icons in the Device Manager, uninstall and reinstall the drivers (see Installing Drivers, page 59).

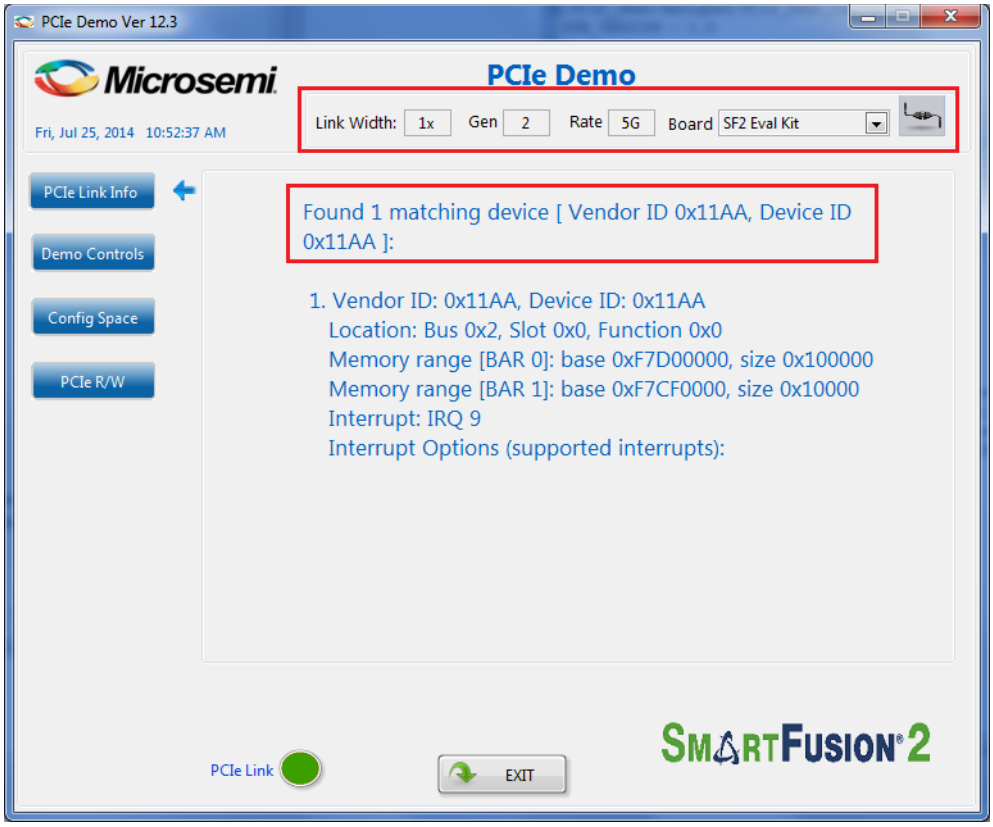
3. Open the PCIe Demo GUI (shown in the following figure) from **ALL Programs > PCIeDemo > PCIe Demo GUI**.

Figure 55 • **PCIe Demo GUI**



4. Click the **Connect** icon (highlighted in the above figure) at the top-right corner of the GUI. The link width, device generation (Gen 1/Gen 2), data rate, and kit type are displayed on the GUI, as shown in the following figure.

Figure 56 • **Version Information**

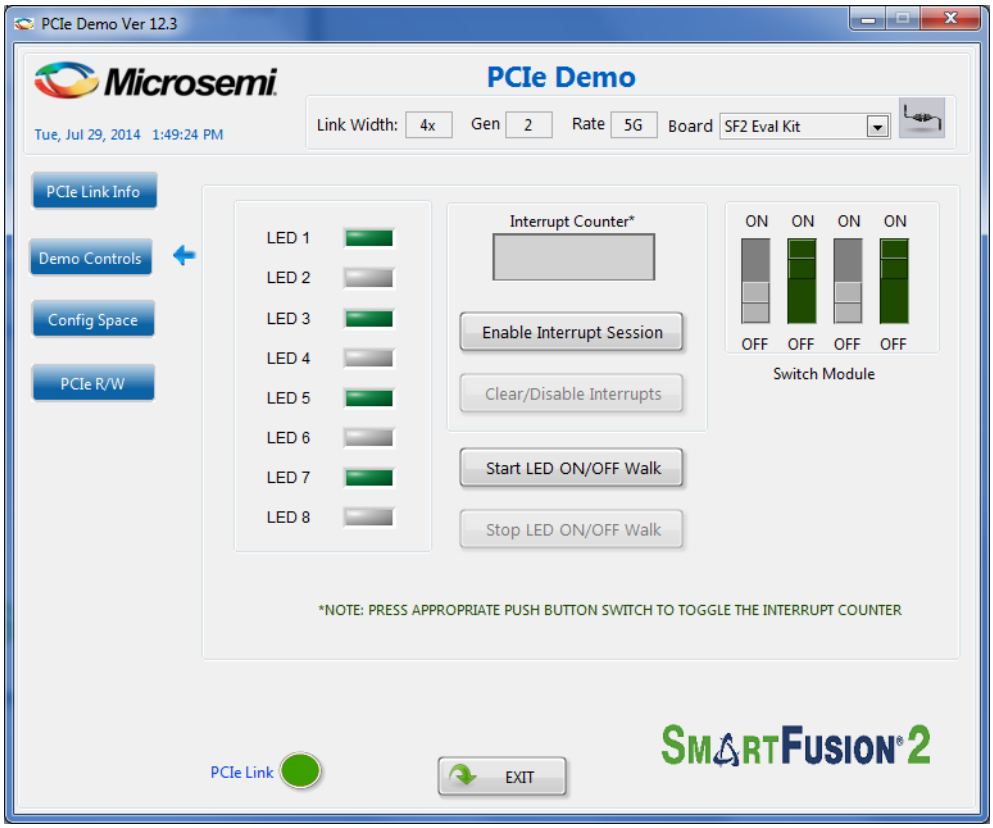


Notes:

- The SmartFusion2 Security Evaluation Kit provides x1 PCIe lane width for board configuration.
- If the host PC does not support the Gen 2 slot, the design automatically changes to the Gen 1 slot.

5. Click **Demo Controls** to display the LED options and DIP switch status, as shown in the following figure.

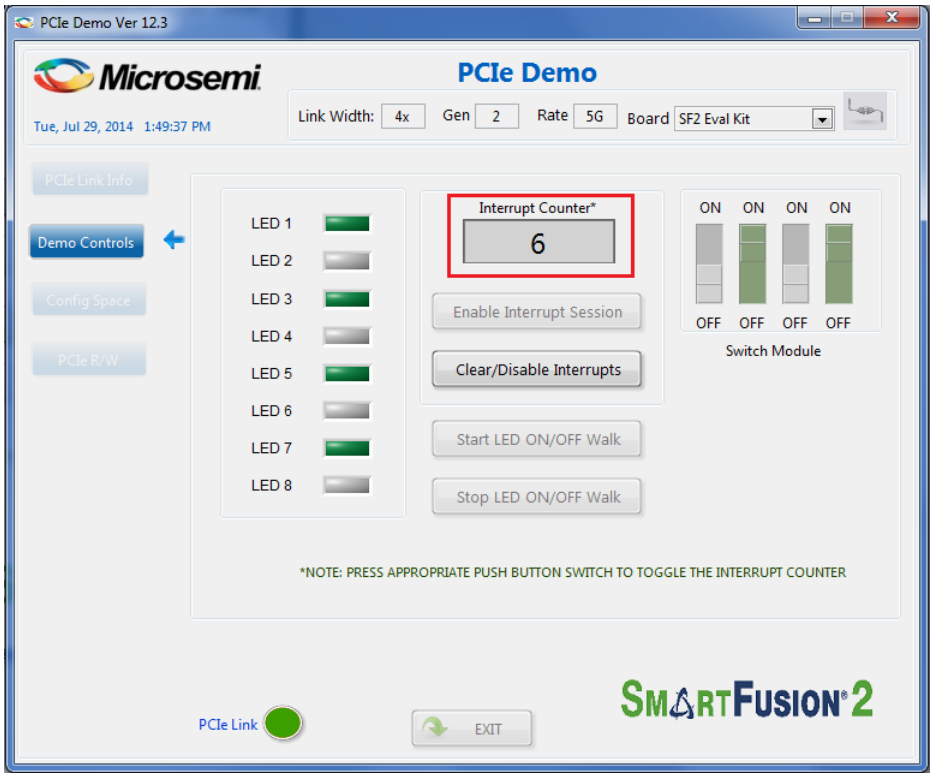
Figure 57 • **Demo Controls**



6. Click the various LEDs appearing on GUI to switch ON and switch OFF the LEDs on the SmartFusion2 Security Evaluation board.
7. Click **Start LED ON/OFF Walk** to make the LEDs on the board blink.
8. Click **Stop LED ON/OFF Walk** to stop the blinking of LEDs.
9. Change the position of DIP switches 1 to 4 on **SW5** of the board, and observe the position of those switches in **GUI SWITCH MODULE**.
10. Click **Enable Interrupt Session** to enable the PCIe interrupt.

11. Press the **SW4** push-button switch on the SmartFusion2 Evaluation Board and observe the interrupt count in the **Interrupt Counter** field, shown in the following figure.

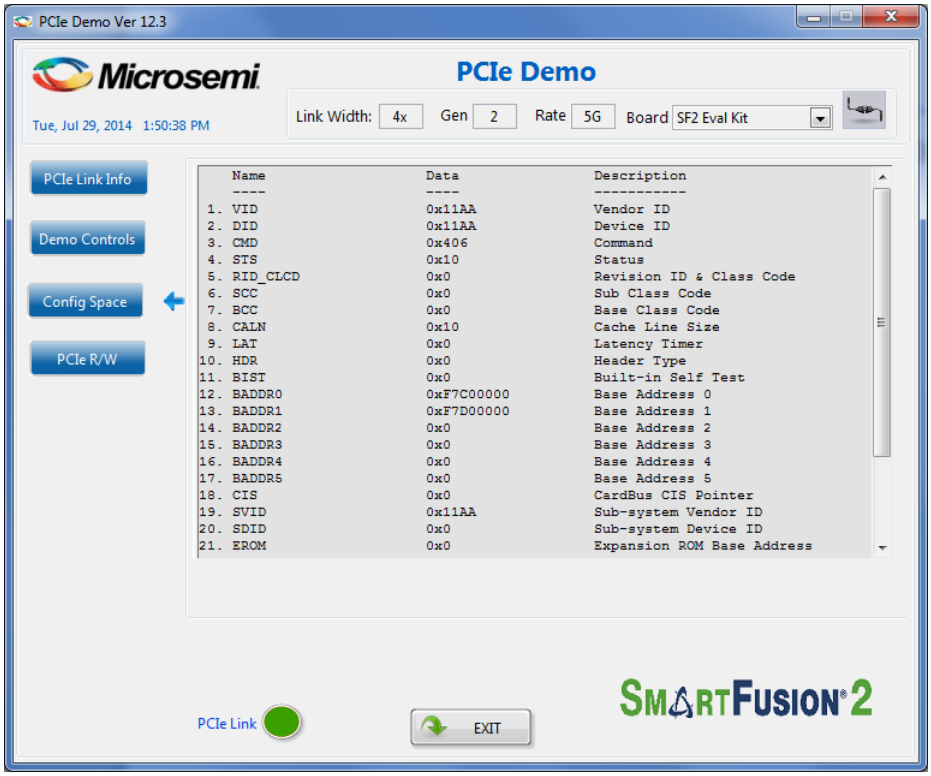
Figure 58 • **Interrupt Counter**



12. Click **Clear/Disable Interrupts** to clear and disable the PCIe interrupts.

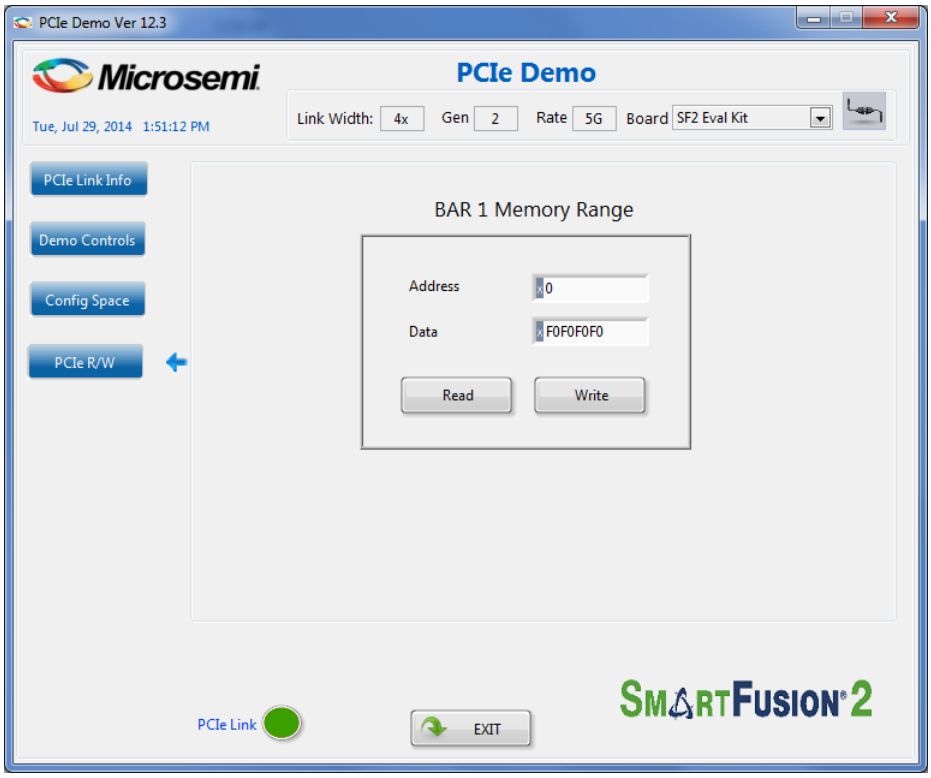
13. Click **Config Space** for details about the PCIe configuration space, as shown in the following figure.

Figure 59 • **Configuration Space**



14. Click **PCIe R/W** to perform read and writes to LSRAM memory through the **BAR1** space. The **PCIe R/W** window appears, as shown in the following figure.
15. In the **Address** field, enter an address in the 0x0000 to 0xFFFC range in the **Address** field.
16. In the **Data** field, enter a 32-bit hexadecimal value.

Figure 60 • **Read and Write to LSRAM Using PCIe**



17. Click **Exit** to quit the demo.

Note: For running the demo design on Linux, see *DG0566: SmartFusion2 SoC FPGA PCIe Control Plane Demo For Advanced Dev Kit and Evaluation Kit Demo Guide.*

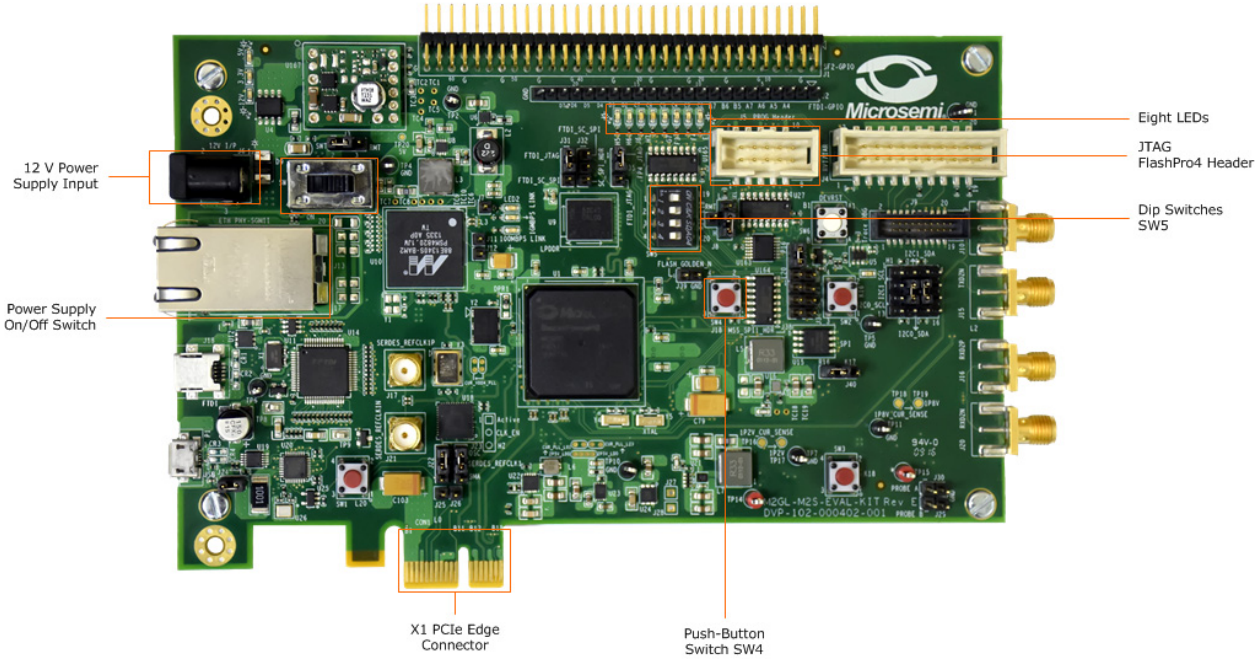
10 Appendix: FPGA Programming Using FlashPro4

The M2S090TS-EVAL-KIT can be programmed and/or debugged using the FlashPro4 programmer.

10.1 Board Setup

The following figure is a snapshot of a sample setup of the SmartFusion2 Security Evaluation Board for FlashPro4 programming.

Figure 61 • **SmartFusion2 Evaluation Board Setup for FlashPro4 Programming**



Note: The notch (highlighted in red) does not go into the adapter card.

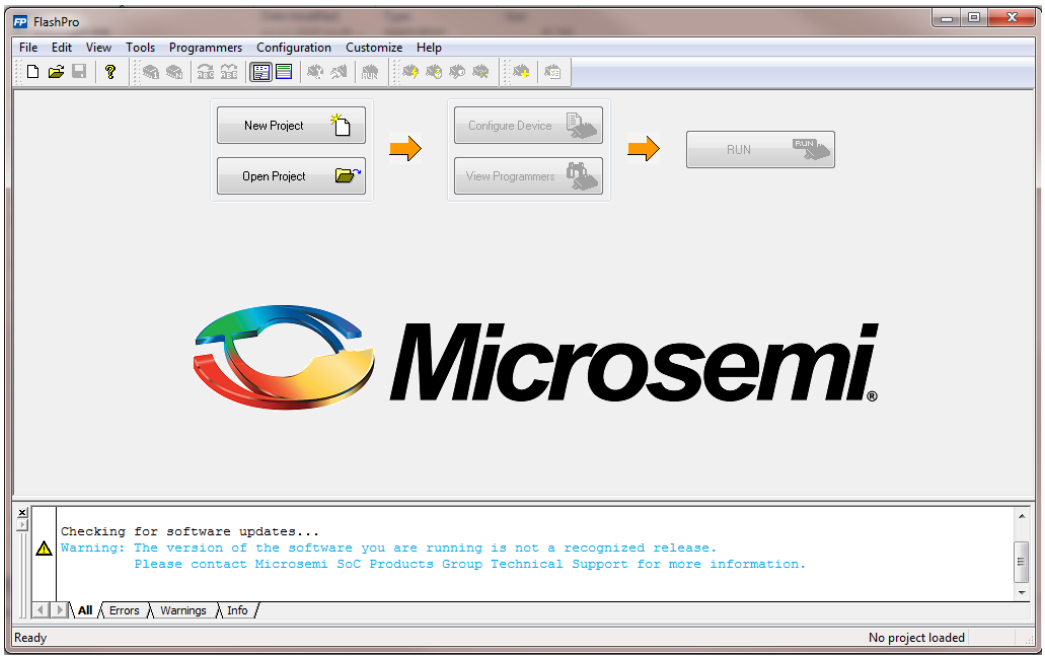
10.2 Programming the Device Using FlashPro4

FlashPro4 must be installed on the host PC to program the device using FlashPro4.

To program the board using FlashPro4, follow these steps:

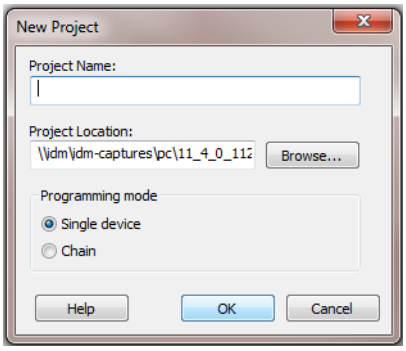
1. Connect the FlashPro4 header to the **J5** jumper.
2. Switch ON the **SW7** power supply switch.
3. Open the FlashPro software.

Figure 62 • **FlashPro Window**



4. Click **New Project** to create a new project.
   The **New Project** window appears, as shown in the following figure.

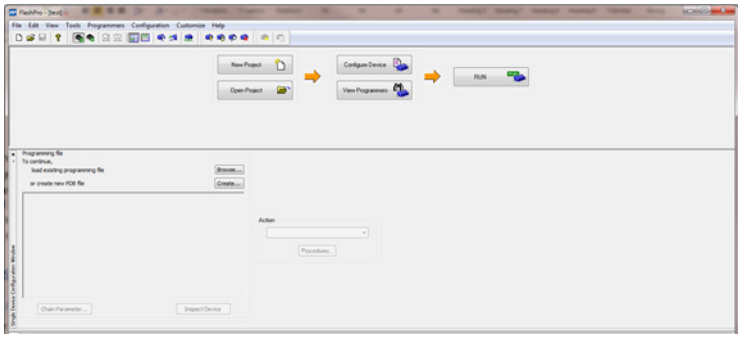
Figure 63 • **Creating a New Project**



5. Enter the **Project Name**.
6. **Select Single device** as the programming mode, and click **OK**.

7. Click **Configure Device**.

Figure 64 • **Configuring the Device**



8. Click **Browse,** and select the `M2S090_EVAL_KIT_MTD_top_rev1.stp` file from the **Load Programming File** window.
9. Click **Program** to program the device.
   When the device is programmed successfully, a **Run Program PASSED** status is displayed.