PD70210/ PD70210A

Designing a Type-1/2 802.3 or HDBT type 3 PD using PD70210/ PD70210A ICs Application Note

Introduction

The following document provides guidelines for designing a PoE system Powered Device (PD) compliant with IEEE 802.3af (IEEE802.3at Type 1), or 802.3at (Type 2), standards or HDBASET POH standard (Type 3) using Microsemi's PD70210/A/AL Front-End ICs.

PD70210/A/AL Front-End IC provides the necessary detection, classification, 2-event mark for "AT" flag, and operating current levels compliant with IEEE 802.3at Type 2 standard and POH Type 3 standard 3-event mark for "HD flag".

PD70210A has PD70210 features plus a Wall adapter input connection feature, it enables a wall adapter input to switch off the POE isolation switch. PD70210AL is functionally similar to PD70210A with larger package and higher current support.

This document includes a brief overview of PoE functionality with respect to the applicable standards; however it is not to be considered a substitute for IEEE standards. Applicable standard should always be consulted when making decisions affecting the design of the circuit.

Microsemi offers a Complementary product for high power POE applications, which is an Ideal Diode bridge PD70224, this diode bridge is a low loss solution for the POE dual diode bridges. Please consult Microsemi site for additional information.

To complete PD70210 family, Microsemi also offers PD70211 Front-End plus PWM controller IC combined in a single 36-Pin QFN 6x6mm package in which PD70210A die is combined as its PD front end.

Applicable Documents

- IEEE802.3at-2009 standard, DTE Power via MDI
- PD70210/PD70210A/PD70210AL datasheet DS_PD70210_PD70210A
- PD70210 and PD70224 EVB user guide PD70210EVB_UG
- PD70210AL and PD70224L EVB user guide PD70210ALEVB_UG

PD70210/A/AL Features

- HDBASET Type 3 Compliant
- IEEE802.3 Type 1 and Type 2 backward Compliant
- Supports up to 0.95A 4 pair systems (95W HDBASET) with a single PD70210AL
- Supports up to 0.72A 4 pair systems with a single PD70210/A
- Provides PD Detection Signature
- Programmable PD Classification Signature
- Supports 1,2 and 3 Event Classification Flag
- Supports 2 or 4 Pair powering Flag
- Integrated Isolation Switch
- 24.9KΩ signature resistor disconnection when power is on, for power saving

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- Inrush Current Limit (Soft Start)
- Integrated 10.5V Start-up Supply Output for DC-DC Converters
- Short Circuit Protection
- Internal Discharge Circuitry for DC-DC Bulk Capacitor
- Wall adapter input switching- PD70210A and PD70210AL
- Wide Temperature Operating Range -40°C to +85°C
- On-Chip Thermal Protection

POE Overview

In its simplest form, PoE consists of a power source, referred to as Power Source Equipment (PSE), an Ethernet cable (typically contained in an infrastructure) with maximum length of 100 meters, and a Powered Device (PD) which accepts both data and power from the Power Interface (PI) of the Ethernet cable. PI is typically an eight pin RJ45 type connector. A diagram of this arrangement is shown in Figure **1**.

IEEE 802.3af (IEEE 802.3at type 1) PSEs are designed to operate with Ethernet cabling which may include CAT3 (per TIA/EIA 568). As such they may contain a 26AWG wire. A cable of this type may impose a 20Ω maximum power loop resistance to a PSE operating into the maximum specified 100 meter cable length.

IEEE 802.3at type 2 PSEs are designed to operate at higher output power levels with CAT 5 or higher (per TIA/EIA 568) Ethernet cabling. These cables contain 24AWG wire (or better) and may impose a maximum 12.5Ω power loop resistance to a PSE operating into the maximum specified 100 meter cable length. The voltage drop and internal temperature rise created in a 100 meter Ethernet cable affect the voltage and current available to the PD. A brief comparison between the AF and AT standards for the PSE and the PD are presented in Table 1 and Table 2, respectively.

HDBASET standard follows IEEE 802.3at type 2 cable types, however due to its higher supported current, it limits the number of cables in a single cable Bundle.

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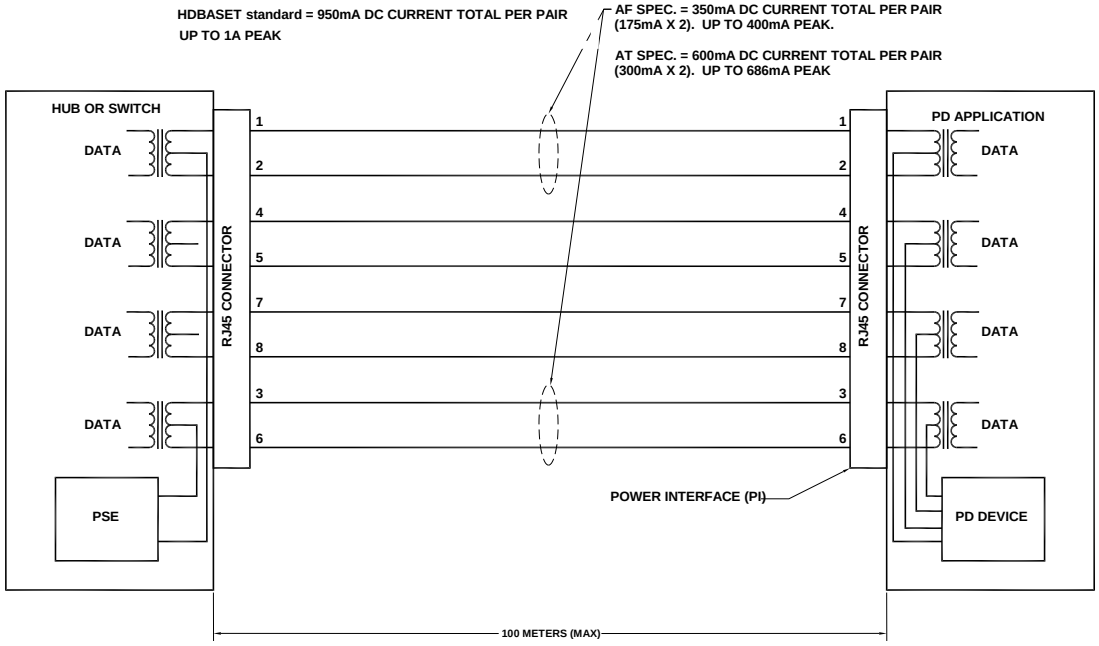
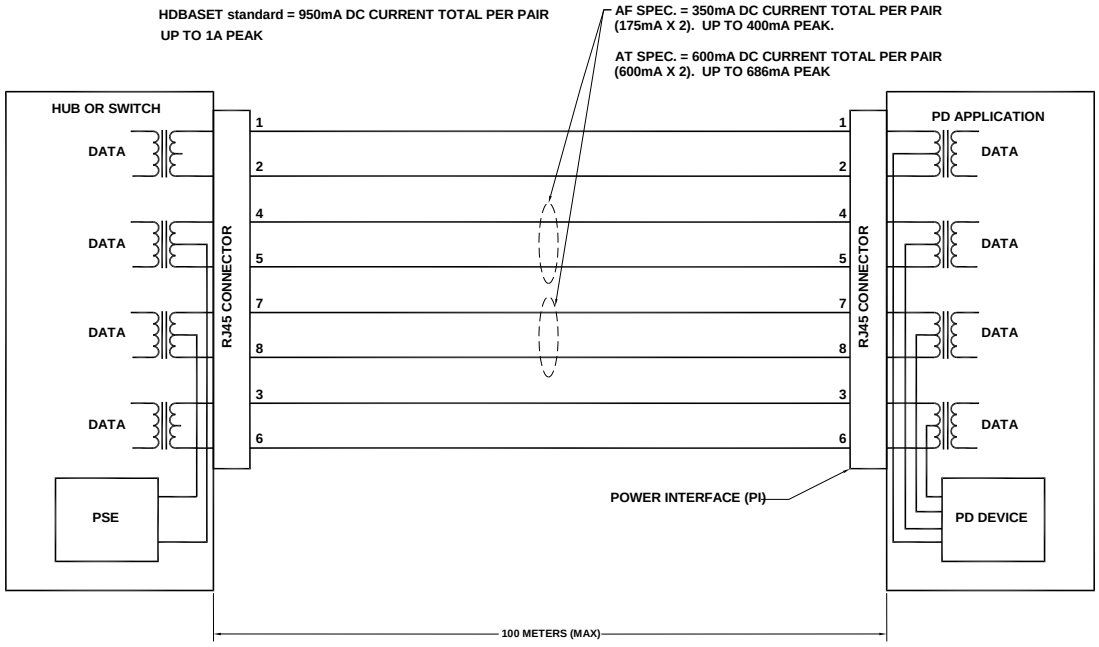


Alternative A



Alternative B

Figure 1: Basic PoE Configuration for IEEE 802.3at Standard

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Comparison of IEEE 802.3af/ IEEE 802.3at and HDBASET Standards for PSE				
PSE Requirements	**IEEE 802.3af or IEEE 802.3at type 1**	**IEEE 802.3at type 2**	**Single HDBASET**	**Twin HDBASET**
Guaranteed Power at PSE Output	15.4W	30W	47.5W	95W
PSE Output Voltage	44V to 57V	50V to 57V	50V to 57V	50V to 57V
Guaranteed Current at PSE Output	350mA DC with up to 400mA peaks	600mA DC with up to 686mA peaks	950mA DC with up to 1000mA peaks	2x 950mA DC with up to 2000mA peaks
Maximum Cable Resistance	20Ω	12.5Ω	12.5Ω	12.5Ω
Physical Layer Classification	Optional	Mandatory	Mandatory	Mandatory
Supported Physical Layer Classification Classes	Class 0 to 4	Class4 mandatory	Class4 mandatory	Class4 mandatory
Data Link Classification	Optional	Optional	Optional	Optional
2-Events Classification	Not required	Mandatory	Not required	Not required
3-Events Classification	Not required	Not required	Mandatory	Mandatory
4 pairs power feeding	Not allowed	Allowed with 2 collocated PSEs	NA	Allowed
Communication Supported	10/100 BASE-T (Midspan) 10/100/1000 BASE-T (switch)	10/100/1000 BASE-T Including Midspans (Both type1 and type2)	10/100/1000/ 10000 BASE-T	10/100/1000/ 10000 BASE-T

Table 1: IEEE 802.3af, 802.3at and HDBASET Standards for PSE

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Comparison of IEEE 802.3af and IEEE 802.3at Standards for PD			
PD Requirements	**IEEE 802.3af or IEEE 802.3at type 1**	**IEEE 802.3at type 2**	**HDBASET spec Type 3**
Guaranteed Power at PD Input	12.95W	25.50W	95W after 1m cable 72.40W after 100m cable
PD Input Voltage	37V to 57V	42.5V to 57V	38.125V to 57V
Guaranteed Current at PD Input	350mA DC with up to 400mA peaks	600mA DC with up to 686mA peaks	950mA DC with up to 1000mA peaks
Physical Layer Classification	Mandatory (no class = Class 0)	Mandatory	Mandatory
Supported Physical Layer Classification Classes	Class0 to 4	Class4 mandatory	Class4 mandatory
Data Link Classification	Optional	Optional	Optional
2-Events Classification	Not required	Mandatory	Optional
4 pairs power receiving	Allowed	Allowed	supported
Communication Supported	10/100 BASE-T (Midspan) 10/100/1000 BASE-T (switch)	10/100/1000 BASE-T Including Midspans (both type1 and type2)	10/100/1000/10000 BASE-T

Table 2: IEEE 802.3af and 802.3at Standards for PD

PSEs can supply power on the RJ45 PI through either the RX and TX wire pairs (pins 1-2 and 3-6, respectively for 10/100 Base-T), or the spare pairs (pins 4-5 and 7-8). For 1000 Base-T connections, power can be present on the same pin combination. However the spare pair terminology is eliminated as data is transmitted on all pairs. Power through wire pairs can be of either polarity. To accommodate all possible combinations of PoE power available at the PI, a use of dual diode bridges on the PD side is required.

IEEE802.3 and HDBASET standards define a method of determining whether a cable is disconnected, connected to a non-Power receiving capability device, or connected to a Power receiving capability device – a compliant PD.

IEEE802.3 and HDBASET standards further define a method of determining power requirements of the connected PoE-compliant PD, and a method by which the PD may determine the power level that is supported by the PSE.

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These determining methods are accomplished in Classification Phase . The determining events are triggered at different voltage levels, all of which occur before PSE applies the nominal PoE voltage levels specified in Table 3. Nominal operating voltage is not applied if a valid signature is not present during the Detection phase.

A diagram of the Detection, Classification, and Power-up sequences is shown in Figure 2.

PSE initially operates in an idle state, in which PI is unpowered, with an exception of a periodic detection signal “looking” for a valid detection signature. Signal levels presented at the PI during Detection phase are of sufficiently low levels for not causing damage to non-PoE devices. During Detection phase, a PoE-compliant PD will provide a valid detection signature using two components, each located on the output side of the diode bridges. A capacitor of 50nF to 120nF connected across the diode bridge output terminals, and a 25kΩ resistor, switched across the diode bridge output terminals, and present only during Detection phase.

After a valid signature is detected, PSE may start Classification phase. Classification phase is optional for 802.3af and 802.3at type 1 PSEs and PDs; however it is mandatory for 802.3at type 2 and HDBASET POH standard PSEs and PDs. Classification signature is achieved by means of a programmed current draw, set by the PD corresponding to one of 5 classes. The programmed current draw is required to be at a valid level and remains constant throughout Classification period. Class levels and their corresponding currents are outlined in Table 3.

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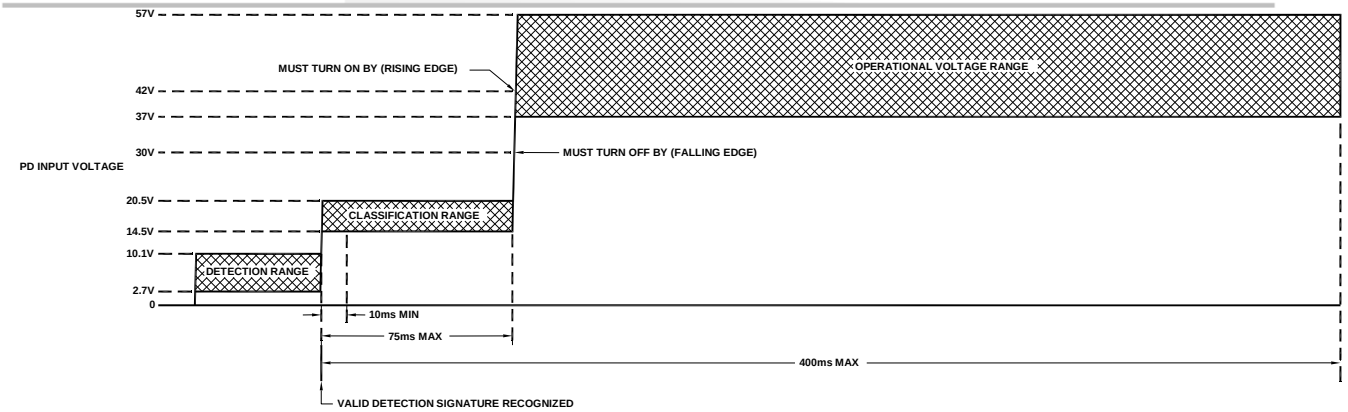
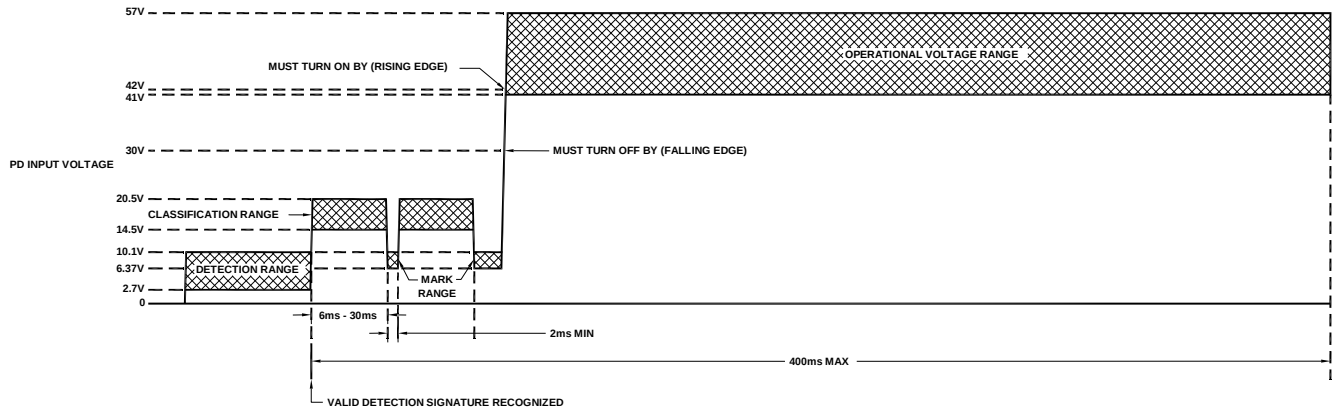


802.3af and 802.3at TYPE 1 PD INPUT REQUIREMENTS



802.3at TYPE 2 and HDbaseT PD INPUT REQUIREMENTS

Figure 2: Basic PoE Detection, Classification, and Power-Up Sequences for 802.3at standards

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Classification Current Definitions Note: PD Input Voltage During Classification Phase = 14.5V to 20.5V					
Class	**Usage**	**Maximum PD Power**	**PD Current Draw During Classification**		
			Min	**Average**	**Max**
0	Default	0.44W to 12.95W	0		4mA
1	Optional	0.44W to 3.84W	9mA	10.5mA	12mA
2	Optional	3.84W to 6.49W	17mA	18.5mA	20mA
3	Optional	6.49W to 12.95W	26mA	28mA	30mA
4	Classify AT type 2 and HDBASET Type 3 (AT compliant PD)	AT level/ HDBASET level based on number of class fingers	36mA	40mA	44mA

Table 3: Classification Current Definitions

In addition to hardware-generated (physical layer) classification outlined above, IEEE802.3 and HDBASET standards define a Data Link Layer (DLL) classification, established through Ethernet data link after PD power-up occurs. DLL classification may be used by 802.3af or 802.3at type 1 PDs optionally, but *shall* be used by 802.3at type 2 and HDBASET type 3 PDs.

A second Classification phase is required only for IEEE 802.3at type 2 compliant PSEs and PDs.

A third Classification phase is required only for HDBASET POH type 3 compliant PSEs and PDs

Classification phase serves in informing the PD whether PSE is 802.3at type 2/HDBASET Type3 compliant or not. An AT type 2 compliant PSE will provide a “2-Events Classification” signature during Classification phase. The 2-Events Classification signature toggles the input voltage between standard classification voltage range and lower voltage “mark” level. PSE voltage is toggled twice between these two voltage ranges to indicate PSE is 802.3at type 2 compliant. AT type 2 compliant PD is required to recognize the 2-event classification, and provide to internal circuits AT flag signal that indicates PD is connected to an AT type 2 compliant PSE.

HDBASET type 3 compliant PD is required for recognizing the 3-event classification, and provide to internal circuits HDBASET flag signal that indicates PD is connected to an HDBASET type 3 compliant PSE.

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Should the port voltage present at the PI drops below 2.8V, PSE class information resets and PD must reset the class dependent flag.

Once Detection and Classification phases are complete, PSE will provide a specified operating voltage at a maximum current level determined by the PSE itself.

IEEE and HDBASET standards require normal operation voltage that will be established by the PSE within 400ms of a valid detection signature.

During normal operation, PD must provide a signature to inform the PSE it is still present and requires power. This signature is referred to as “Maintain Power Signature” (MPS). MPS is defined as a minimum current draw by the PD, lasting a minimum period of 60ms, and occurring at least once every 400ms. If a valid MPS is not detected by the PSE, it will disconnect the power from the PI, return to an idle state, and start Detection phase. A diagram of the Maintain Power Signature is shown in Figure 3.

All compliant PDs contain an isolating switch that disconnects the return side of the PD from the PI during Detection and Classification phases, or during power loss. PD is required to turn on the isolating switch at PI voltage levels of ~42V or higher, and turn off the isolating switch at PI voltage levels of ~30V. In case PD circuit output is connected to a bulk capacitor of 180µF or more, PD must actively limit the current during start-up to 350mA or less. A block diagram illustrating a basic PD circuit is shown in

Figure 4: Basic PD Block Diagram.

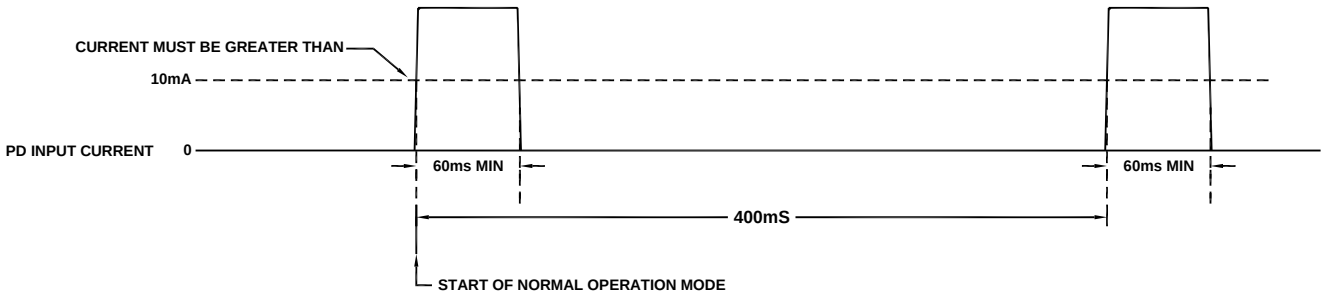

Figure 3: PoE Maintain Power Signature (MPS) Requirements

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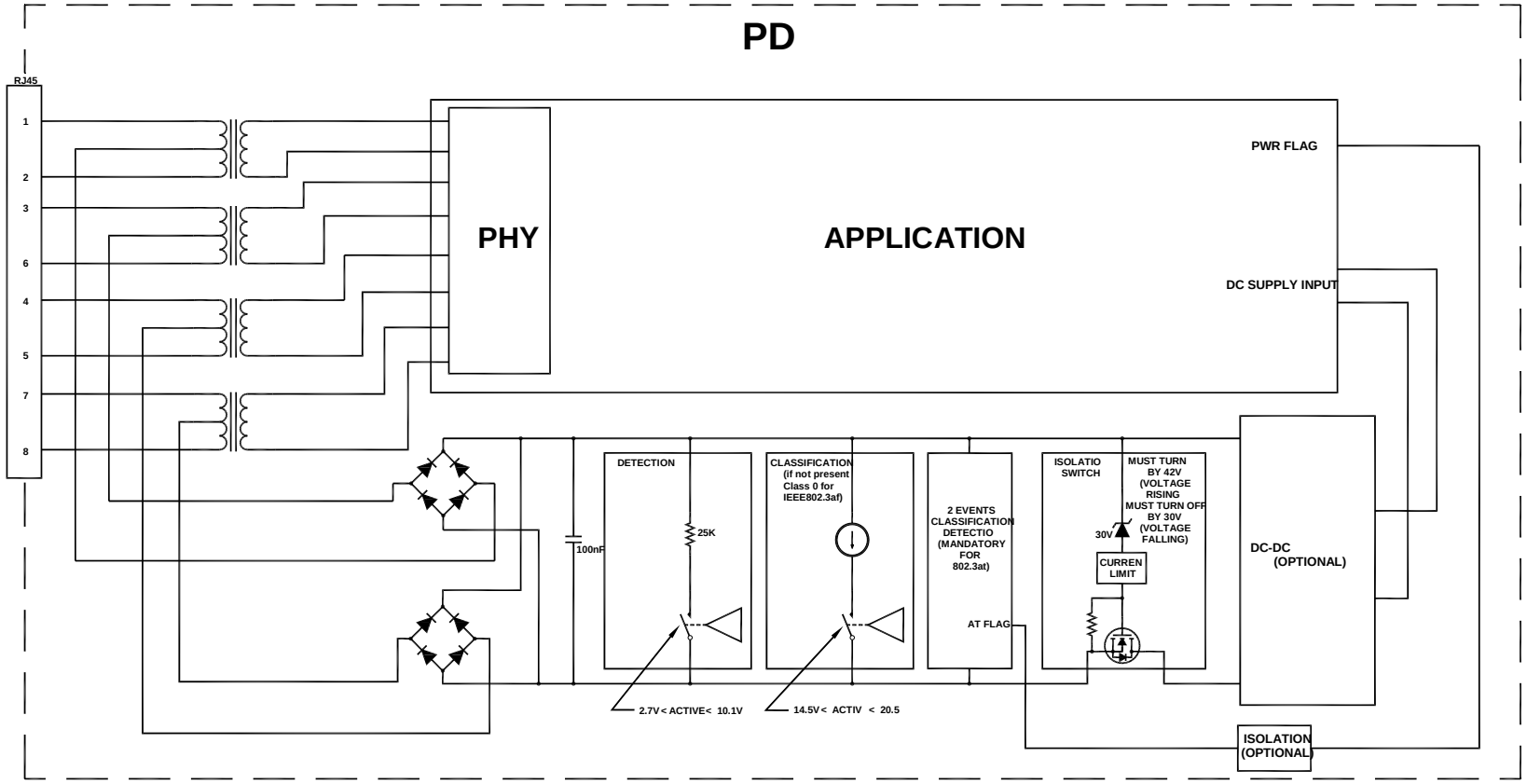

Figure 4: Basic PD Block Diagram

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Using PD70210 IC

PD70210/A/AL Front-End IC provides the necessary Detection, Classification, and Isolation Switch control functions for a PoE-powered device conforming to 802.3at type 1 (IEEE 802.3af), 802.3at type 2, or HDBASET type 3 standard.

PD70210/A/AL IC may be used for 2/4 pair systems (see Figure 5).

A single PD70210/A/AL IC placed between diode bridges and the input capacitor for the DC/DC converter.

A output terminal from the two diode bridges is connected to PD70210/A/AL IC at V_{PP} (positive connection, pin 1), and VPN_{IN} (negative connection, pin 7,8).

A capacitor is required across the positive and negative output terminals of the paralleled diode bridges. PD70210/A/AL output connections to the DC/DC converter/application are made at V_{PP}, and VPN_{OUT}.

VPN_{OUT} is the application ground connection to the integrated isolation switch of PD70210/A/AL IC.

In addition to the basic input/output connections, the following components are required for a typical application:

- **Detection Resistor:** Connect a 24.9kΩ ±1% resistor between V_{PP} and R_{DET} pin. This resistor is used to satisfy the Detection signature. A low wattage type may be used as there is less than a 7mW stress on this resistor while Detection phase is active, and the resistor is disconnected after power is on.
- **Reference Resistor:** Connect a 60.4kΩ ±1% resistor between R_{REF} pin and VPN_{IN}. This resistor should be located close to the PD70210/A/AL IC. A low wattage type may be used (resistor stress there is less than 1mW).
- **Classification Current Resistor:** The value of this resistor determines the PD current draw during Classification Phase. Values corresponding to IEEE compliant classification levels are shown in data sheet. Connect this resistor between R_{CLASS} pin and $VPN_{IN.}$
- **Input capacitor:** a 100nF/100V ceramic capacitor should be connected between V_{PP} pin and $VPN_{IN.}$ This capacitor should be located as close as practical to the device. Between V_{PP} and VPN_{IN} pins.
- **Input TVS:** a 58V TVS should be connected in the device input between V_{PP} pin and $VPN_{IN.}$
- **SUPP_S1 and SUPP_S2 Resistors:** a 10K ohm resistor connected in serial to each of the input pins SUPP_S1 and SUPP_S2.
- **Classification Current Resistor:** The value of this resistor determines the PD current draw during Classification Phase. Values corresponding to IEEE compliant classification levels are shown in Table 4. Connect this resistor between R_{CLASS} pin and $VPN_{IN.}$
- **Power Good Pull-up (PD70210 only):** Power Good signal is available at P_{GOOD} pin. After startup, a P_{GOOD} flag is generated low voltage to inform the application DC/DC converter that the power rails are ready. This is an open drain pin. Pull-up voltage on this pin is limited to 20V. Power Good can be pulled up by the bootstrap winding of the DCDC.

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- **All other Flags**

  The flags are typically sampled by the application to decide upon the maximum power to consume. These flags are open drain pins. Pull-up voltage on these pins is limited to 20V. The flags can be pulled up by the bootstrap winding of the DCDC.

  Flags state is set only once at port startup. If SUPP_S1 and SUPP_S2 pins are changing after port turn on, the flags do not change accordingly

  Flags functionality is as follows:

  - AT_FLAG pin: This flag goes high when a Type 2 PD-PSE mutually identifies each other via classification.
  - HD_FLAG pin: This flag goes high when a 2-pair HDBaseT PD-PSE mutually identifies each other via Classification.
  - 4P_AT_FLAG pin: This flag goes high when a 4-pair version of a (non-standard) Type 2 PD-PSE mutually identifies each other via classification. Or when 2-pair PSE is identified and both SUPP_Sx pins are high.
  - 4P_HD_FLAG pin: This flag goes high when a 4-pair (Twin) HDBaseT PD-PSE mutually identifies each other via Classification.
- **V_{AUX} Output Capacitor:** V_{AUX} is a low power regulated output available for use as a start-up supply for an external DC/DC converter controller. This supply is low duty, and intended to be used on a supply rail bootstrapped to a DC/DC converter output. V_{AUX} output requires ceramic capacitor of minimum 4.7µF, to be connected directly between V_{AUX} pin and VPN_{OUT} pin.

A single PD70210/A IC may be operated with 4 pairs for extended current of 720mA.

A single PD70210AL IC may be operated with 4 pairs for extended power capability up to 100W.

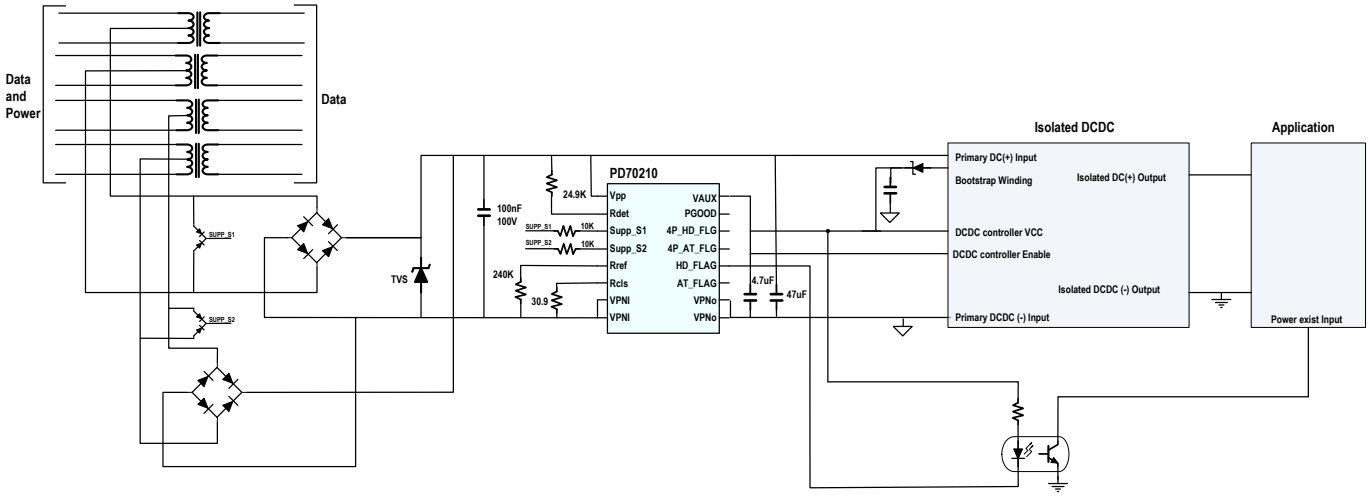

Figure 5: Typical 2 or 4 Pair Configuration with a Single PD70210 IC

Operation with an External DC Source

PD applications utilizing PD70210/A/AL IC may be operated with an external power source (DC wall adaptor). There are three methods of providing power with an external source:

1) External source connected directly to PD70210/A/AL Input (VPP to VPN_{IN}). Requires external source output voltage to be 42V minimum no load and more than 34.5V for max load. Adaptor must be isolated from VPP or VPN_{IN} through a diode. In this case either PD70210 or PD70210 A can be used.
2) External source connected directly to PD70210A/AL output connection to the application. External source output voltage will be dependent on application input requirements. External source must be isolated from VPP or VPN_{OUT} through a diode. In this case PD70210 cannot be used.
3) External source connected directly to application's low voltage supply rails (output side of an isolated or non-isolated power supply). External source must be isolated from application power supply's output either through a switched connection, a diode, or a separate regulator that sources current only (does not sink current). In this case either PD70210 or PD70210 A can be used.

PD70210/A/AL configured with an external wall adaptor is presented in Figure 6 to Figure 8

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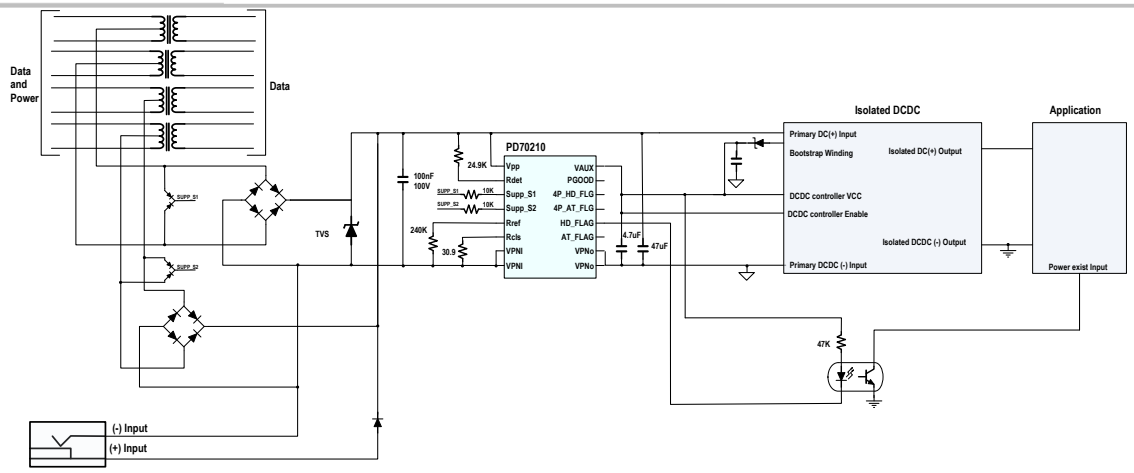

Figure 6: External Power Input connected to PD70210 Input

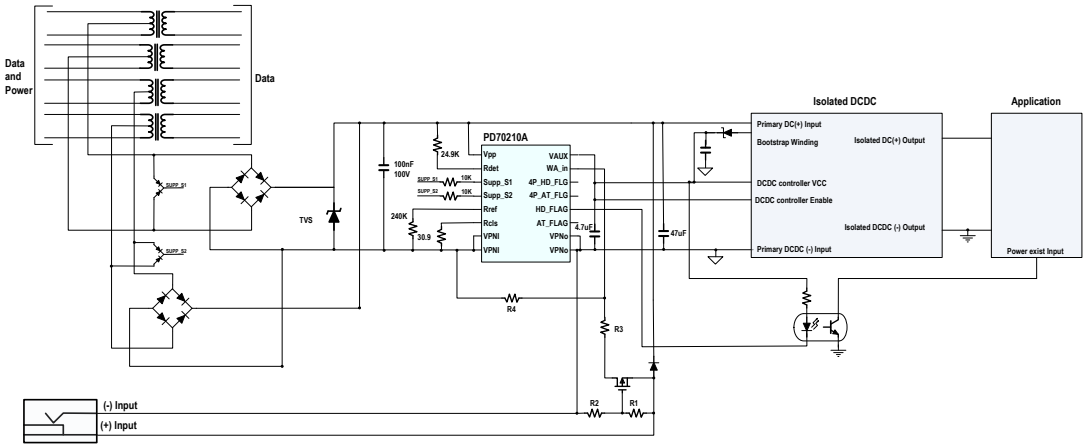

Figure 7: External Power Input connected to PD70210A Output

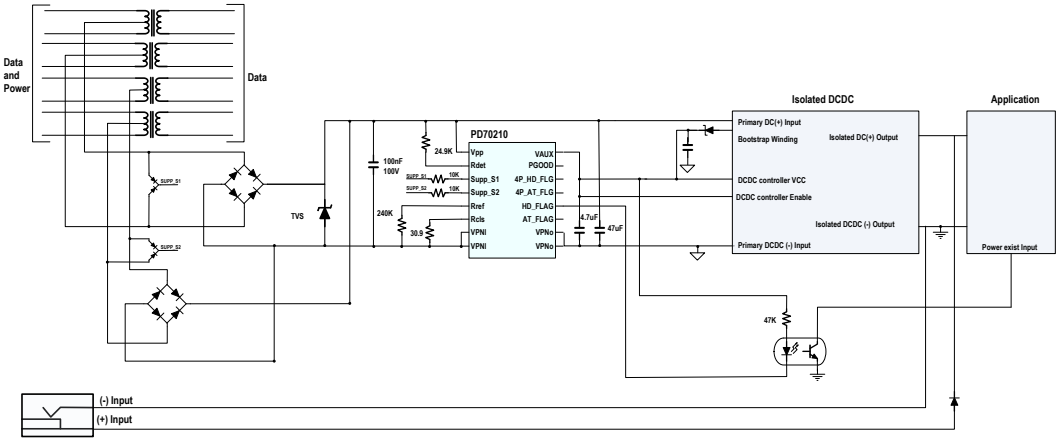

Figure 8: External Power Input connected to Application supply Rails – Switched Connection

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General Circuit Description

Event Thresholds

PD70210/A/AL IC switches between states based on voltage level differences between V_{PP} and VPN_{IN}.

Threshold levels between V_{PP} and VPN_{IN} are defined as follows:

- **V_{PP} - VPN_{IN} = 1.3V to 10.1V (Rising Voltage):** Detection resistor R_{DET} is connected between V_{PP} and VPN_{IN}.
- **V_{PP} - VPN_{IN} = 10.1V to 12.8V (Rising Voltage):** Detection Resistor R_{DET} is disconnected from VPN_{IN}.
- **V_{PP} - VPN_{IN} = 11.4V to 13.7V (Rising Voltage):** Classification current source is connected between V_{PP} and VPN_{IN}. This threshold establishes the programmed current draw set by R_{CLASS}. Current magnitude sets class level per IEEE 802.3at and HDBASET standards. This function is optional for IEEE 802.3af compliant PDs and mandatory for IEEE 802.3at and HDBASET compliant PDs. There is a hysteresis between Enable and Disable thresholds of classification current source. Classification current source remains connected during VPP rising voltage up to 20.9V.
- **V_{PP} - VPN_{IN} = 20.9V to 23.9V (Rising Voltage):** Classification current source is disconnected.
- **V_{PP} - VPN_{IN} = 4.9V to 10.1V (Falling Voltage):** This is the Mark voltage range. IC will recognize V_{PP} - VPN_{IN} voltage falling from Classification current source connect threshold to Mark threshold as one event of the 2 Events Classification Signature. The number of Class to Mark level events will cause IC to set the relevant flags to their active low state.

- **V_{PP} - VPN_{IN} = 36V to 42V (Rising Voltage):** Isolation switch is switched from Off to Low Current Soft Start mode. In Soft Start mode the isolation switch limits the DC current to 240mA (typical). The current limit circuitry during Soft Start mode monitors the voltage difference across the isolation switch (VPN_{OUT} - VPN_{IN}) and maintains Soft Start current.
  When VPN_{OUT} - VPN_{IN} drops to 0.7V or below, isolation switch Soft Start current limit is disabled, V_{AUX} is enabled, the isolation switch is fully turned on with 2.2A (max) over current protection and relevant flags are asserted after $\mathbf{t_{FLAG}}$ delay, which is minimum 80 ms.

- **V_{PP} - VPN_{IN} = 30.5V to 34.5V (Falling Voltage):** Isolation switch is switched off at this threshold, establishing high impedance between VPN_{IN} and VPN_{OUT}. Bulk capacitor discharge function is enabled, and stays enabled as long as difference between voltages V_{PP} and VPN_{OUT} remains between 30V and 7V.

- **V_{PP} - VPN_{IN} = 2.8V to 4.85V (Falling Voltage):** Detection resistor R_{DET} is reconnected at this threshold.R_{DET} is disconnected when V_{PP} - VPN_{IN} voltage drops below 1.1V.

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Soft Start Current Limit

PD70210/A/AL IC provide Soft Start current limiting. A rising voltage of 36V to 42V between V_{PP} and VPN_{IN} will enable isolation switch in Soft Start Current Limit mode. During this time, the current through isolation switch is limited to 240mA (typical). PD70210/A/AL IC continuously monitors the voltage drop across isolation switch (VPN_{OUT} to VPN_{IN}) during Soft Start mode. When difference between voltages VPN_{OUT} and VPN_{IN} drops below 0.7V, PD70210/A/AL IC will switch to normal operating mode, in which isolation switch is fully on, with over-current protection circuitry active.

Soft Start current limit is necessary for limiting the inrush current created by initial charge-up of input capacitors upon system start-up. Large inrush currents can create large voltage sags at PI, which in turn can cause system functions tied to event thresholds (such as AT_FLAG) to reset to their initial states. Soft Start current limit will significantly reduce voltage sag upon start-up.

Start-up into a fully discharged bulk capacitor will result in large power dissipation in the isolation switch for a period of time dependent on the size of the bulk capacitance. This occurs due to the initial voltage drop across the isolation switch. Maximum initial voltage drop across isolation switch can be of 42V. Maximum power dissipated by the isolation switch will decrease as the bulk capacitor charges, eventually decreasing to a maximum normal operating power dissipation of 1.9A*1.9A*0.3 ohm =1.08W. The period of time required to switch from Soft Start mode to normal operation mode can be calculated using the following formula:

$$T = \frac{(\Delta V - 0.7) \times C}{I}$$

Whereas:

I = PD70210/A/AL IC's current during soft start

C = Total input bulk capacitance

ΔV = Initial VPN_{OUT} - VPN_{IN} voltage at start of soft start (ΔVmax = V_{PP})

Bulk Capacitor Discharge

PD70210/A/AL IC provide discharge of the application bulk capacitor when V_{PP} - VPN_{IN} falling voltage drops below the isolation switch turn-off. This feature insures that the application bulk capacitance does not discharge through the detection resistor, which can cause detection signature to fail and prevent PSE from starting the PD. While enabled, discharge function provides a minimum controlled discharge current of 22.8mA, which flows through VPP pin, internally through isolation MOSFET's body diode, and out through VPN_{OUT} pin. Discharge circuitry monitors voltage difference between V_{PP} - VPN_{OUT}, and remains active while difference voltage is 7V ≤ (V_{PP} - VPN_{OUT}) ≤ 30V. Maximum time to discharge can be calculated by:

$$T = \frac{(\Delta V - 7V) \times C}{0.0228}$$

Whereas:

C = Total Input Bulk Capacitance

ΔV = Initial V_{PP} - VPN_{OUT} Voltage at Isolation Switch Turn-off

Example: Assuming an initial capacitor voltage of 32V, it will take 240ms for a 220µF capacitor to discharge to a 7V level.

The discharge operation has a timer and it is active for at least 430mSec.

Auxiliary Voltage – V_{AUX}

PD70210/A/AL IC have an available regulated voltage output, V_{AUX}, to be used primarily as a start-up supply for an external DC/DC controller. V_{AUX} is a low current, low duty cycle output, providing current momentarily until an external bootstrap supply can take over.

V_{AUX} output is regulated at nominal 10.5V, and will supply a peak current of 10mA for 10ms. Continuous current is 4mA. Typically V_{AUX} output is connected to a bootstrapped supply of higher voltage (such as a rectified auxiliary output from an isolated DC/DC converter transformer). V_{AUX} output does not sink current. Once bootstrapped voltage exceeds V_{AUX} output voltage level, V_{AUX} output will no longer provide current and will be transparent to the operation of the DC/DC converter. It is recommended to design the rectified bootstrapped output under all operating conditions for a minimum output voltage of 12.5V.

During Soft Start mode or at isolation switch turn-off, V_{AUX} output is disabled due to falling V_{PP}. V_{AUX} regulated output is enabled only when isolation switch is in normal operation mode. This insures DC/DC controller does not start prematurely.

P_{GOOD} Output

PD70210 IC provides an open drain output indicating power good status. This output is in a high impedance state until 80mSec after isolation switch moves from Soft Start current limit mode to normal operation mode. Upon assertion, P_{GOOD} output switches to ground with a current sink capability of 5mA. When V_{PP} - VPN_{IN} voltage falls below the isolation switch turn-off threshold, P_{GOOD} output sets back to high impedance state.

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This output may be used as an enable/disable control for a DC/DC converter to detect when PI voltage has fallen below operating threshold. Alternatively, it can be used to guarantee Soft Start function is finished before DC/DC is allowed to start.

PD70210A and PD70210AL ICs do not contain PGOOD output. If such functionality is required, VAUX can be used as an option. Tie VAUX to Nch FET gate, have FET's source connected to VPNout and FET Drain can be used as PGOOD replacement.

WA_EN inputs

This input pin is used for external power input connection between VPP and VPNout.

Please refer to Figure 7.

A resistor divider R1 and R2 is connected between VPP and VPNout. The resistors set the Pch turn on threshold.

A 100V low signal Pch FET gate and source should be connected to R1.

The Pch Drain is connected to WA_EN input through R3 resistor. R4 resistor is connected between WA_EN and VPNIN.

R3 and R4 set the level in which a valid WA input is detected.

WA_EN is a standard logic level input.

When WA_EN input is "high", PD70210A isolation switch is turned Off and all the flags are asserted-changed to "low" level.

The resistor selection guide is specified in the device data sheet.

SUPP_S1 and SUPP_S2 inputs

SUPP_S1 and SUPP_S2 inputs enable the PD to recognize the source of the power whether it is Data or Spare pairs or both. Each of these inputs requires a common Cathode dual diode to be connected to the relevant pair, if the PD device samples a High level of 35V and above in this input it counts this pair as an active pair.

These inputs are used when working with special PSE which having detection and classification on two pair only but having the power in all 4 Pairs.

SUPP_S1 and SUPP_S2 inputs should have 10K ohm resistor connected in serial to each of them.

When these inputs are not needed, it can be connected to VPNin input.

PSE type Flag Outputs

PD70210/A/AL IC provides open drain outputs indicating the PSE type by its detected Classification pattern. The output is in a high impedance state until the isolation switch moves from Soft Start Current Limit mode to normal operation mode.

It will then be asserted low, depends on the Classification pattern that was recognized. Upon assertion, Flags output switches to ground with a current sink capability of 5mA. Flags output signals switch back to high impedance state when V_{PP} - VPN_{IN} voltage falls below isolation switch turn-off threshold.

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The flags enable the PD designer to work with the flag that is relevant to the application. For each power that is detected all of the lower power flags are also asserted (IE AT_FLAG is asserted AT level and for all power levels above AT).

The available power level is specified in Table 1. As specified in the table the PD counts the Classification fingers event and by its count recognize the PSE type.

SUPP_S1 and SUPP_S2 enable the PD to recognize a special AT level PSE which having the classification on two pair only but having the power in all 4 Pairs. Thus if 2 fingers are recognized, then the PD device samples SUPP_S1 and SUPP_S2 inputs and if both are “High” then the power is supplied to the 4 pair and 4P_AT flag is asserted.

Thermal Protection

PD70210/A/AL IC provide thermal protection. Integrated thermal sensors monitor the internal temperatures of the isolation switch and classification current source. If the over-temperature threshold of either sensor is exceeded, that sensor’s respective circuit will disable.

To insure trouble free operation, it is important to make sure PD70210/A/AL IC’s exposed pad is mounted to a copper area on the PCB that provides an adequate heat sink.

PCB Layout Guidelines

IEEE 802.3at and HDBASET standards specify certain isolation requirements which must be met by all POE equipment. Isolation is specified at 1500Vrms minimum between incoming Data and Power lines, and any signal, power or chassis connection that can come into contact by the end user outside the application. On a typical FR4 PCB, this requirement is generally satisfied by creating an isolation barrier of a minimum 0.080 inch (2mm) between adjacent traces requiring 1500Vrms isolation.

Any adjacent traces containing POE voltage potentials should be considered for proper creepage and clearance per IEC 60950.

Give PD70210/A/AL PCB design special attention to provide adequate heat sinking of the exposed pad (VPNOUT). PD70210/A IC’s 16 pin DFN package and PD70210AL 38 pin QFN package utilizes the exposed pad to provide thermal cooling of the package, and as such requires PCB design to include sufficient copper area attached to the exposed pad. For multilayer boards, conductive vias to an adjacent plane layer may be used. Keep in mind that exposed pad is electrically connected to VPNIN and must be electrically isolated from VPNOUT.

When using vias to provide thermal conductivity between a plane layer and exposed pad, barrels should be 12mils in diameter and (where possible) placed in a grid pattern. Barrel holes should be plugged or tented for proper solder paste release. When tented holes are used, solder mask inclusion area should be 4mils (0.1mm) larger than via barrel.

A recommended footprint for PD70210/A/AL and via placement example is contained in device data sheet.

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For single or dual layer boards you should use large copper fills in direct contact with the exposed pad. Copper thickness of 2Oz will improve thermal performance. If using copper traces of less than 2Oz, it is recommended to increase overall trace thickness by adding excess solder to trace areas where appropriate.

PCB design should provide wide, heavy copper traces for high current power lines. A 4 pair, extended power PD can have maximum trace currents of 1.9A for the VPP and VSS input terminals. Traces carrying current for VPP, VPNIN, and VPNOUT should be sized to provide the lowest temperature rise practical at the maximum current. For example, a minimum of 15 mils wide 2Oz copper will accommodate up to 1.6A current with a maximum 10°C temperature rise. If using copper traces of less than 2Oz, increase the minimum width to accommodate maximum current with lowest temperature rise.

POE signals contain voltages up to 57Vdc. Component working voltage must be considered, and components sized accordingly. Surface mount resistors are a good example: 0402 and 0603 resistors have typical maximum working voltage specifications of 50V, whereas 0805 resistors are typically specified at 150V.

When used with PD70210/A/AL IC, detection resistor RDET is only connected at POE voltages up to 12.8V, and is disconnected otherwise. 24.9K RDET resistor may be a low voltage type when used with PD70210/A/AL IC's RDET pin.

Number of Class Fingers	SUPP_S1	SUPP_S2	PGOOD_ FLAG	AT_ FLAG	HD_ FLAG	4P_AT_ FLAG	4P_HD_ FLAG	Available power Level
1	X	X	0V	Hi Z	Hi Z	Hi Z	Hi Z	802.3 AF level/ 802.3 AT Type 1 level
2	H	L	0V	0V	Hi Z	Hi Z	Hi Z	802.3 AT Type 2 level
2	L	H	0V	0V	Hi Z	Hi Z	Hi Z	802.3 AT Type 2 level
2	H	H	0V	0V	Hi Z	0V	Hi Z	Dual 802.3 AT Type 2 level
3	L	H	0V	0V	0V	Hi Z	Hi Z	HDBT Type 3 level
3	H	L	0V	0V	0V	Hi Z		HDBT Type 3 level
3	H	H	0V	0V	0V	0V	Hi Z	HDBT Type 3 level
4	X	X	0V	0V	0V	0V	Hi Z	Dual 802.3 AT Type 2 level
5	X	X	RESERVED FOR FUTURE					NA
6	X	X	0V	0V	0V	0V	0V	Twin HDBT Type 3 level

Table 4: Available PD power level and Flag indication

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Application examples

Reference designs for 2/4 pair application can be found on the following pages. A design example is shown in Figure 9 and Figure 10.

Figure 9

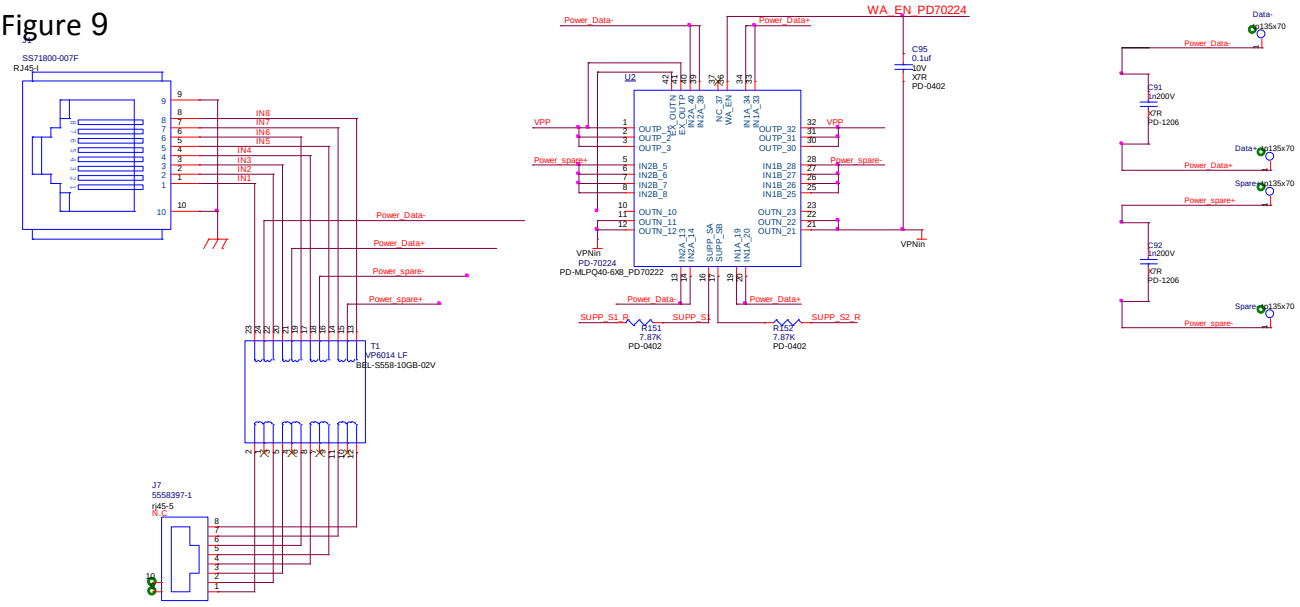

Figure 9: Type 3 HDBASET front end- connector and diode bridge(1 of 2)

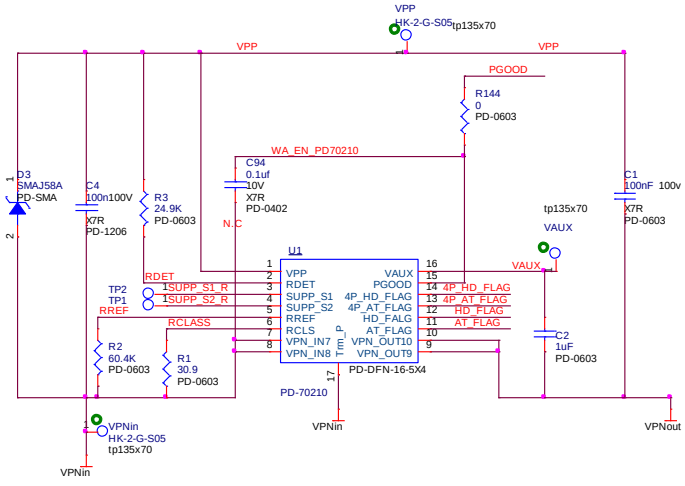

Figure 10: HDBASET Type 3 front end- PD device (2 of 2)

Revision History

Revision Level / Date	Para. Affected	Description
0.1/ 27 June 2013		Initial release
0.2/ 22 June 2014		
1.0/ 07 Oct 2014	Page 12	flags description update

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Visit our web site at: www.microsemi.com **Catalog Number**: PD70210_PD70210A_AN209