ZLE30150_88X2242M/P Reference Design Board

This document provides a brief overview of the ZLE30150_88X2242M/P Reference Design Board (RDB).

The RDB was developed to demonstrate the use of a ZL3015x device to implement the timing in a Synchronous Ethernet application, developed around a Quad-port Multi-speed Ethernet Transceiver from Marvel; part number 88X2242M or 88X2242P.

Two flavors of the ZL3015x family of circuits can be populated on the RDB: ZL30154 or ZL30150.

ZL30154 is a Synchronous Ethernet Network Synchronizer that provides all the functionality that is required for a central timing card in carrier grade network equipment. It is targeting timing card and pizza-box type of applications.

ZL30150 is a dual Channel Clock Translator with two programmable Numerically Controlled Oscillators (NCOs), and provides all the features required to implement the timing on a 10GBASE-R or 10GBASE-W line card.

The RDB allows a customer to test and evaluate different aspects of SyncE synchronization and to perform G.8262 SyncE Conformance testing. It can also serve as a reference for customer's hardware development helping to shorten the development and the time to market of a new product.

The ZLE30150_882242M/P RDB provides the following features:

- One ZL3015x timing device.
- One 88X2242M/P Quad-port Multi-Speed Ethernet Transceiver.
- Four SFP+ connectors providing access to the four line side ports of 88X2242M/P.
- LOS and LINK/ACT status LED's for each line side port.
- 16 SMP connectors providing access to the four system side ports of 88X2242M/P (2 x TX SMP and 2 x RX SMP per port).
- LINK/ACT status LED's for each system side port..
- Master clock reference for ZL3015x. Four footprints are available to accommodate the most common XO, TCXO and OCXO recommended for ZL3015x.
- One USB interface to allow RDB configuration and control using the GUI.
- One uC used to implement the configuration and control of the board.
- Two differential output clocks provided through SMA connectors. These clocks are replica of the 156.25MHz and 155.52MHz reference clocks provided by ZL3015x to 88X2242M/P.
- Two differential external reference input clocks for ZL3015x through SMA connectors.
- Power supply circuits that are generating all the RDB voltages from an external supply voltage.
- SPI debug interface. Can be used to access ZL3015x using the Microsemi ClockCenter GUI software and USB configuration module.
- MDIO debug interface. Can be used to access 88X2242M/P using the Marvell GUI and USB dongle.
- Configuration header for 88X2242M/P power up configuration.
- RDB reset button.
- DIP switch used to select the default configuration of the RDB at power-up/reset: 10GBASE-R or 10GBASE-W.
- Four status LED's indicating the LOCK and HOLDOVER status of ZL3015x DPLL0 and 1.

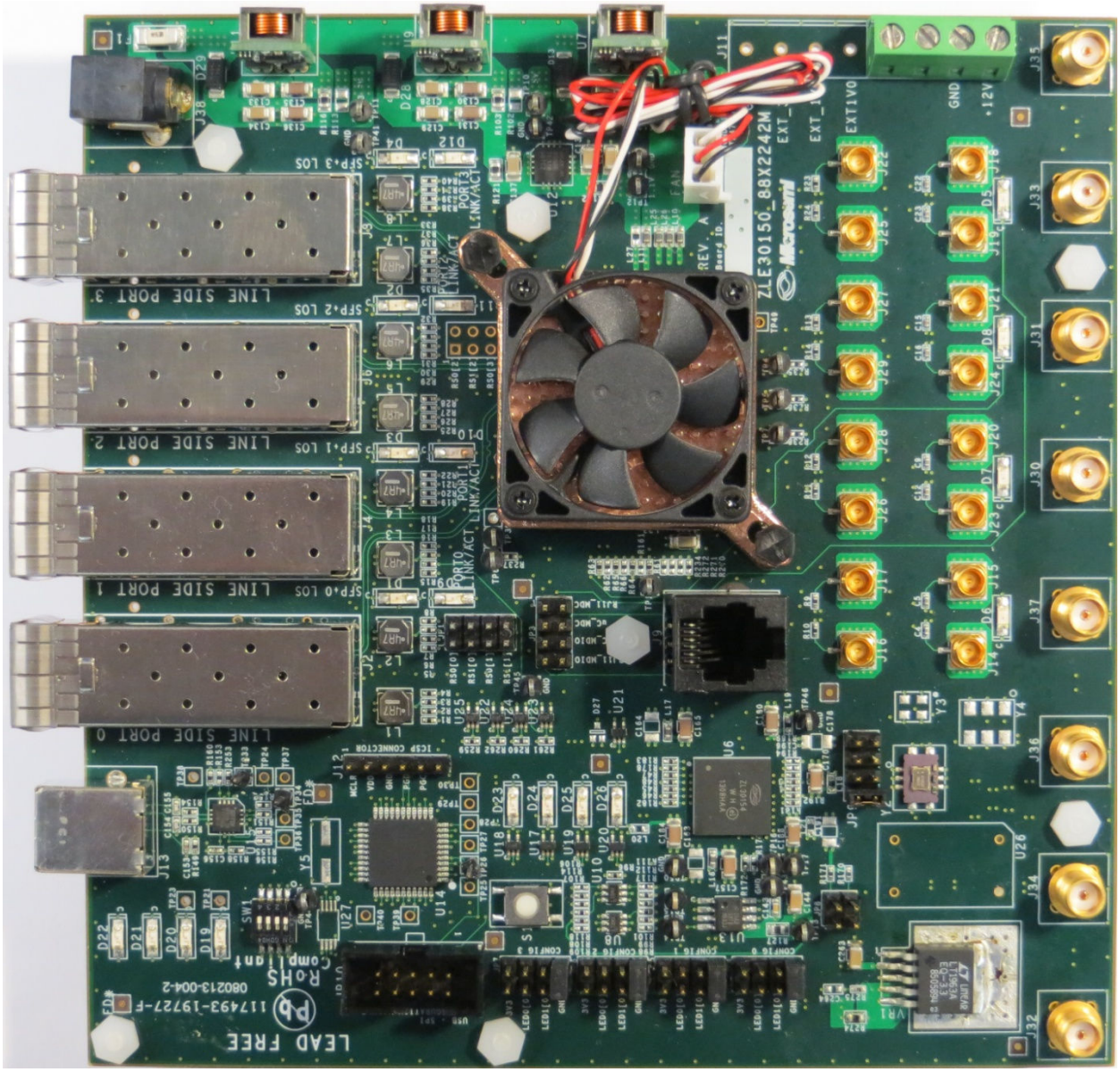

Figure 1 · Top view of ZLE30150_88X2242M/P Reference Design Board

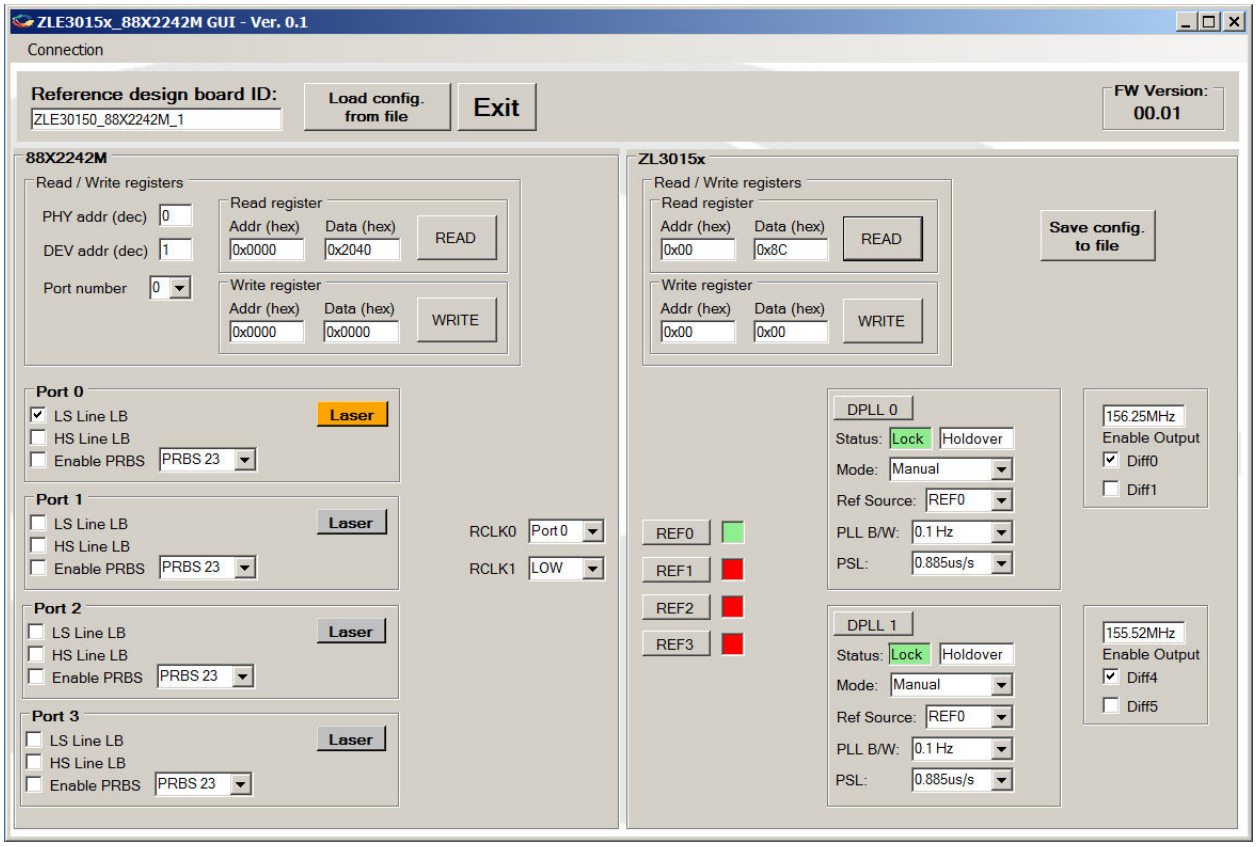

Figure 2 · ZLE30150_88X2242M/P GUI main window

Microsemi is the market leader in network synchronization and offers an industry-leading portfolio focused on timing solutions for packet networks (SyncE and IEEE1588) and optical transport network (OTN) systems. The company offers a complete portfolio of timing products for high-performance network synchronization including digital phase locked loop (DPLL) solutions to drive network clocks, as well as analog and mixed-signal timing ICs to meet performance requirements for up to 10G/40G interfaces. Microsemi's clock management solutions include clock generators and synthesizers, clock fanout buffers, and rate conversion jitter attenuators that allow product developers to simplify system and board design.

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