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ZL30151, ZL30169, and ZL3025x Series GUI and Evaluation Board Step-by-Step User Guide

Revision 1.2 September 16, 2014

Contents

Introduction

- The ZL30151/ZL30169/ZL3025x GUI and evaluation board provide an easy-to-use, flexible platform for evaluating device features and performance

- **GUI**
  - A single Windows®-based GUI program supports all devices in the product family
  - Offline mode can be used to learn about device capabilities and create configuration files without the need for an evaluation board
  - Online mode can be used to control an evaluation board for live device evaluation

- **Evaluation Board**
  - Evaluation boards are available for the ZL30151, ZL30169, ZL30251, and ZL30253.
  - Highly configurable for easy evaluation of a wide range of applications
  - Easy access to all device input and output clocks, and many device features

Collateral Documentation

- ZL30250 Evaluation Software User Manual
  - Provided with GUI software
- ZLE30250 Evaluation Board Quick Start Guide
  - Provided with GUI software
- ZLE30250 Hardware Guide
  - Provided with GUI software
- ZLE30250 Evaluation Board bill-of-materials, schematic, and layout files
  - Contact factory

GUI Overview

GUI Overview

- Single GUI supports all device variants
- Runs on Windows 7 (recommended) and Windows XP
  - Windows XP support may be discontinued in the future
- Has two layers:
  - GUI – User facing. Only enough knowledge about the Jade architecture to rearrange its controls to suit the part number and mode chosen.
    - Makes Windows calls such as File Open, Save As, etc.
    - Handles all graphical aspects
    - Communicates with the evaluation board
  - HAL – Device facing. Encapsulates all detailed knowledge about the device.
    - Calculations to convert from user concepts such as bandwidth to low-level device concepts such as proportional and integral path parameters
    - Calculates internal solutions for input frequency and output frequency combinations
    - Calculates low-level setup details for input monitors
    - Handles any function that is complex and/or has multiple input variables
  - This approach provides a simple-to-use GUI interface which allows easy entry of high level application requirements. Most device configuration details and optimization are performed automatically by the HAL.

GUI Overview

- Can be used with, or without, an evaluation board
- Required for generating device configurations
- Operating model is to make one or more .MFG files and optionally an EEPROM image file for customer use
- Evaluation board uses the same FTDI USB interface IC as CC+ and the same FTDI driver. Same methods should be used for debug of driver issues.
- Simply connecting a PC with internet access to a powered evaluation board causes Windows to fetch and install the FTDI driver from Windows Update.

GUI Overview

- The GUI is available for download from the Microsemi website
  - A MyMicrosemi account is required
  - A MyCMPG account is also required
  - With these two accounts the GUI can be downloaded from the website using the Software Delivery System (SDS)

Starting the GUI

Starting the GUI
Device Selection Window

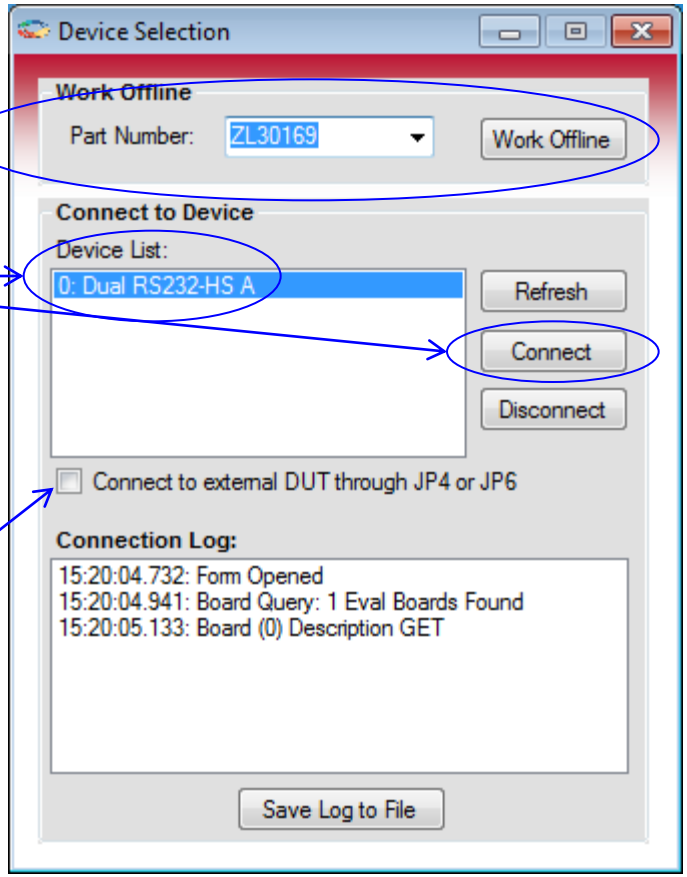
- When the GUI is started, the **Device Selection** window is displayed
  - Use this window to select Offline mode or to connect to an evaluation board
  - This window can also be accessed from the GUI main window to change the initial selection

To use the GUI in offline mode, select the desired device part number and press the **Work Offline** button

To use the GUI with an evaluation board, select the board from the list and press the **Connect** button

Note: When the GUI connects to the evaluation board, it automatically detects the installed device and configures itself to that device

Selecting this checkbox configures the evaluation board to allow the GUI to communicate with an off-board ZL30151/169/25x device whose SPI bus is attached to evaluation board connector JP4 or JP6. The on-board ZL30151/169/25x device is not accessible in this mode.



Starting the GUI
DUT Connection Window

- When connecting to a device, the **DUT Connection** window is displayed next
  - Use this window to specify how to synchronize the GUI and the device on the evaluation board

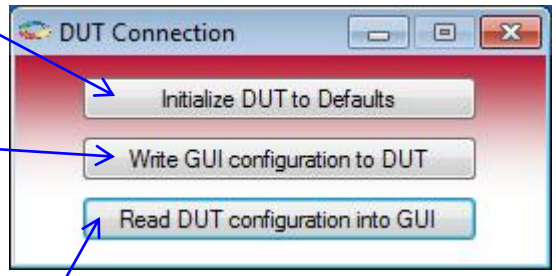
Select **Initialize DUT to Defaults** option to initialize both the GUI and evaluation board device to the default settings

Select **Write GUI configuration to DUT** option to write the current GUI configuration to the device on the evaluation board

- This option can be used to load the current GUI configuration into the evaluation board device when the GUI is configured in offline mode prior to connecting to the evaluation board device
- This option is only displayed when the GUI has been configured in offline mode prior to connecting to a device

Select **Read DUT configuration into GUI** option to synchronize the GUI to the current evaluation board device configuration

- This option is only displayed when the GUI detects that the evaluation board device is not configured to its power-on default settings



Starting the GUI
Initial Configuration Window

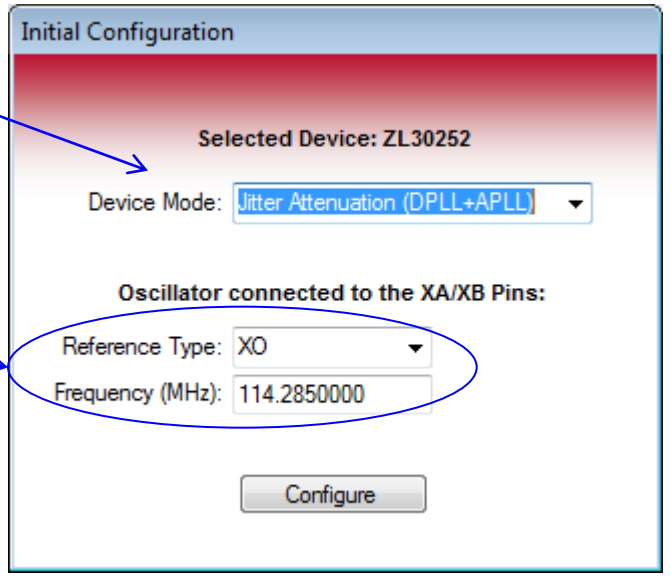
- After the device and operating mode have been selected, the **Initial Configuration** window is displayed
  - Use this window to select the initial device mode, reference type, and reference frequency
  - These settings can be changed on the GUI main window

Select the desired device operating mode

Note: Only valid modes for the selected device will be displayed

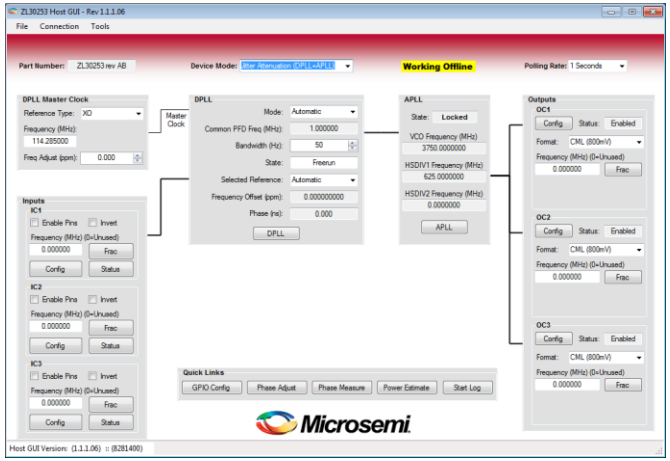
Select the appropriate reference type connected to the device XA/XB pins and specify its frequency

Note: When connecting to an evaluation board, these setting must match the board configuration for proper operation

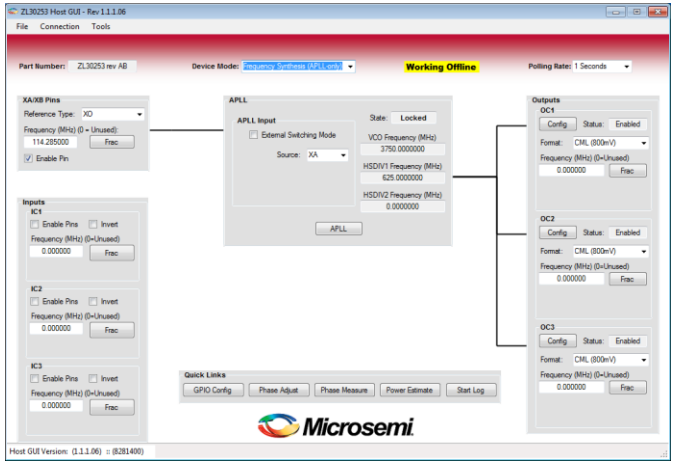


Starting the GUI
GUI Main Window

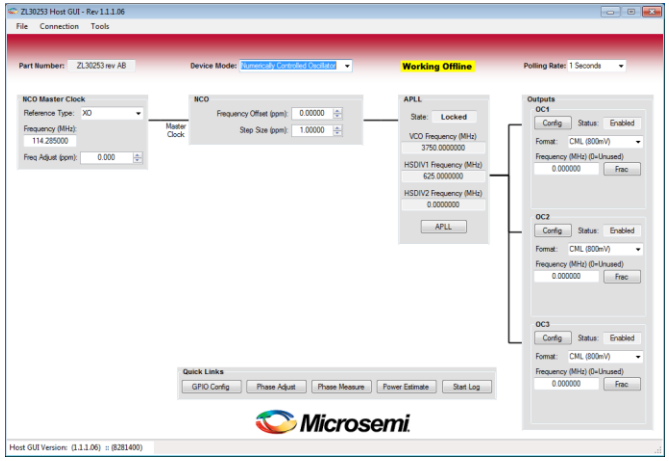
- The GUI main window is a block diagram representation of the selected device mode



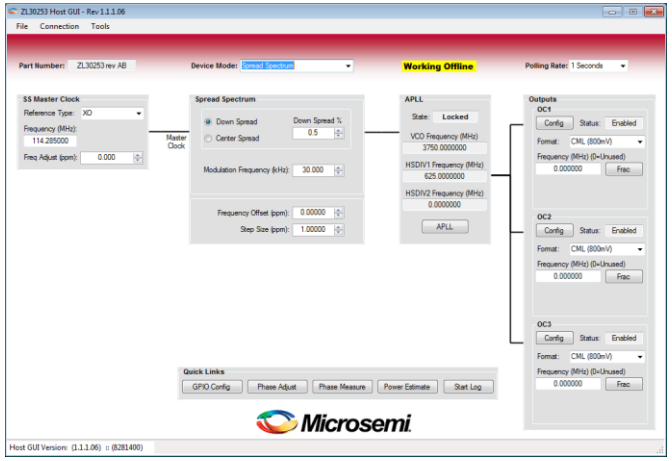
Jitter Attenuation (DPLL+APLL) Mode



Frequency Synthesis (APLL-Only) Mode



Numerically Controlled Oscillator Mode

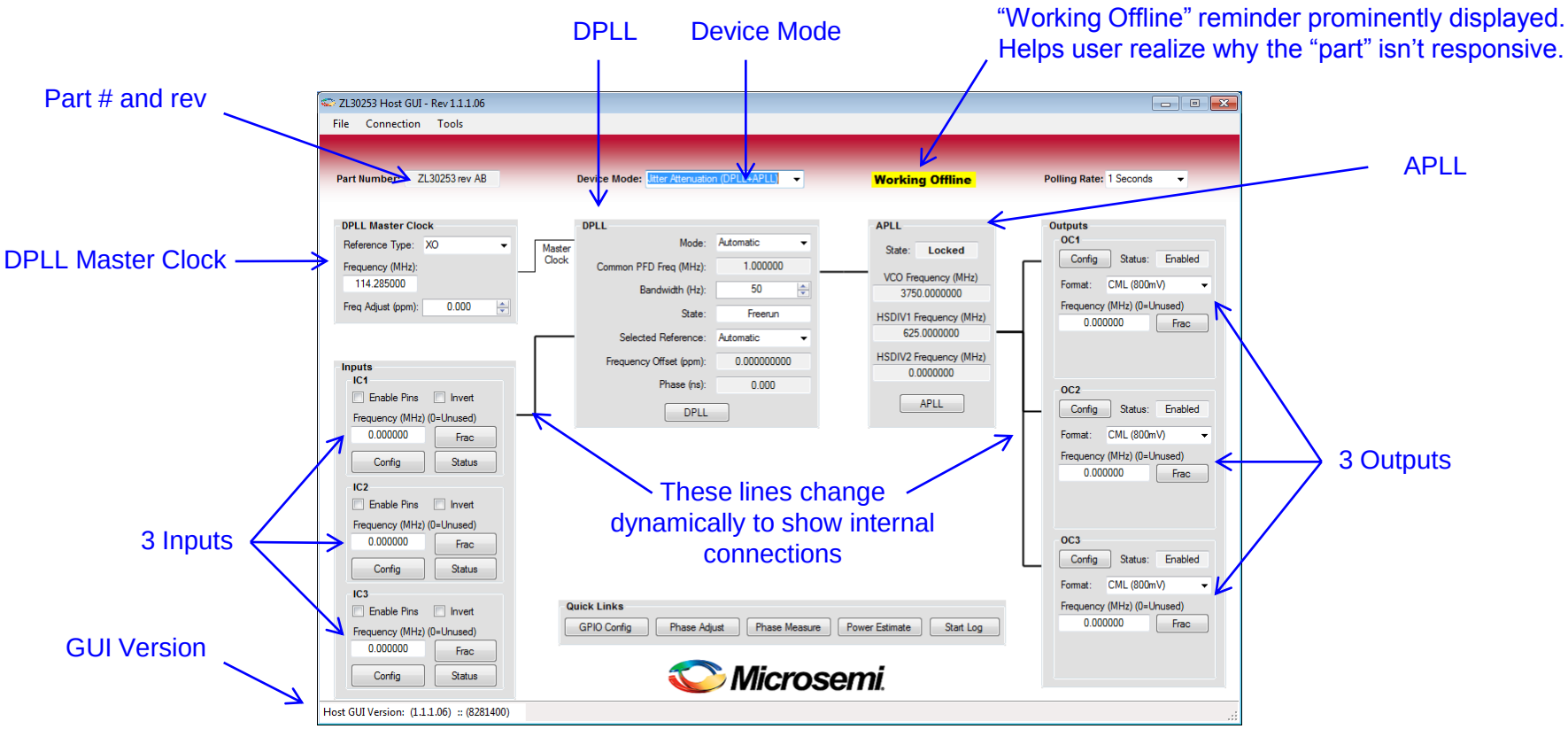


Spread Spectrum Mode

GUI Functionality Common to All Device Modes

Common GUI Functionality
Main Window Overview

- The GUI main window provides an intuitive, high-level view of the device configuration
  - Most commonly used device features are located on the main window
  - Signal flow arrows provide a graphical representation of internal connectivity

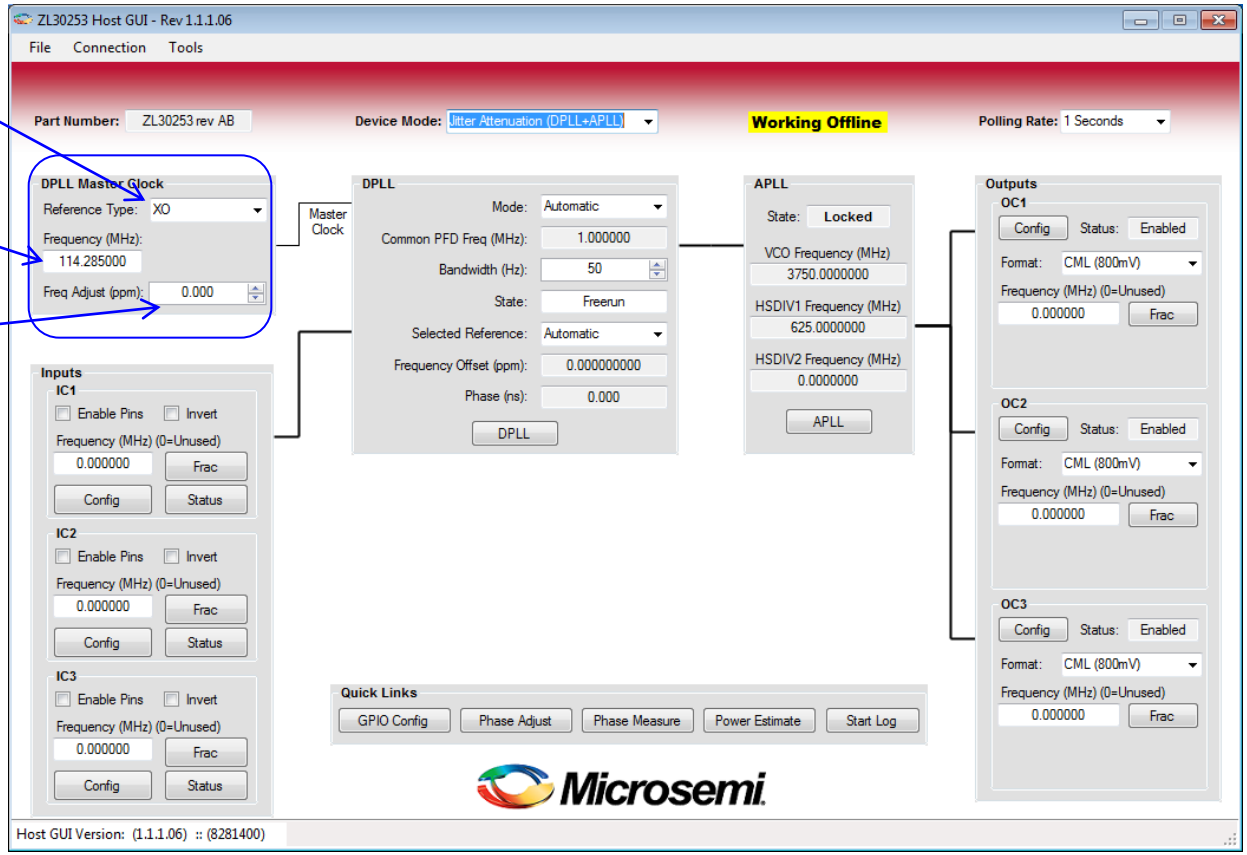


Common GUI Functionality
Main Window – Master Clock Configuration

Master Clock Type

Nominal Master Clock Frequency

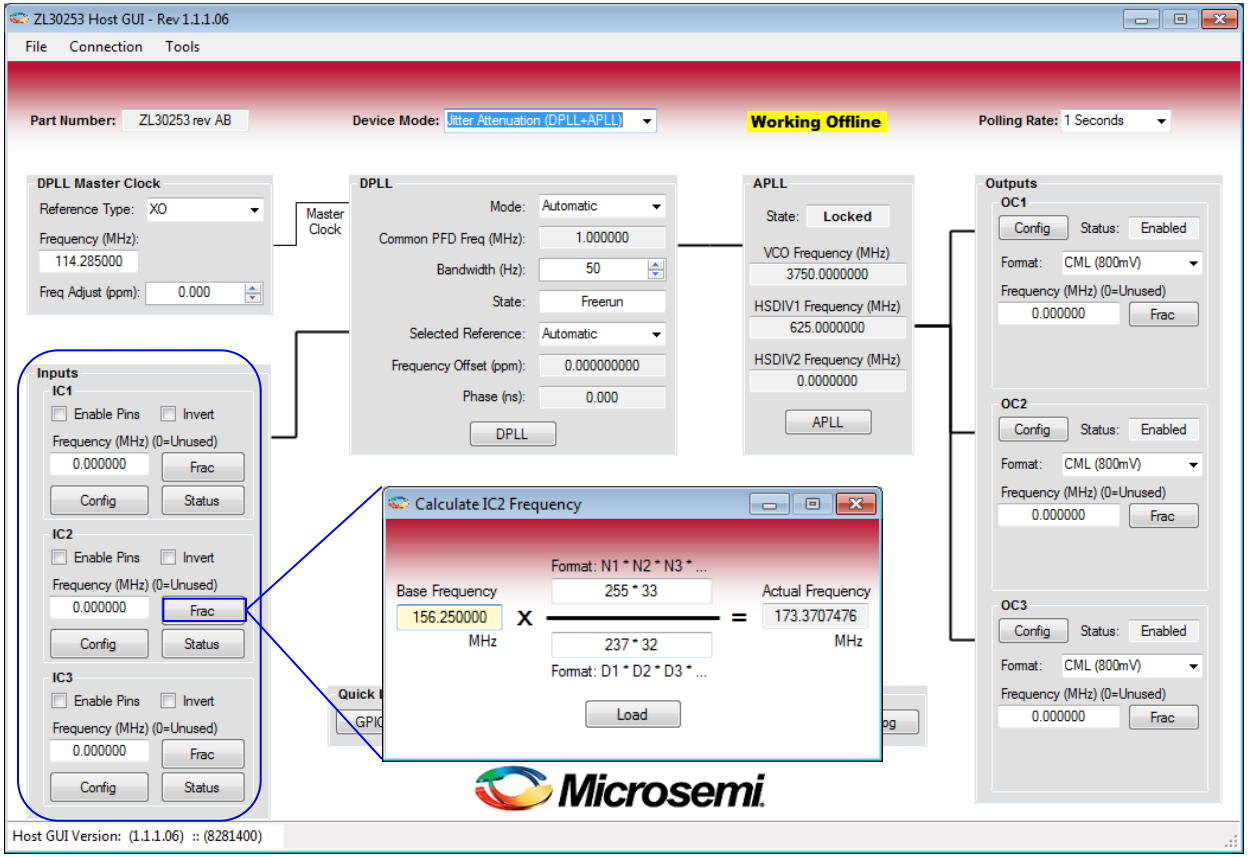
Master Clock Frequency Offset Adjustment



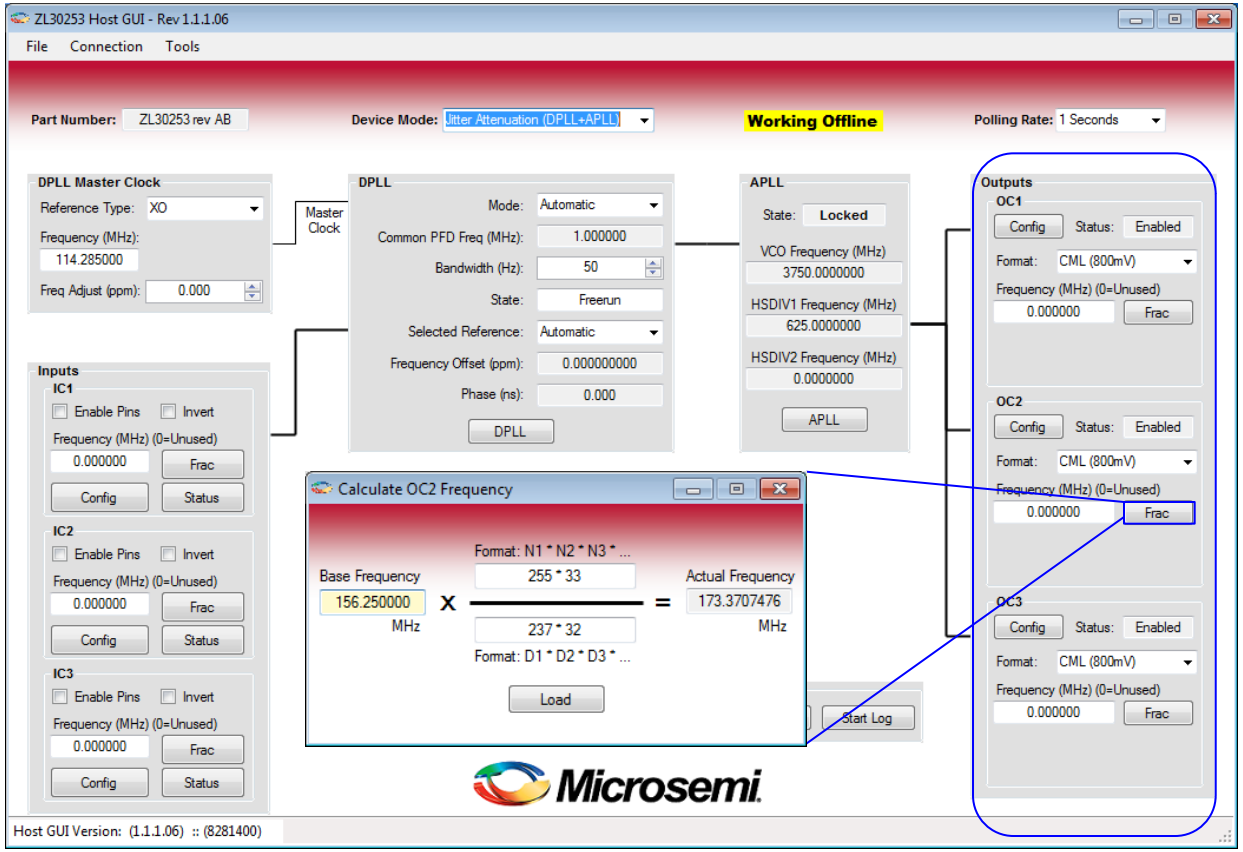
- The initial DPLL master clock configuration is specified on the **Initial Configuration** window when the GUI is started
- The DPLL Master Clock section of the main window can be used to change these settings
- The **Freq Adjust** field can be used to apply a ppm bias to the reference oscillator or crystal nominal frequency

Common GUI Functionality
Main Window – Input Clock Configuration

- Each input clock is independently configured
- The **Enable Pins** check box enables or disables an input clock
- Input clock frequency is configured independent of enable/disable state to allow support of initially disabled inputs
- The input clock **Frac** button can be used to precisely specify complex frequencies such as FEC rates
- The specified set of input frequencies must be integer divisible to a common frequency between 1kHz and 500kHz
- A frequency of 0 excludes an input from the frequency plan solver
- The GUI input clock frequency plan solver converts the specified set of frequencies into an optimized device configuration
- The GUI will display a pop-up error message if an invalid combination of frequencies is specified

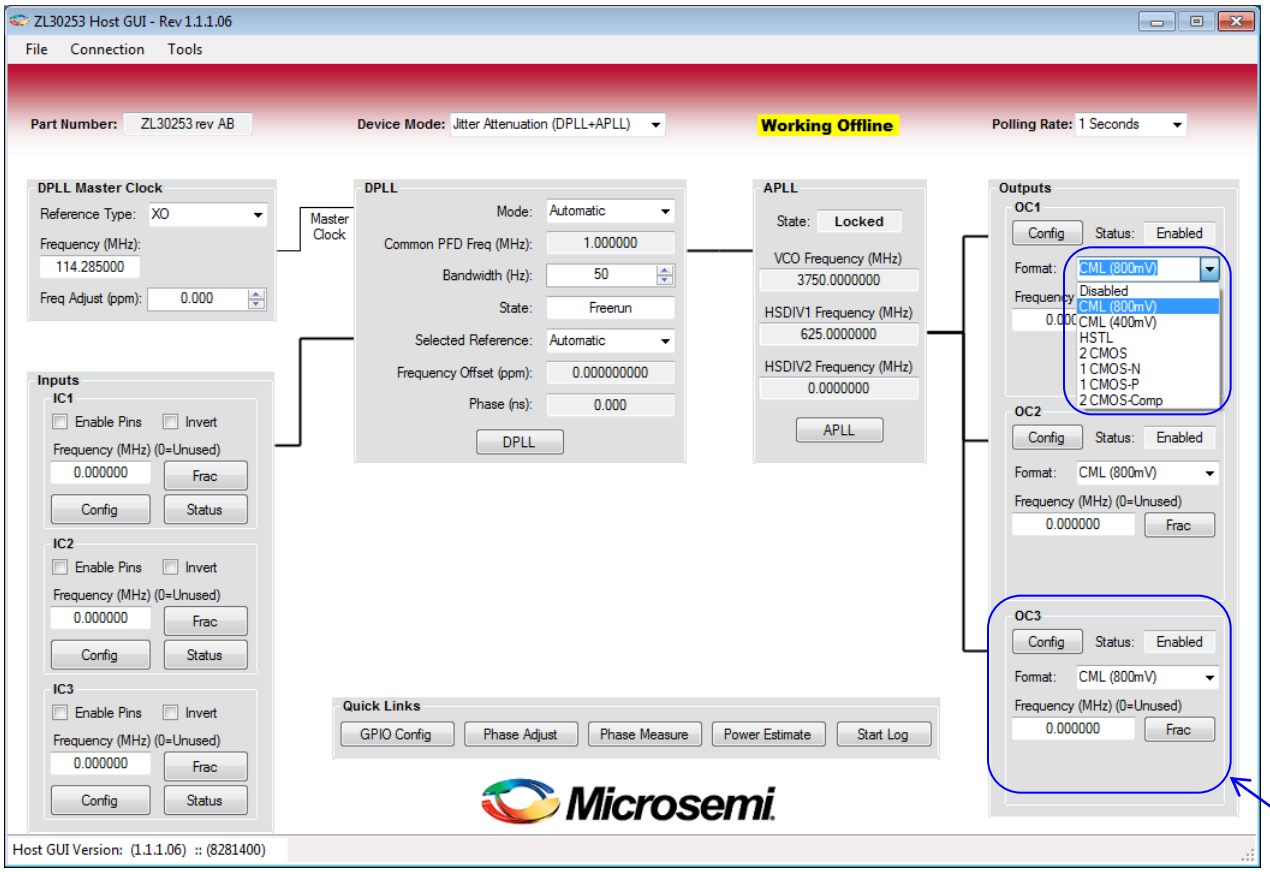


Common GUI Functionality
Main Window – Output Clock Configuration



- Each output clock is independently configured
- Output clock frequency is configured independent of enable/disable state to allow support of initially disabled outputs
- The output clock **Frac** button can be used to precisely specify complex frequencies such as FEC rates
- The specified set of frequencies must be integer / half-divide derivable from a common APLL VCO frequency
- An frequency of 0 excludes an input from the frequency plan solver
- The GUI output clock frequency plan solver converts the specified set of frequencies into an optimized device configuration
- The GUI will display a pop-up error message if an invalid combination of frequencies is specified

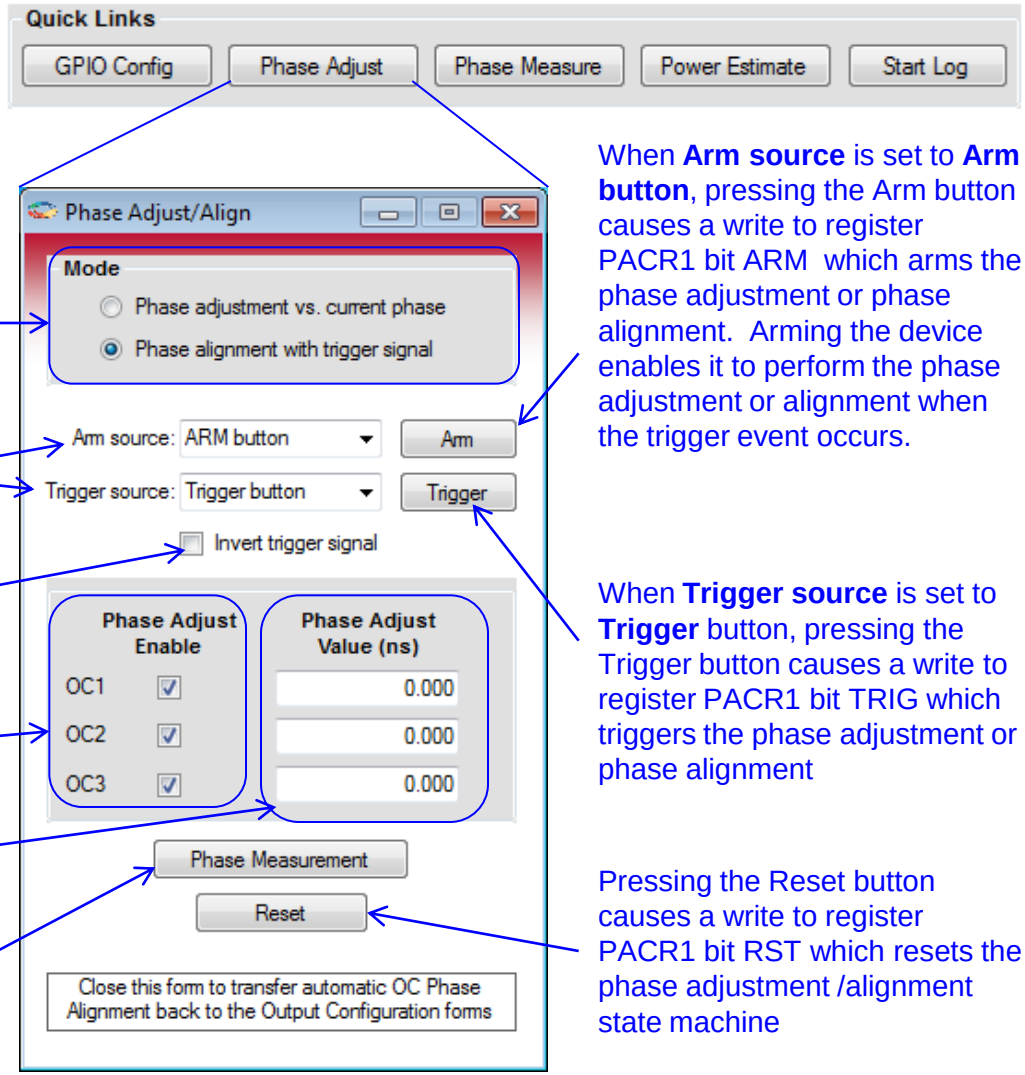
Common GUI Functionality
Main Window – Output Clock Configuration



- Output Clocks signal format is specified using the **Format** drop-down list
- Selecting **Disabled** places the output in a high impedance state
- Two CML options
  - CML (800mV) provides standard CML signal swing
  - CML (400mV) provides a lower power half amplitude signal swing
  - Both modes require a 3.3V pad supply (pin VDDOn)
- HSTL Option
  - Can also be used to implement an HCSL compatible signal format with a 1.5V or 1.8V pad supply (VDDOn)
- Multiple CMOS options
  - Single CMOS output on POS or NEG
  - Two phase aligned, or complementary CMOS outputs on POS and NEG
  - When both CMOS outputs are used, NEG can be configured to be POS / LSDIV divider. Not all division options are supported.

Common GUI Functionality
Phase Adjust/Align Window

- Accessed from Main window Quick Links **Phase Adjust** button
- Provides high level implementation of device output clock phase alignment and phase adjustment functionality



Select Phase alignment mode to align all outputs
Select phase adjustment mode to perform a phase adjustment on an output relative to its current phase

Select Arm and Trigger events for phase alignment or adjustment

Arm and Trigger events cannot be concurrent. If same signal used for Arm and Trigger, select invert trigger signal to place Arm and Trigger events on opposite signal edge transitions.

Select which output clocks will participate in the phase adjustment or alignment

Specify output phase adjustment or alignment to be applied for each participating output clock

Pressing the Phase Measurement Button opens Phase Measurement Window

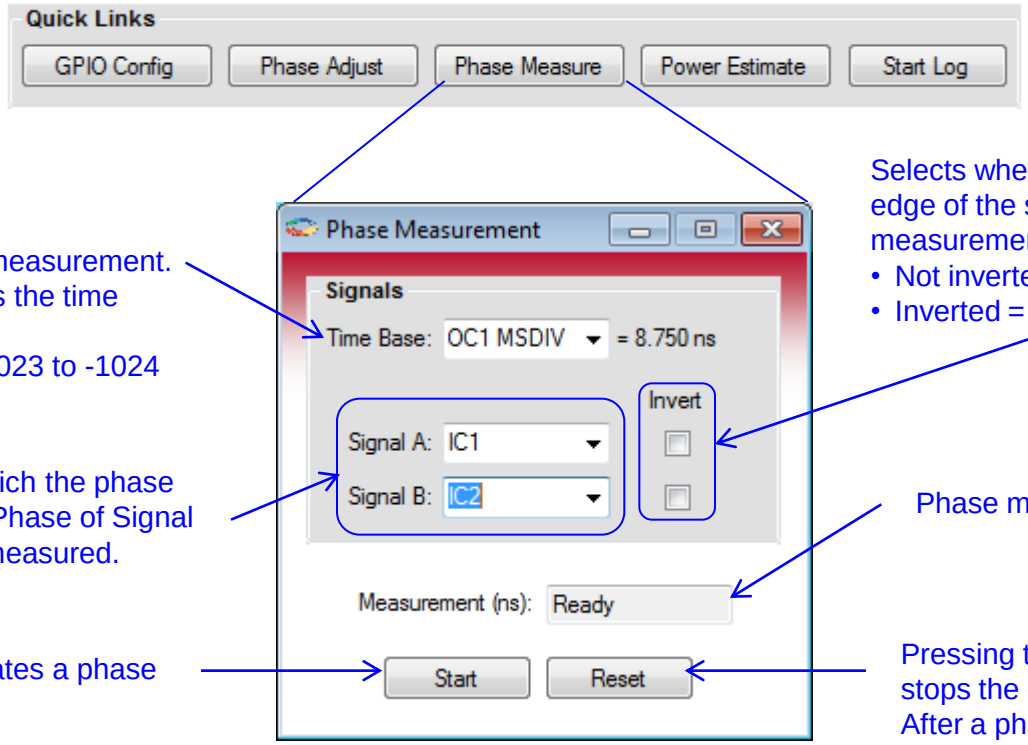
When **Arm source** is set to **Arm button**, pressing the Arm button causes a write to register PACR1 bit ARM which arms the phase adjustment or phase alignment. Arming the device enables it to perform the phase adjustment or alignment when the trigger event occurs.

When **Trigger source** is set to **Trigger** button, pressing the Trigger button causes a write to register PACR1 bit TRIG which triggers the phase adjustment or phase alignment

Pressing the Reset button causes a write to register PACR1 bit RST which resets the phase adjustment /alignment state machine

Common GUI Functionality
Phase Measurement Window

- Accessed from Main window Quick Links **Phase Measure** button
- Used to perform a phase measurement between two signals



Selects time base for phase measurement.
- Measurement resolution is the time base period
- Measurement range is +1023 to -1024 time base periods.

Selects the two signals on which the phase measurement is performed. Phase of Signal B with respect to signal A is measured.

Pressing the Start button initiates a phase measurement

Selects whether the rising or falling edge of the signal is used for measurement
- Not inverted = Use rising edge
- Inverted = Use falling edge

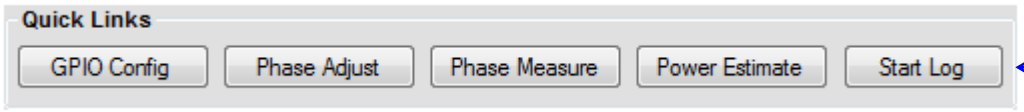
Phase measurement result

Pressing the Reset button stops the current measurement. After a phase measurement completes, the Reset button must be pressed prior to starting a new measurement.

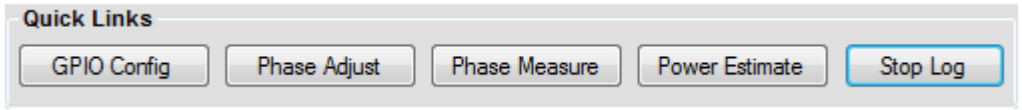
Important Notes:
- The frequency of B must be an integer multiple of the frequency of A
- Before using this feature see the IC data sheet for information on measurement variability and guidance for use.

Common GUI Functionality
Main Window - Device Register Write Logging

- The Main window Quick Links Start/Stop Log button is a toggle button that starts and starts device configuration register write logging to a text file
- Device configuration register writes are performed when device configuration option is changed in the GUI



Device configuration register writes are not currently being logged.
Pressing the Start Log button enables device configuration register write logging.
The user is prompted to specify a log file name.

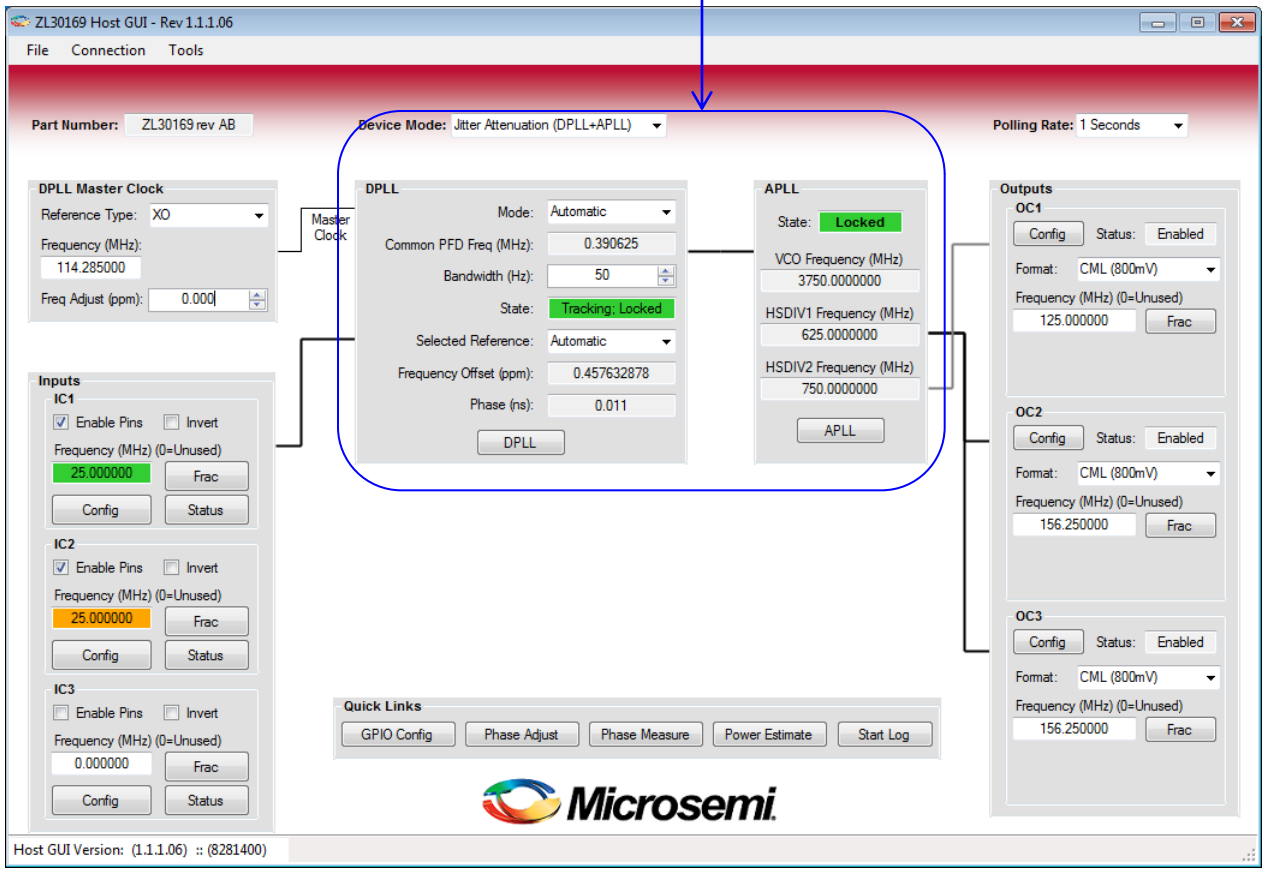


Device configuration register writes are currently being logged.
Pressing the Stop Log button disables logging.

GUI Jitter Attenuation (DPLL+APLL) Mode

GUI Jitter Attenuation (DPLL+APLL) Mode
Window Overview

Jitter attenuation (JA) mode is also known as DPLL+APLL mode



- The DPLL master clock is the reference connected to the device XA/XB pins
- The DPLL can accept up to 3 input clocks
- When connected to a board, the GUI color codes the input clock frequency fields to indicate an input's status
  - Green indicates an input clock is valid
  - Orange indicates an input clock is invalid
  - White indicates an input clock is disabled

GUI Jitter Attenuation (DPLL+APLL) Mode
Input Clock Configuration Window

- Accessed from Main window ICn **Config** button
- Used to configure an input clock's monitor functionality

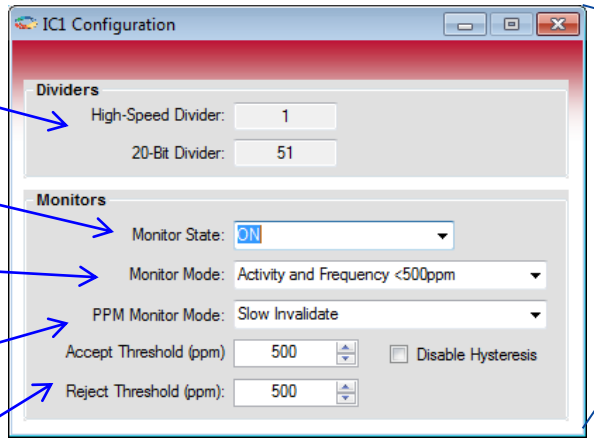
Input divider values chosen by GUI (read-only)

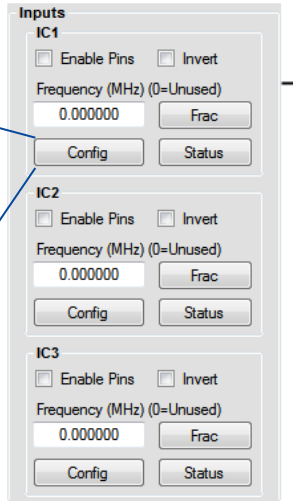
Enable for the input monitor logic

Can choose Activity Only, Activity + ppm freq. monitor or Activity + % freq. monitor

Fast, slow or high jitter tolerance (slowest) monitor averaging time

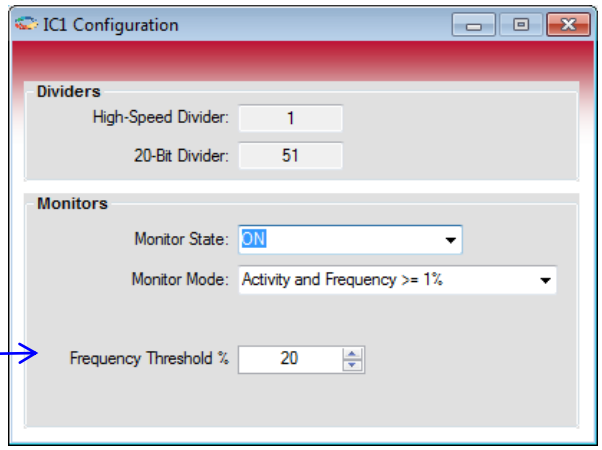
ppm monitor has two thresholds available to implement hysteresis





ppm frequency monitor mode selected - Only available on ZL30151 and ZL30169

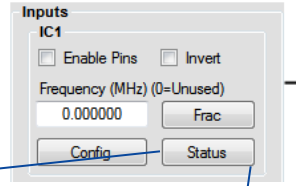
% monitor has one threshold (no hysteresis)

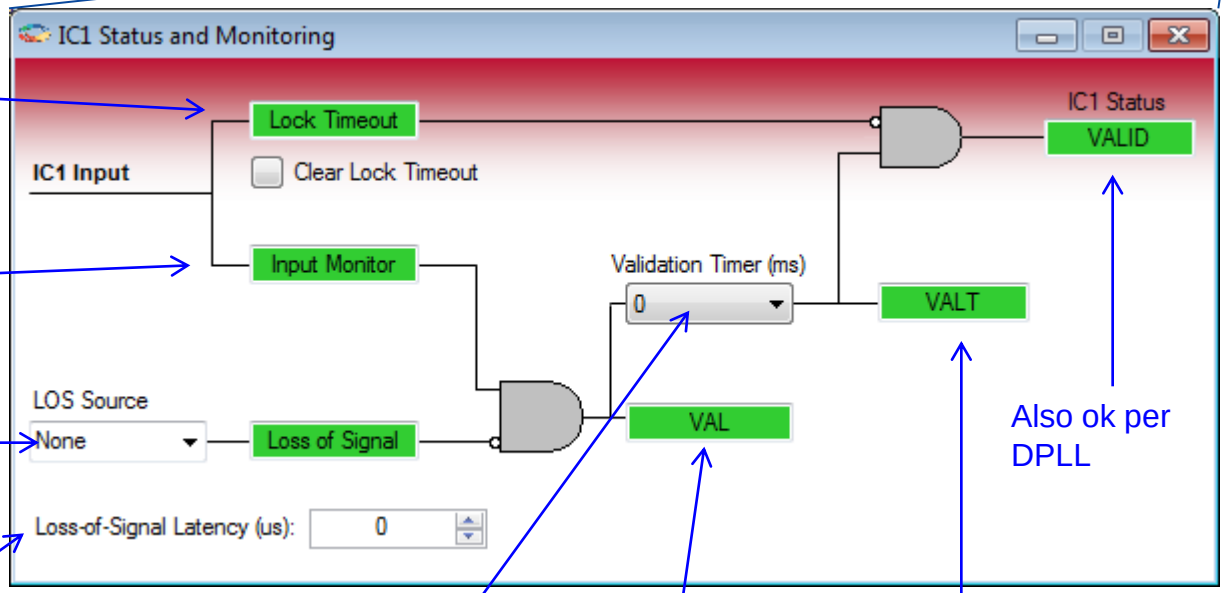


% frequency monitor mode selected – Available on all devices

GUI Jitter Attenuation (DPLL+APLL) Mode
Input Clock Status Window

- Accessed from Main window ICn **Status** button
- Used to view an input clock's monitor's status





DPLL can be configured to "give up" on an input after it fails to lock for a configurable interval. This is the status for that functionality.

Indicates input monitor's real-time status

Any GPIO can be configured to be LOS input for an ICx input clock. (Think LOS output from LIU or Ethernet PHY.)

This is how long it takes for the LOS signal to get to the part. GUI considers this info when setting up the input monitor.

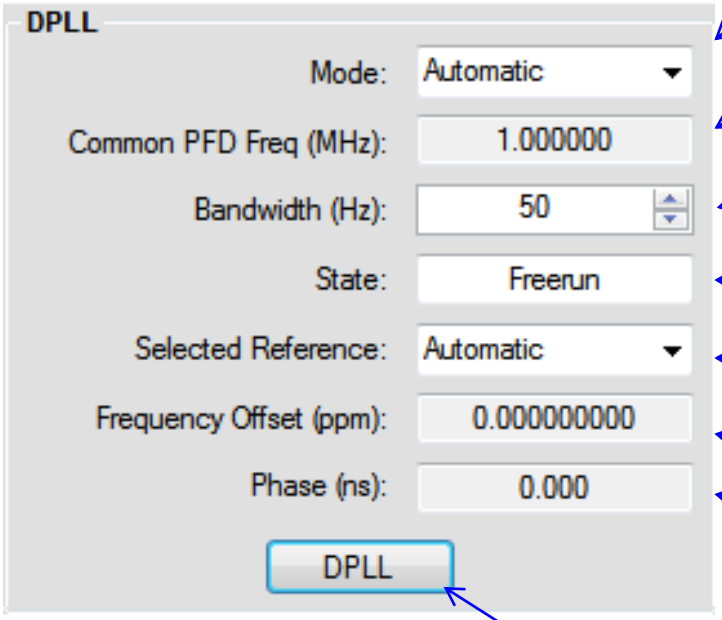
User can require an input to be declared valid by the monitor for an interval before being declared valid by the part.

Valid per monitor and LOS input.

Valid through timer duration.

Also ok per DPLL

GUI Jitter Attenuation (DPLL+APLL) Mode
Main Window DPLL Section



Automatic, freerun or holdover

IC1 to IC3 each divided to this frequency

DPLL Bandwidth
Minimum bandwidth is device dependent

Current state (read-only)

Automatic or force IC1, IC2 or IC3

Current FFO (vs. XA signal) (read-only)

Current phase error, DPLL input vs. feedback (read-only)

Displays DPLL Window which provides access to several DPLL configuration options

GUI Jitter Attenuation (DPLL+APLL) Mode
DPLL Configuration Window

- Accessed from Main window **DPLL** button
- Used to configure DPLL functionality

When jitter tolerance is set higher, input clocks may be further divided

Internal feedback (default) or external through IC1, IC2 or IC3
Note: When external feedback is used, the User Priority of that clock must be set to 0

Revertive or nonrevertive switching

A GPIO can be used to control simple mux switching

User-specified priorities 0=don't use

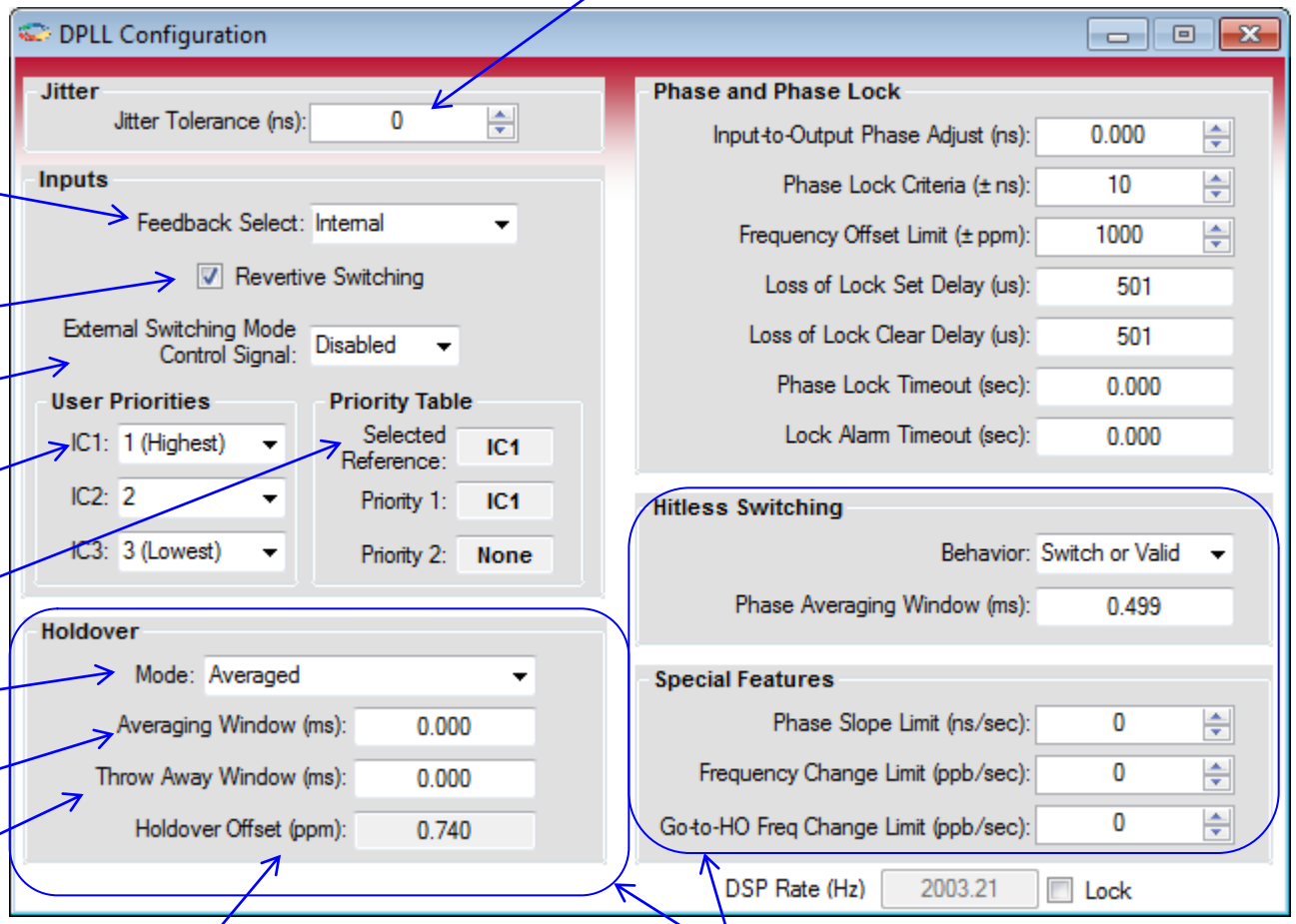
Device's internal table, dynamically calculated

Averaged or freerun behavior

Average over this interval

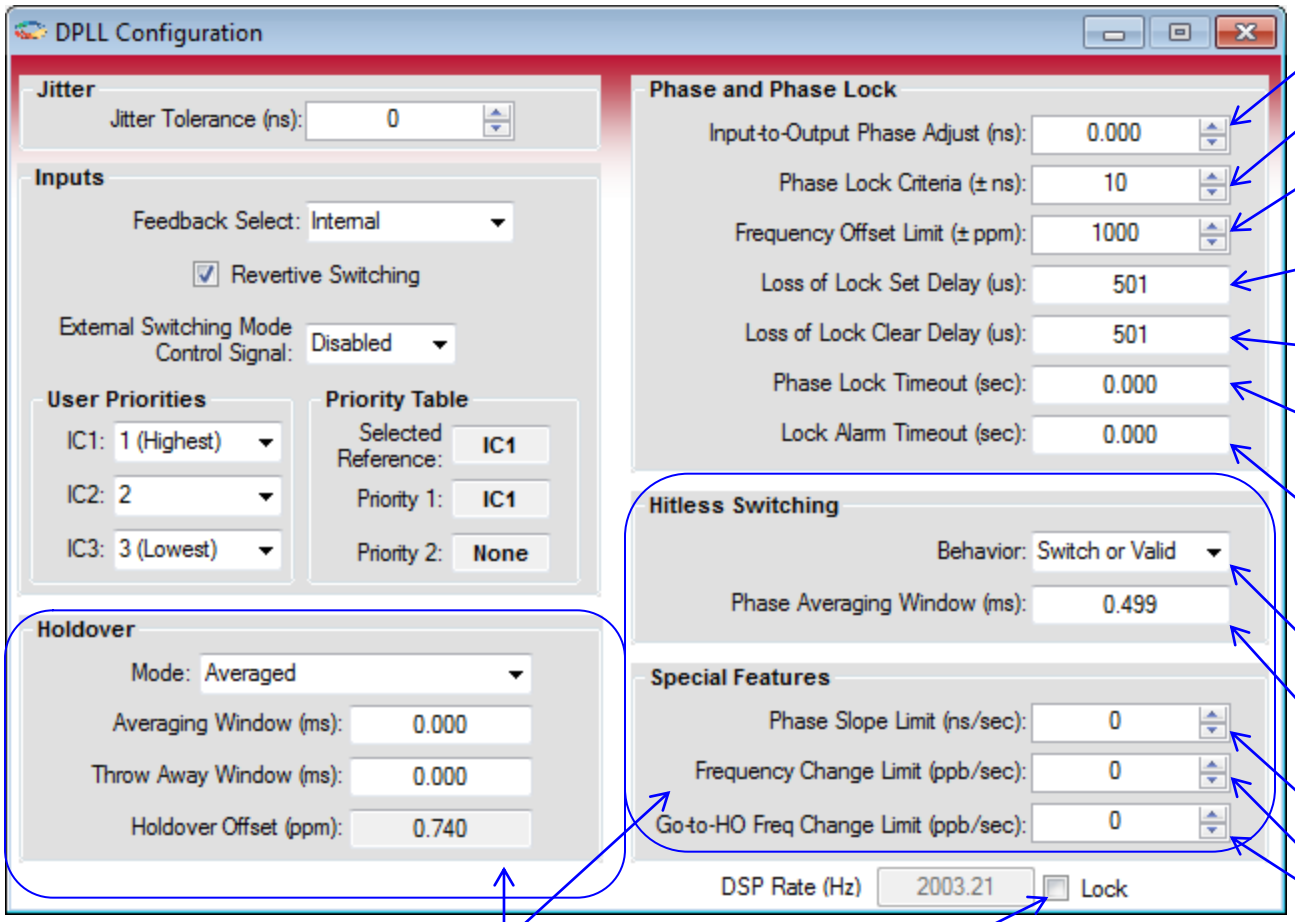
Don't include this most-recent interval in average

Device-calculated HO average (read-only)



These sections ZL30151 and ZL30169 only. Not present on ZL30252 and ZL30253.

GUI Jitter Attenuation (DPLL+APLL) Mode
DPLL Configuration Window



Manual phase adjustment

Defines what lock means

DPLL hard frequency limit

How long DPLL must be out of lock before declaring LOL

How long DPLL must be locked before saying so

How long out of lock before invalidating the input (0=don't invalidate)

Duration between DPLL invalidation of input and auto-clear of phase lock time out condition

Hitless switching on/off

How long to measure phase before doing hitless switch

max phase rate-of-change

Max freq rate-of-change

These sections ZL30151 and ZL30169 only.
Not present on ZL30252 and ZL30253.

Lock DSP rate at current displayed frequency
Should be unchecked for most applications.
Contact factory for support with this option.

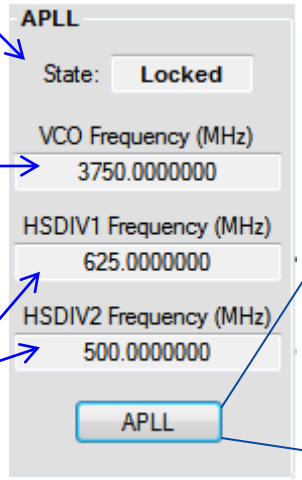
GUI Jitter Attenuation (DPLL+APLL) Mode
Main Window APLL Section and APLL Configuration Window

On Main Window:
(all fields read-only)

APLL locked or unlocked

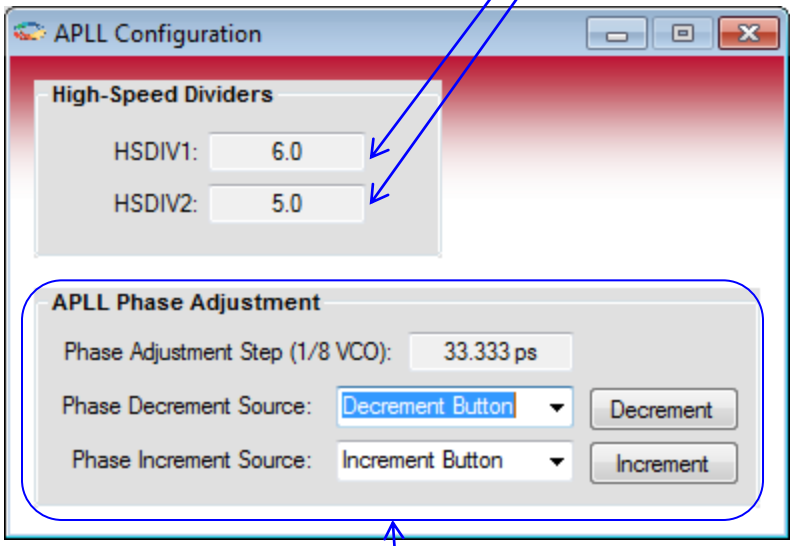
VCO frequency chosen by GUI

output freqs of 2 high-speed dividers chosen by GUI



APLL Window:

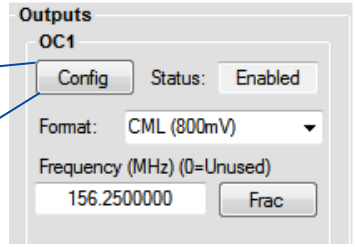
high-speed divide values chosen by GUI (read-only)

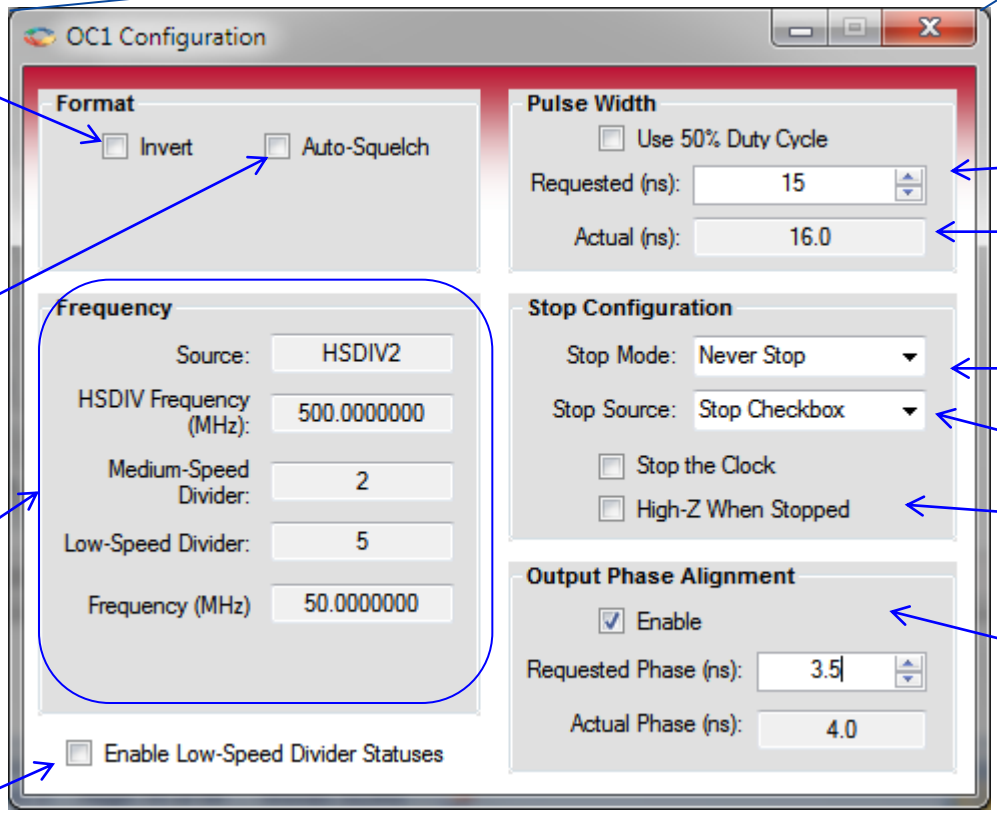


APLL has its own phase adjust in 1/8 VCO cycle steps. This can be controlled by any GPIO or DEC and INC bits. (GUI fronts the bits with buttons.)

GUI Jitter Attenuation (DPLL+APLL) Mode
Output Clock Configuration Window

- Accessed from Main window OCn **Config** button
- Used to configure output clock functionality





Invert output clock signal polarity

When this is checked, output is automatically stopped when DPLL has no valid input

Read-only display of settings chosen by GUI

Check this and a status bit can follow the LSDIV output.
Useful for periodic interrupt out and clock signals out of GPIO pins.

Pulse width:
User gives request

GUI shows closest setting part can do

Stop high, stop low or never stop

Any GPIO or STOP bit

Controls the STOP bit

GUI only accepts >0 values. All values relative to arbitrary zero point.

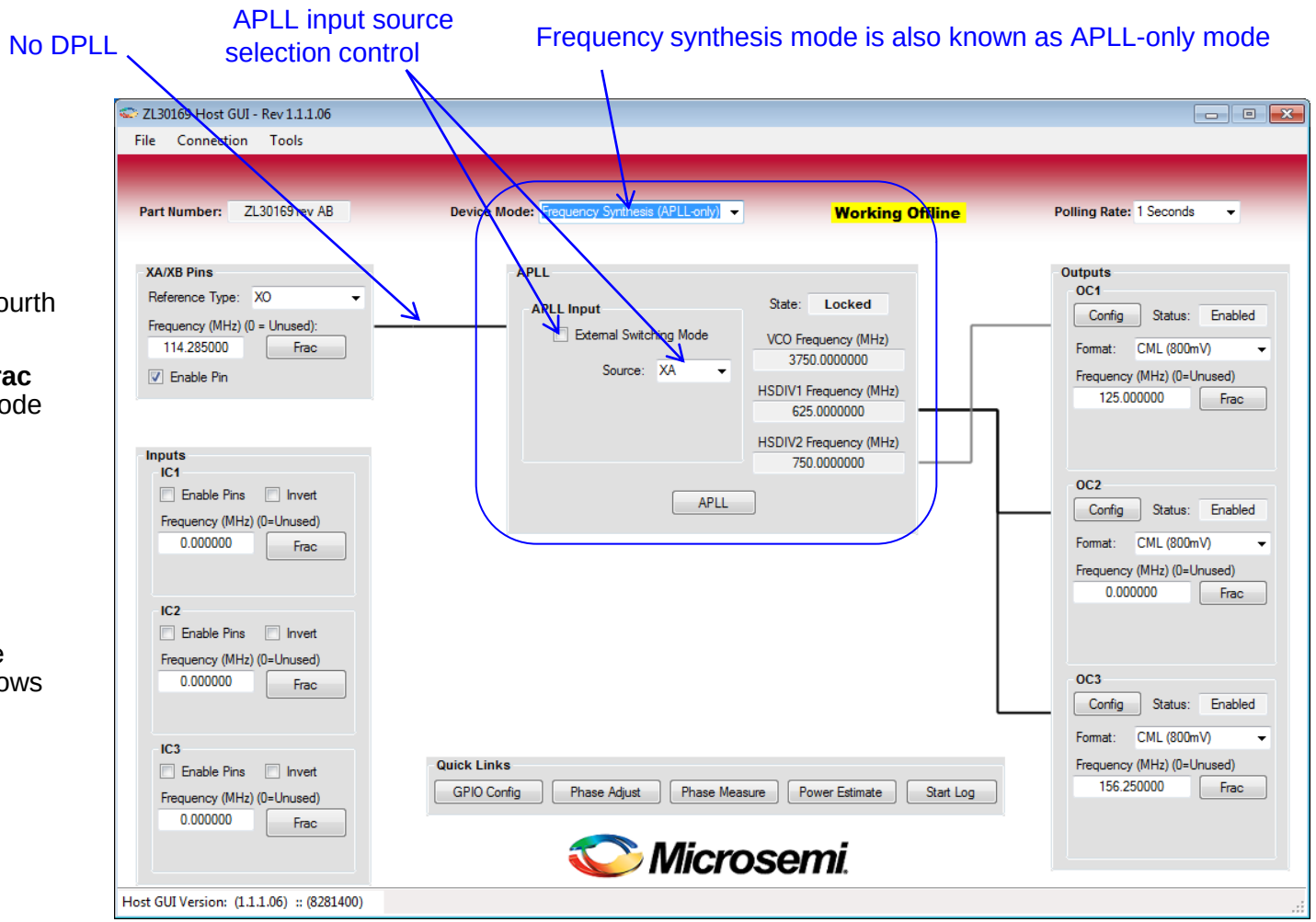
GUI Jitter Attenuation (DPLL+APLL) Mode
Notes

- Master clock required on XA pin must fall in specific ranges:
  - XO, doubler off: 98-104MHz, 110-115MHz, 124-130MHz
  - crystal, doubler on: 49-52M or 55-57.5M
- In this mode XA, ICn clock group, and OCn clock group have no frequency relationship rules with respect to each other
- IC1 to IC3 have a frequency relationship rule:
  - Each must be divisible to common DPLL PFD frequency between 1kHz and 500kHz.
    - IC1=19.44MHz, IC2=25MHz and IC3=156.25MHz is OK: common PFD freq is 10kHz
    - IC1=156.25MHz, IC2=156.25M*66/64 not ok, no common divisor.
- OC1 to OC3 have a frequency relationship rule:
  - Each output clock must be derivable from a common APLL VCO frequency using one of two divider paths. Each divider path can contain integer dividers and at most one half-divider (4.5, 5.5, 6.5, 7.5).
    - OC1=156.25MHz, OC2=125MHz and OC3=100MHz is OK: common APLL VCO frequency is 3750MHz
    - OC1=156.25MHz, OC2=156.25M*66/64 not ok, no common APLL VCO frequency
  - The GUI input and output clock frequency solver checks the configuration against these rules and displays an error message if violated

GUI Frequency Synthesis (APLL-only) Mode

GUI Frequency Synthesis (APLL-only) Mode
Main Window

- In frequency synthesis mode XA/XB is just a fourth input
  - XA/XB has a **Frac** button in this mode
- In frequency synthesis mode inputs don't have **Config** or **Status** windows

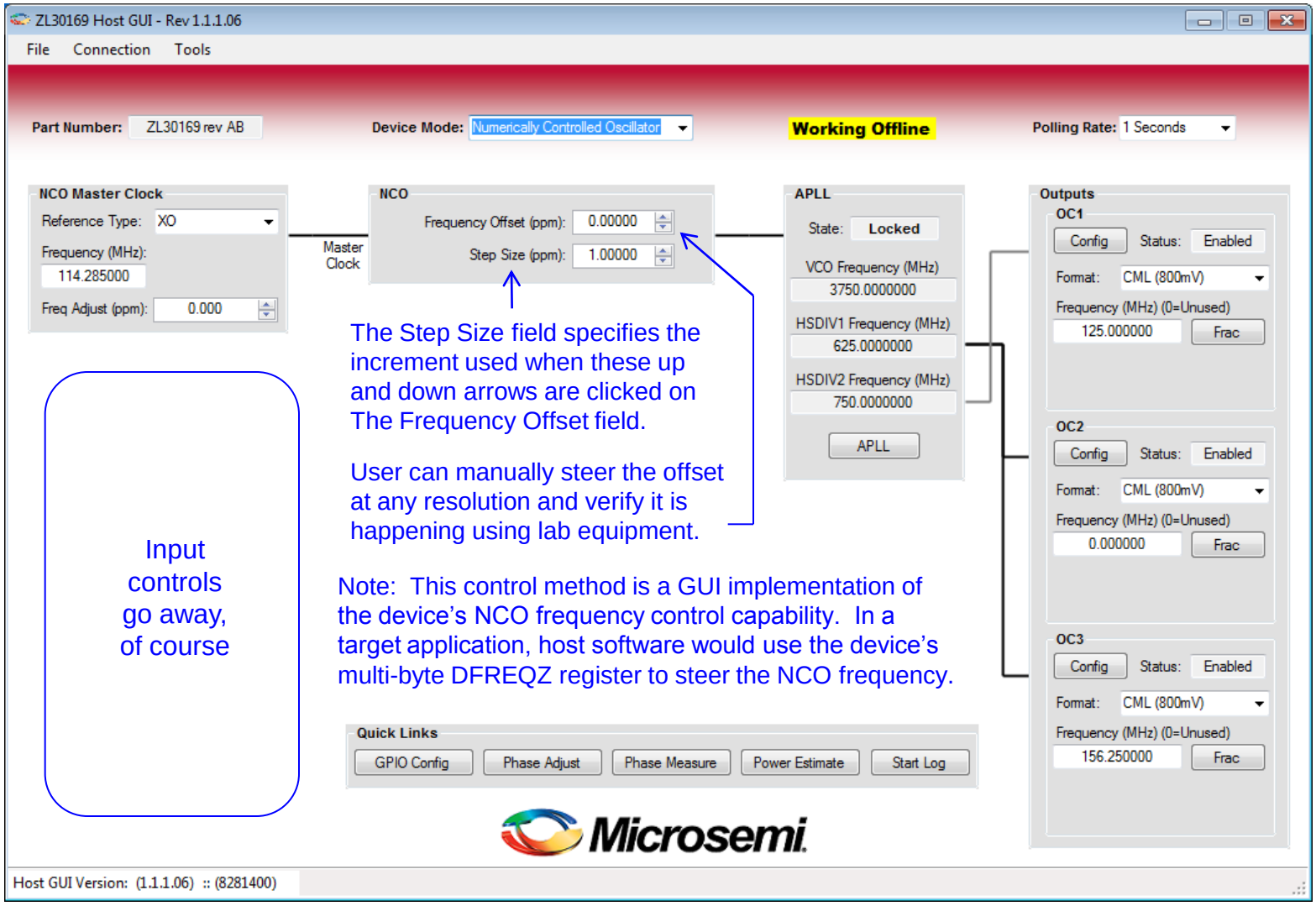


GUI Frequency Synthesis (APLL-only) Mode
Notes

- Synthesis mode is APLL-only and does not need a master clock
- XA is just one of four input clocks
- XA, IC1, IC2 and IC3 have the following frequency relationship rule:
  - All participating inputs after HSDIV (at APLL phase detector) must be same frequency
    - IC1 to IC3 have HSDIV (1, 2, 4 or 8)
    - XA does not have HSDIV
    - If XA is used, XA's frequency sets the phase detector frequency and IC1 to IC3 must each be 1, 2, 4 or 8 times XA
- Minimum APLL input frequency is 9.72MHz
- If lower input frequencies are required, DPLL+APLL mode must be used
- The higher the input frequency the lower the output jitter all else being equal
- OC1 to OC3 have the following frequency relationship rule:
- Each output clock must be derivable from a common APLL VCO frequency using one of two divider paths. Each divider path can contain integer dividers and at most one half-divider (4.5, 5.5, 6.5, 7.5).
    - OC1=156.25MHz, OC2=125MHz and OC3=100MHz is OK: common APLL VCO frequency is 3750MHz
    - OC1=156.25MHz, OC2=156.25M*66/64 not ok, no common APLL VCO frequency
- The GUI input and output clock frequency solver checks the configuration against these rules and displays an error message if violated

GUI Numerically Controlled Oscillator Mode

GUI Numerically Controlled Oscillator Mode
Main Window



GUI Numerically Controlled Oscillator Mode
Notes

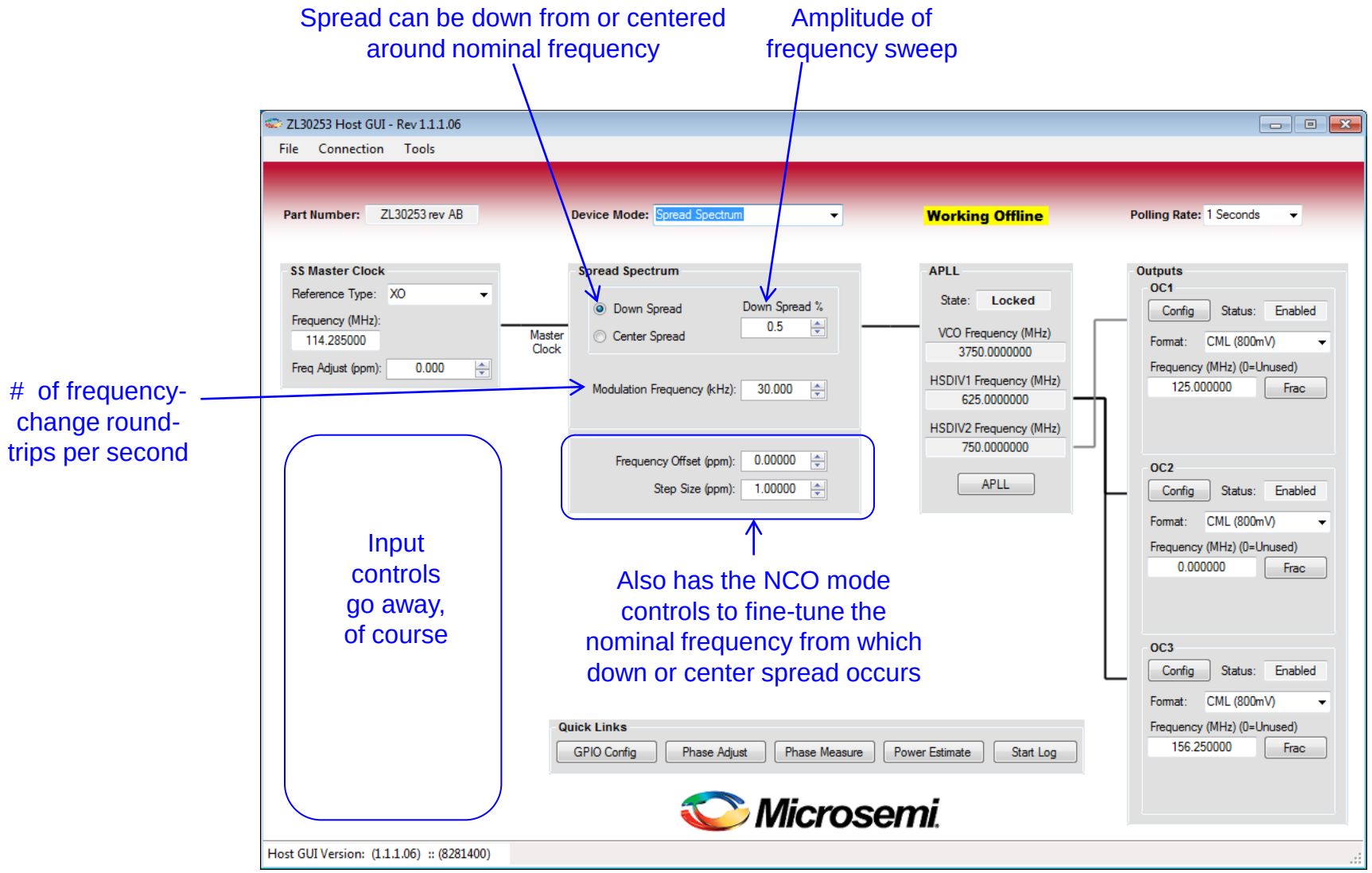
- Uses DPLL's DCO block but not its DSP, doesn't need DSP code loaded
- Master clock required on XA pin must fall in specific ranges:
  - XO, doubler off: 80-130MHz (wider than JA mode because input sampler not needed)
  - crystal, doubler on: 40-60MHz
- Data sheet publishes the function customers need for real-time steering of the frequency offset:

  newFREQZ = round(FREQZ0 * (1 + FFO/1e6))

  where
  - FREQZ0 is the nominal DCO tuning word calculated by the GUI. It is read from the part by the customer's software at system start-up.
  - FFO is the desired fractional frequency offset in ppm
  - newFREQZ is the new 40-bit tuning word to be written to the DFREQZ registers

GUI Spread Spectrum Mode

GUI Spread Spectrum Mode
Main Window



GUI Spread Spectrum Mode
Notes

- Uses DPLL's DCO block but not its DSP, doesn't need DSP code loaded
- Master clock required on XA pin must fall in specific ranges:
  - XO, doubler off: 80-130MHz (wider than JA mode because input sampler not needed)
  - crystal, doubler on: 55-60MHz
- With XO:
  - Center spread range is -0 to ±0.5%
  - Down spread range is 0 to 1%
  - Modulation frequency range is 25 to 55kHz
- With crystal:
  - Center spread range is 0 to ±0.25%
  - Down spread range is 0 to 0.5%
  - Modulation frequency range is 25 to 35kHz
- Data sheet doesn't publish spread spectrum registers. The GUI must be used to configures these.

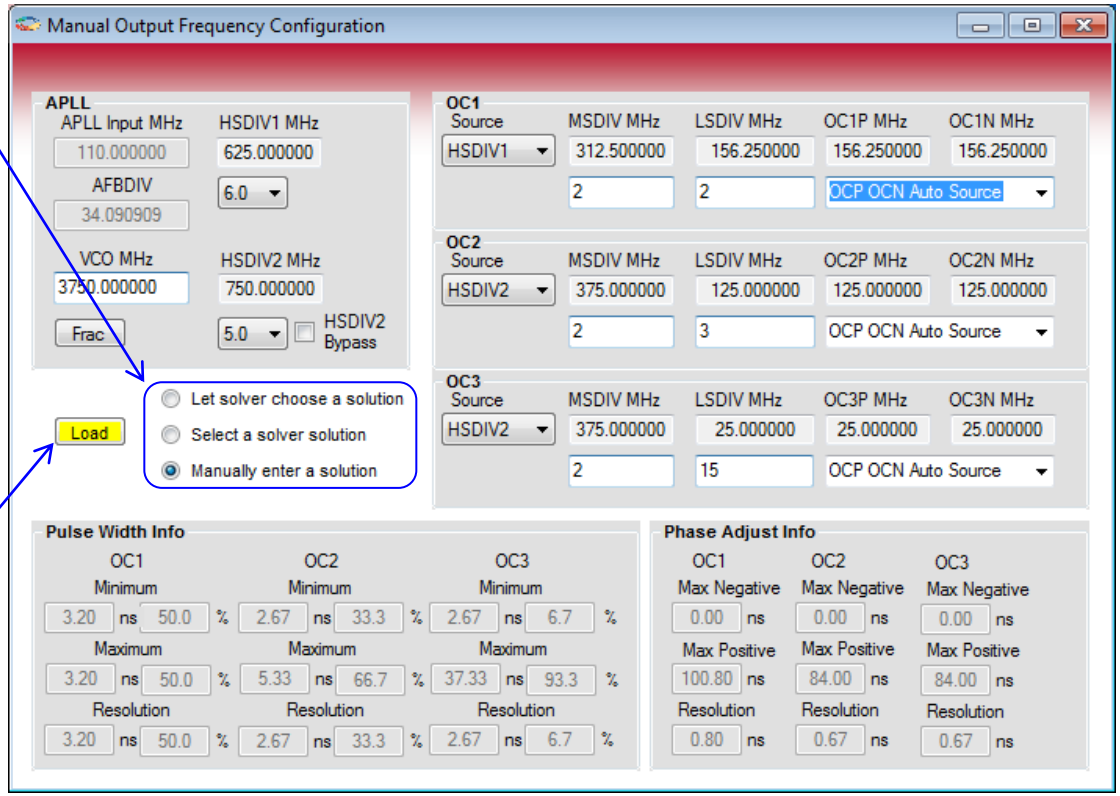
GUI Tools

GUI Tools
Manual Output Frequency Configuration Window

- Accessed from main window menu: Tools → Manual Output Frequency Configuration
  - This menu can be used to override the default output clock configuration chosen by the GUI

Three modes of operation

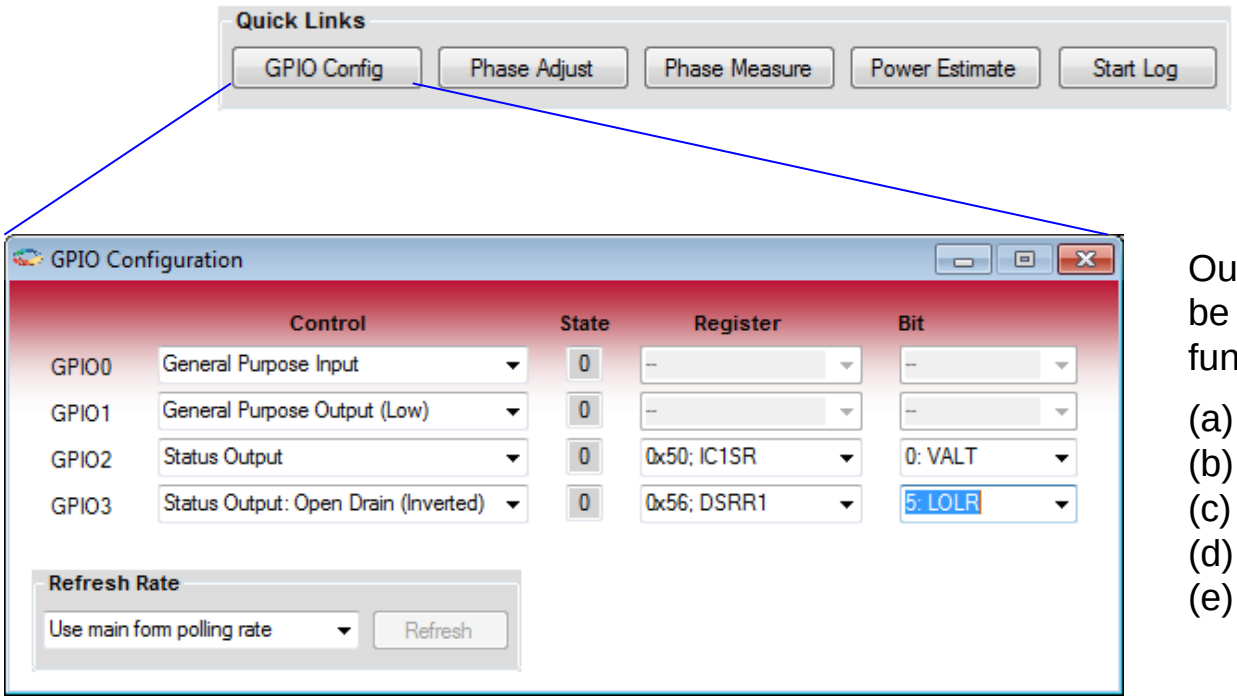
1. **Let solver choose a solution**
   - Default mode of operation
   - This mode can be used to view the frequency plan chosen by GUI
2. **Select a solver solution**
   - The output clock solver typically determines multiple valid output clock frequency solutions. It then selects the optimal solution based on the selected device configuration options.
   - This mode can be use to select an alternate valid output clock solution
3. **Manually enter a solution**
   - This mode can be used to manually enter a custom output clock configuration
   - The GUI performs no error checking in this mode. It is the responsibility of the use to ensure that the output clock configuration is valid. Refer to the ZL30151/169/25x data sheet for configuration restrictions.



The **Load** button is used to load the new output clock frequency plan selected in this window into the device**.** The load button turns yellow to indicate that the window configuration no longer matches the device configuration.

GUI Tools
GPIO Configuration Window

- Accessed from main window Tools menu → GPIO Configuration
  - Also accessible from main window Quick Links **GPIO Config** button
- The 4 GPIOs can be configured as inputs, output low, output high, or status
- Status outputs can be non-inverted, inverted, open-drain or inverted open-drain
- Status outputs can be configured to follow any bit in any status register in the part

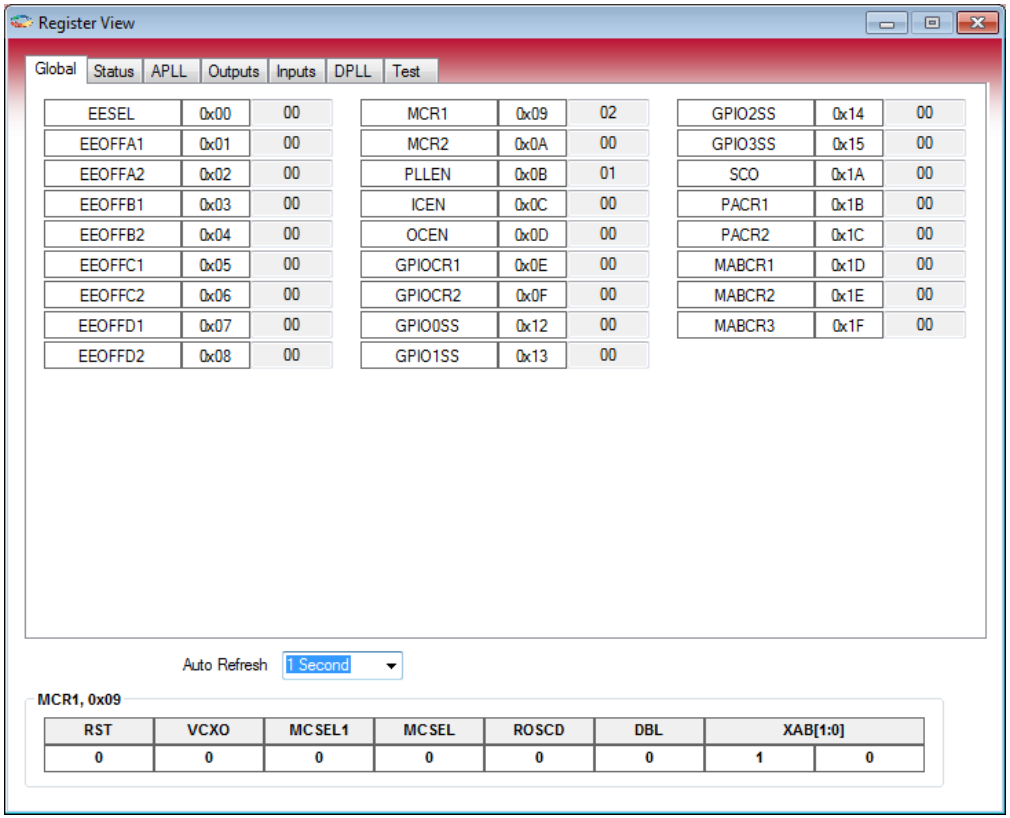


Outside this window GPIOs can be configured for several functions including:

(a) input clock selector
(b) invalidate an input clock
(c) align outputs
(d) inc/dec APLL phase
(e) start/stop outputs

GUI Tools
Register View Window

- Accessed from main window Tools menu → Register View
- Allows lower level access to registers and register fields
- Registers are grouped by function



GUI Tools
Device Configuration Files

Two types of configuration files are supported:

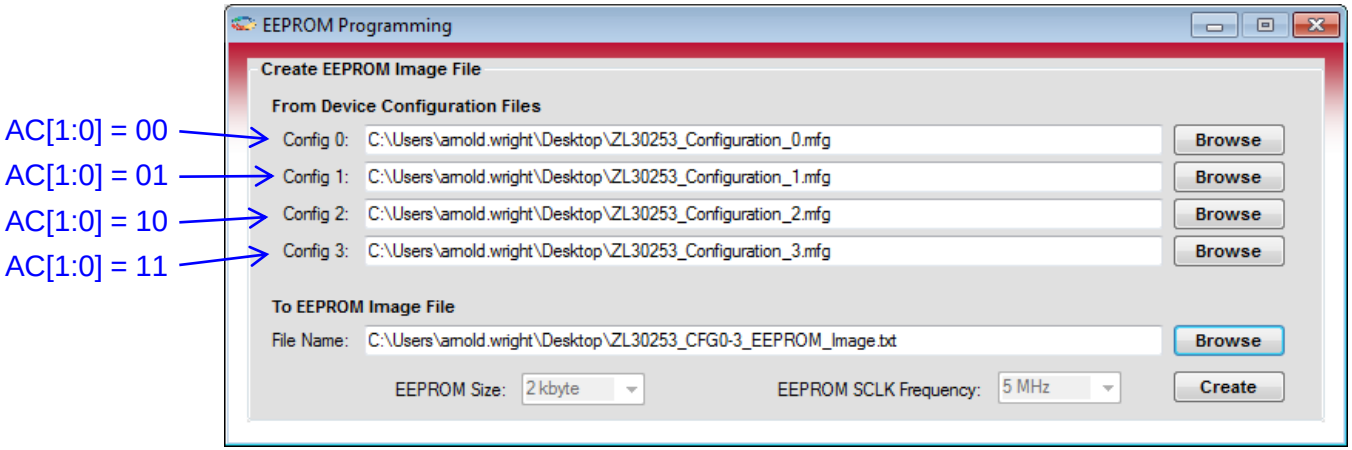
1) GUI config files
   - Fully configure everything the HAL is expecting at a data structure level
   - Accessed from Main window File menu
     - Save a GUI configuration file: File → Save Configuration → GUI Configuration
     - Load a GUI configuration file: File → Load Configuration → GUI Configuration
   - May be removed in future GUI release

2) DUT config files (.MFG files)
   - Provide an order list of writes and waits that can be followed to configure a part
   - Used by host software to configure the device via its SPI/I2C interface
   - Used to create an EEPROM image file
     - Save a DUT configuration file: File → Save Configuration → DUT Configuration
     - Loading a GUI configuration file is not currently supported. Will be added to a future GUI release.

```
; MFG file snippet
X , 0X0009 , 0X15 ; MCR1
X , 0X0101 , 0X02 ; APLLCR2
X , 0X0102 , 0X06 ; APLLCR3
X , 0X0106 , 0XF5 ; AFBDIV1
X , 0X0107 , 0X09 ; AFBDIV2
```

GUI Tools
Create EEPROM Image File Window

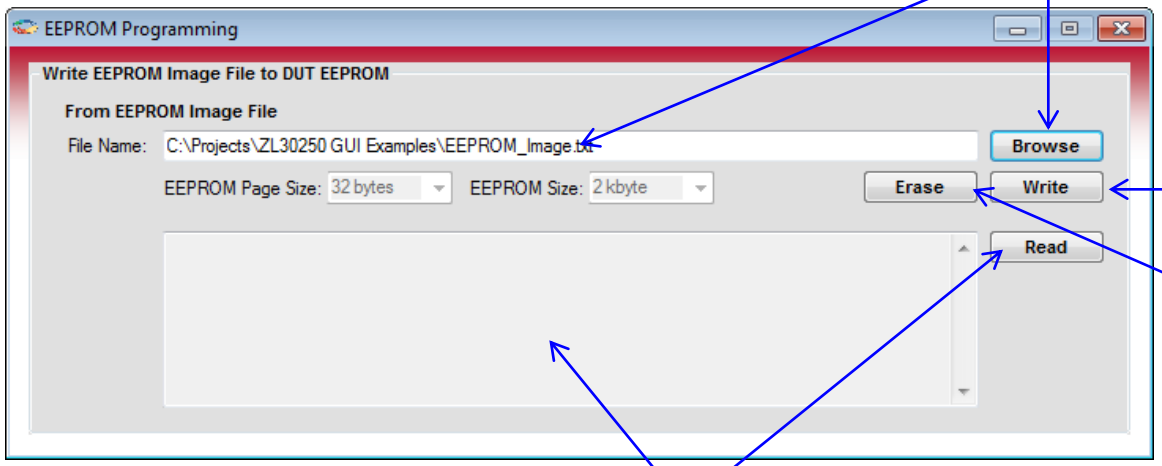
- Accessed from main window menu: File → EEPROM → Create EEPROM Image File
- Used to create an EEPROM image file from a DUT configuration file (.mfg)
- Can merge up to 4 DUT configuration files into a single EEPROM image file
- Used to create EEPROM image files for devices with both internal and external EEPROMs
- 3 supported EEPROM files types
  - ASCII Hex (Used for factory programming)
  - Intel Hex
  - Motorola S-record
- State of device pins AC[1:0] at reset de-assertion determines which configuration is loaded



GUI Tools
Write EEPROM Image File to DUT EEPROM Window

- Accessed from main window menu: File → EEPROM → Write Image to EEPROM → Write to DUT EEPROM
  - Only accessible when the GUI is connected to a device
- Use this window to write an EEPROM image file to a ZL30151, ZL30169, ZL30251, or ZL30253 internal EEPROM

EEPROM Image file to be programmed into EEPROM
- File type specified when file is selected or specified on pop-up menu



Write EEPROM image file to EEPROM

Erase the EEPROM
- 0xFF written to EEPROM
- Erase the EEPROM to prevent it from loading a configuration on power-up

Read and view the contents of the EEPROM
- Use main window File → EEPROM → Dump DUT EEPROM to File to save the contents of the EEPROM to a file

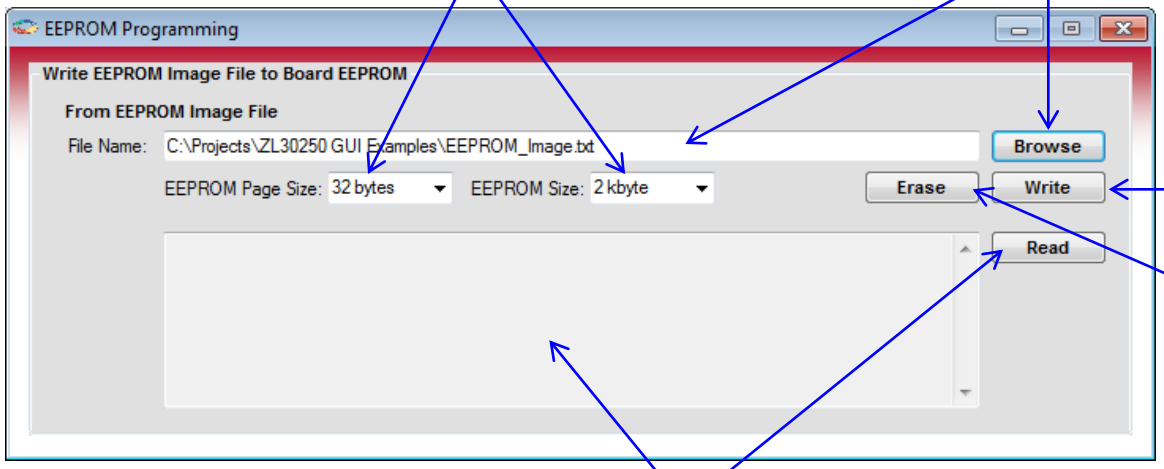
GUI Tools

Write EEPROM Image File to Board EEPROM Window

- Accessed from main window menu: File → EEPROM → Write Image to EEPROM → Write to Board EEPROM
  - Only accessible when the GUI is connected to a device
- Use this window to write an EEPROM image file to the evaluation board external EEPROM connected to a ZL30250 or ZL30252

EEPROM Image file to be programmed into EEPROM
- File type specified when file is selected or specified on pop-up menu

Specify external EEPROM size and page size



Write EEPROM image file to EEPROM

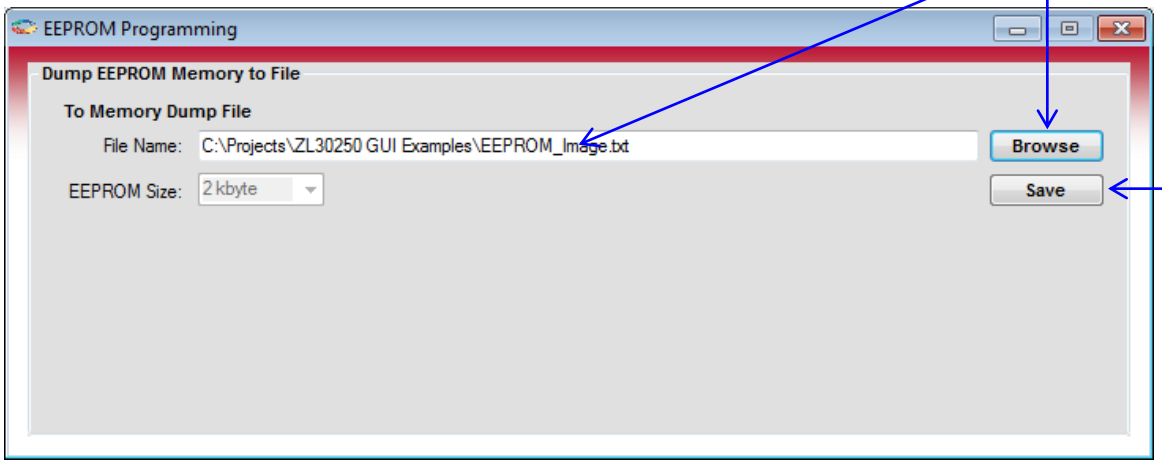
Erase the EEPROM
- 0xFF written to EEPROM
- Erase the EEPROM to prevent it from loading a configuration on power-up

Read and view the contents of the EEPROM
- Use main window File → EEPROM → Dump Board EEPROM to File to save the contents of the EEPROM to a file

GUI Tools
Dump DUT EEPROM Memory to File Window

- Accessed from main window menu: File → EEPROM → Dump DUT EEPROM to File
  - Only accessible when the GUI is connected to a device
- Use this window to save the contents of a ZL30151, ZL30169, ZL30251, or ZL30253 internal EEPROM to a file

Target file for storing the EEPROM image
- File type specified when file is selected or specified on pop-up menu



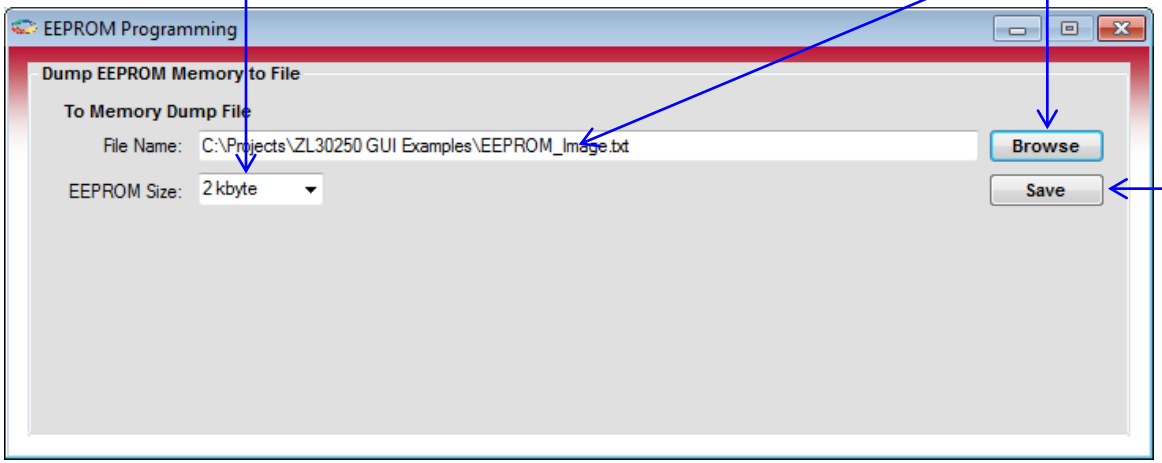
Save the contents of the EEPROM to the specified file

GUI Tools
Dump Board EEPROM Memory to File Window

- Accessed from main window menu: File → EEPROM → Dump Board EEPROM to File
  - Only accessible when the GUI is connected to a device
- Use this window to save the contents of an external EEPROM connected to a ZL30150 or ZL30252 to a file

Specify external EEPROM size

Target file for storing the EEPROM image
- File type specified when file is selected or specified on pop-up menu

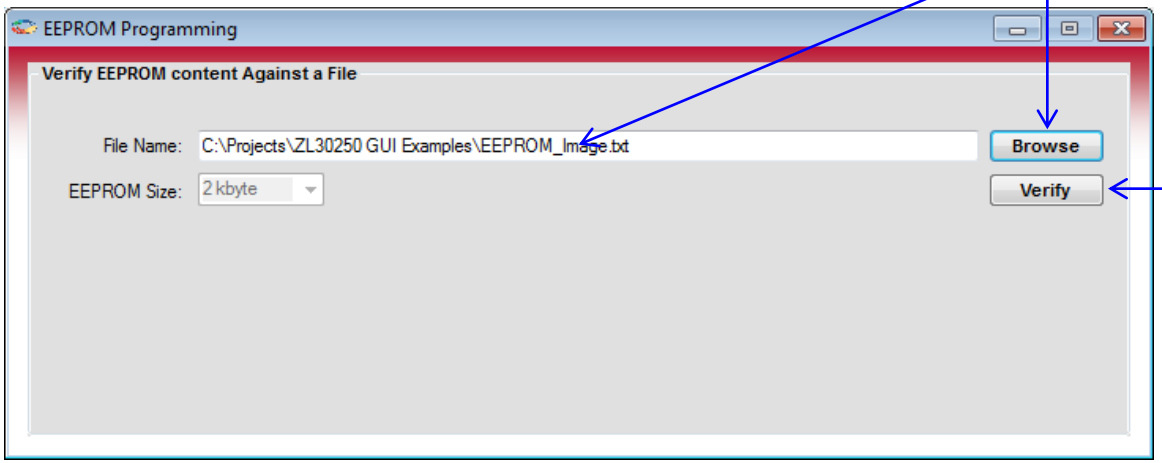


Save the contents of the EEPROM to the specified file

GUI Tools
Verify DUT EEPROM against File Window

- Accessed from main window menu: File → EEPROM → Verify DUT EEPROM against File
  - Only accessible when the GUI is connected to a device
- Use this window to verify the contents of a ZL30151, ZL30169, ZL30251, or ZL30253 internal EEPROM against the specified EEPROM image file

EEPROM image file compared to the device EEPROM contents
- File type specified when file is selected or specified on pop-up menu



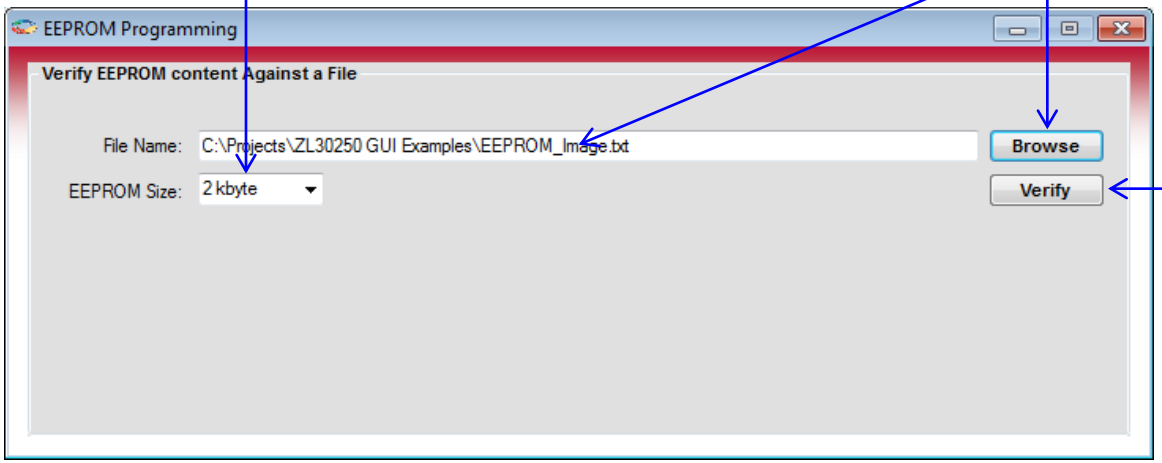
Verify device EEPROM against specified EEPROM image file

GUI Tools
Verify Board EEPROM against File Window

- Accessed from main window menu: File → EEPROM → Verify Board EEPROM against File
  - Only accessible when the GUI is connected to a device
- Use this window to verify the contents of an external EEPROM connected to a ZL30250 or ZL30252 against the specified EEPROM image file

Specify external EEPROM size

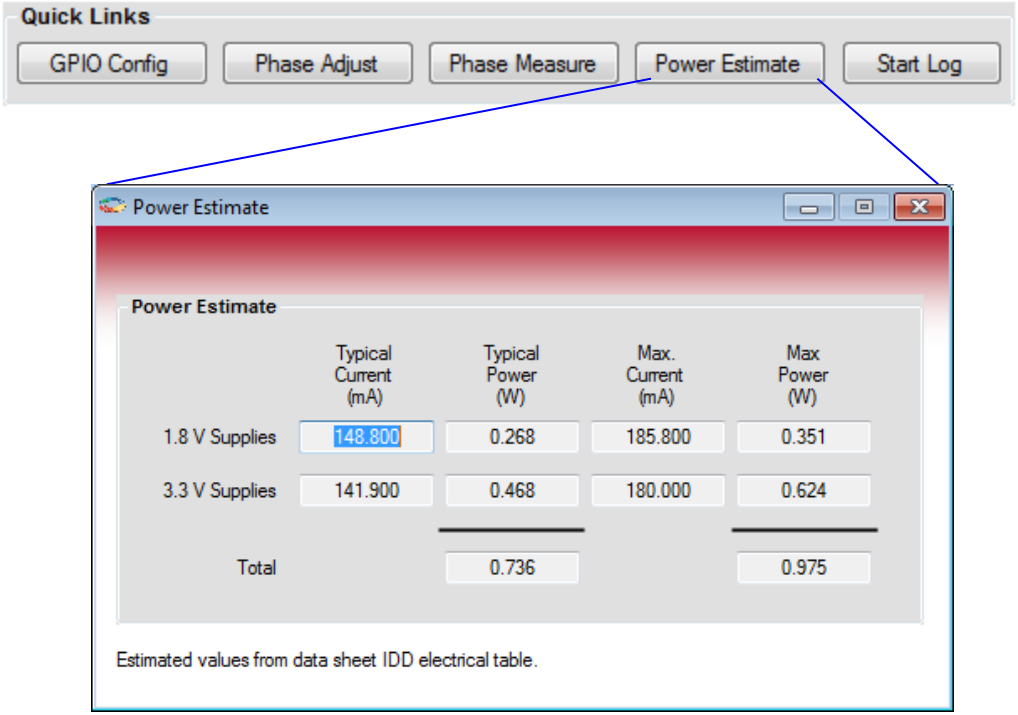
EEPROM image file compared to the device EEPROM contents
- File type specified when file is selected or specified on pop-up menu



Verify device EEPROM against specified EEPROM image file

Common GUI Functionality
Power Estimate Window

- Accessed from main window menu: Tools → Power Estimate
  - Also accessible from main window Quick Links **Power Estimate** button
- The Power Estimate windows provides the estimated typical current and power, and max current and power for the specified device configuration based on the device data sheet IDD electrical table



GUI Tools
Documentation

- Accessed from main window menu: Tools→ Documentation
- GUI Manual
- Release Notes
- Eval Board Quick Start Guide
  - Provides a useful summary of the evaluation board default jumper and switch settings
  - Provides a useful summary of how to configure the board to connect various reference clock options to the ZL30151/ZL30169/ZL3025x

Creating a Frequency Synthesis Mode Device Configuration

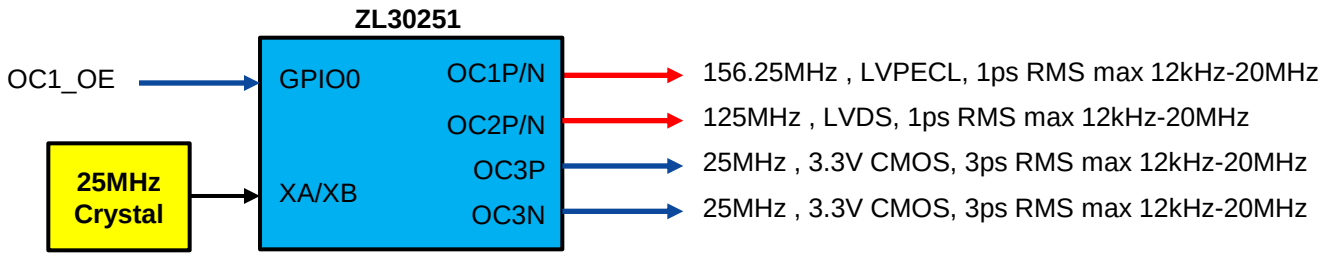
Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

- Key application requirements
  - Self-configuration at startup
  - All output clocks have <1ps max RMS 12kHz-20MHz jitter requirement
  - 156.25MHz must have pin-controlled output enable/disable: 0 = disabled, 1 = enabled

- Key implementation details
  - EEPROM-based ZL30251 used to meet self-configuration at startup requirement
    - EEPROM configuration stored in slot 0
    - ZL30251 pins GPIO1/AC1 and GPIO1/AC0 must be low at RSTN pin de-assertion for device to load configuration from EEPROM slot 0
  - Application output clock jitter requirements are easily met so a 25MHz crystal reference is used to minimize solution cost
  - GPIO0 used to provide pin-controlled output enable/disable of OC1P/N 156.25MHz output clock
    - GPIO0 is also used to specify which device configuration to load from EEPROM
    - ZL30251 OC1P/N output enabled/disable control must be 0 at ZL30251 RSTN pin de-assertion for device to load configuration from EEPROM slot 0
  - 800mV CML mode used to provide LVPECL compatible output clock signal levels
  - 400mV CML mode used to provide LVDS compatible output clock signal levels

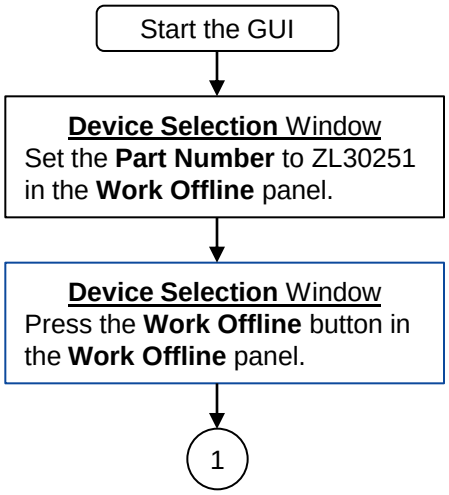
Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

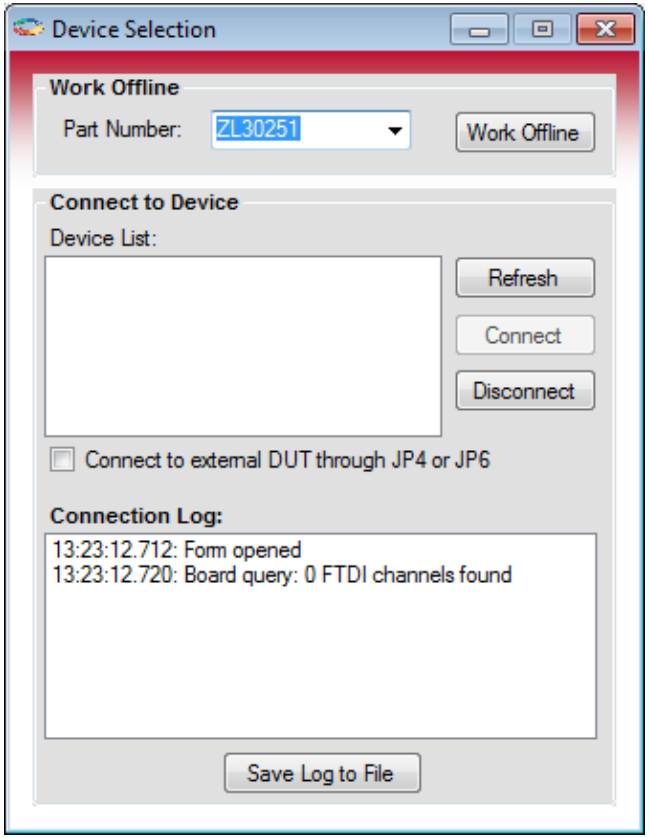
- ZL30251 Block Diagram



Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

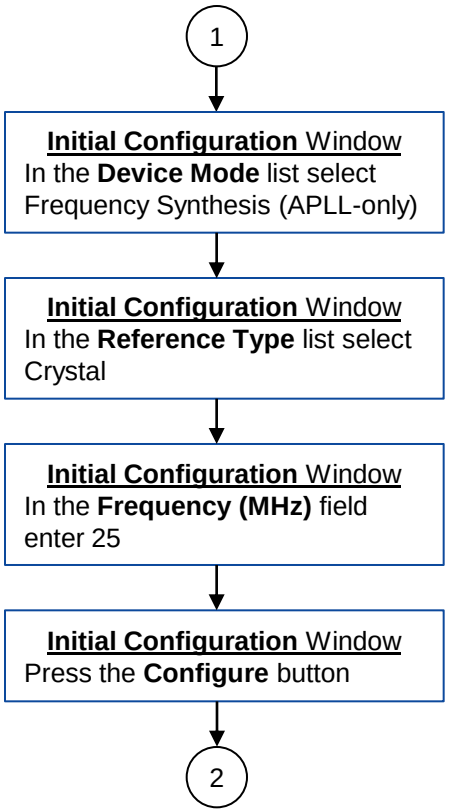
Select the device

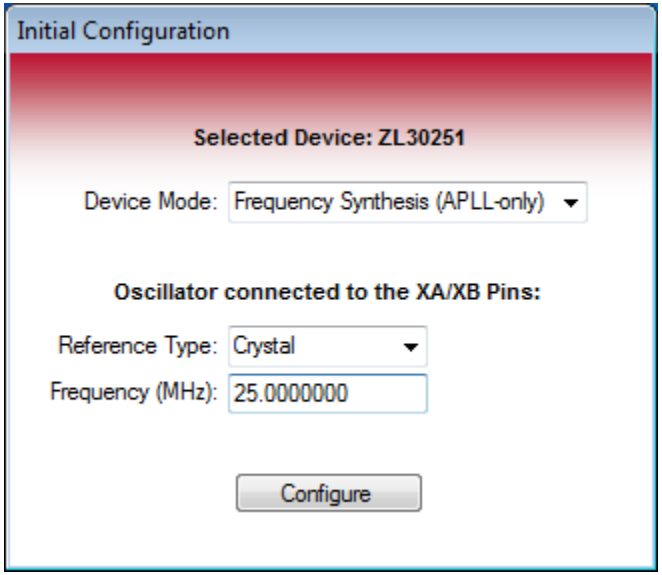




Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

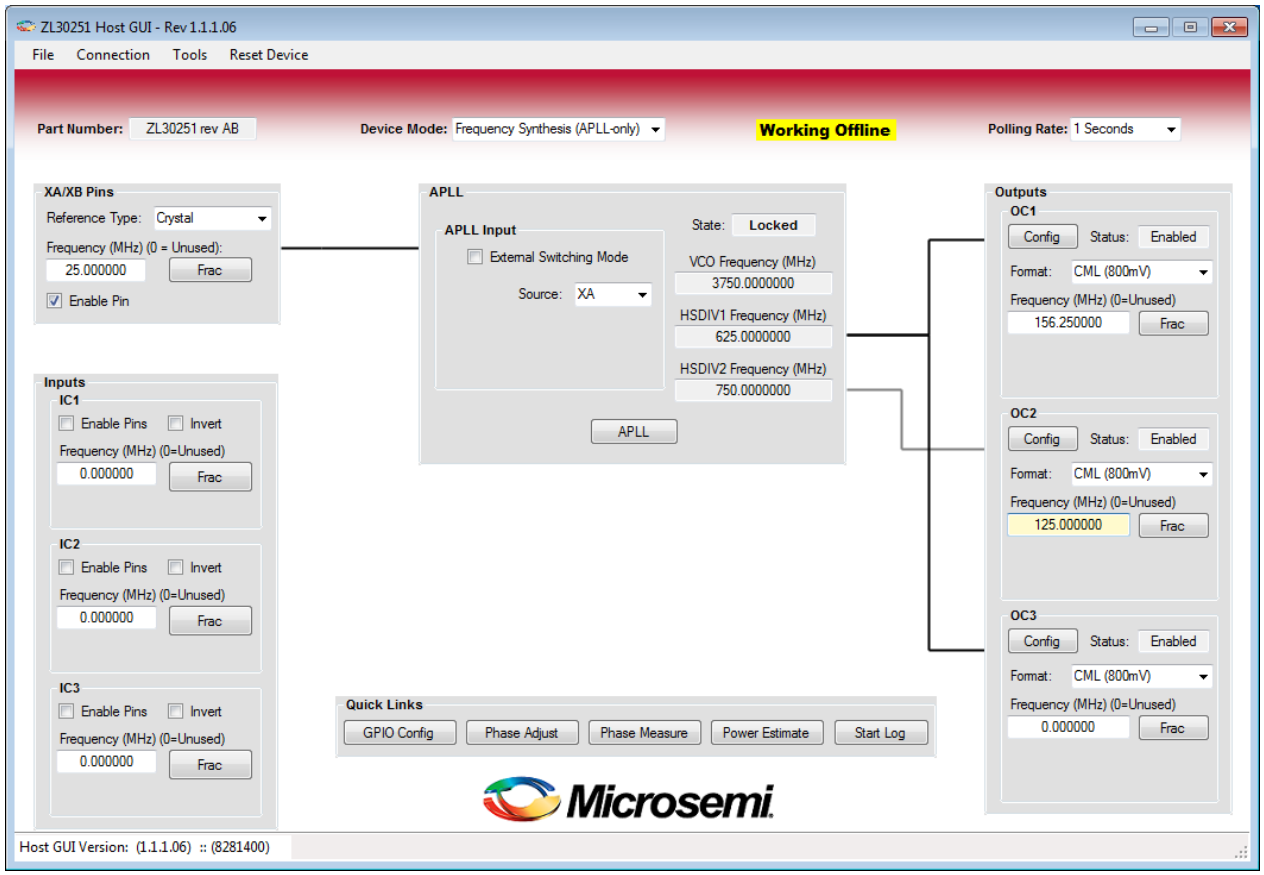
Configure the reference type and frequency

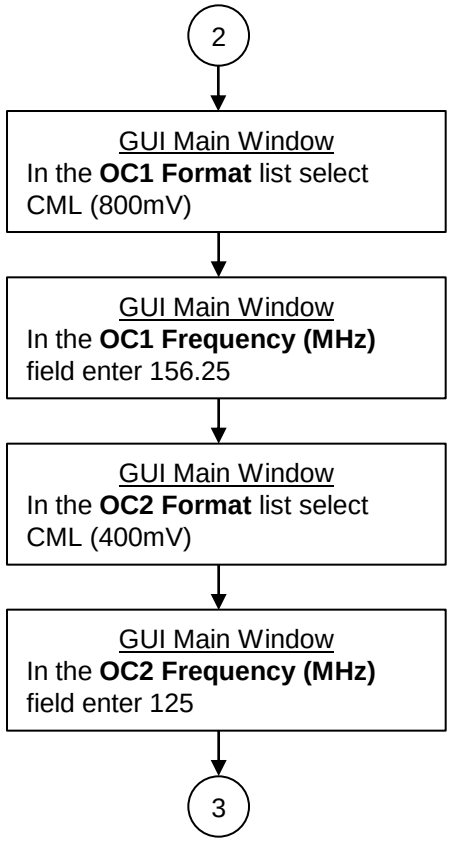




Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

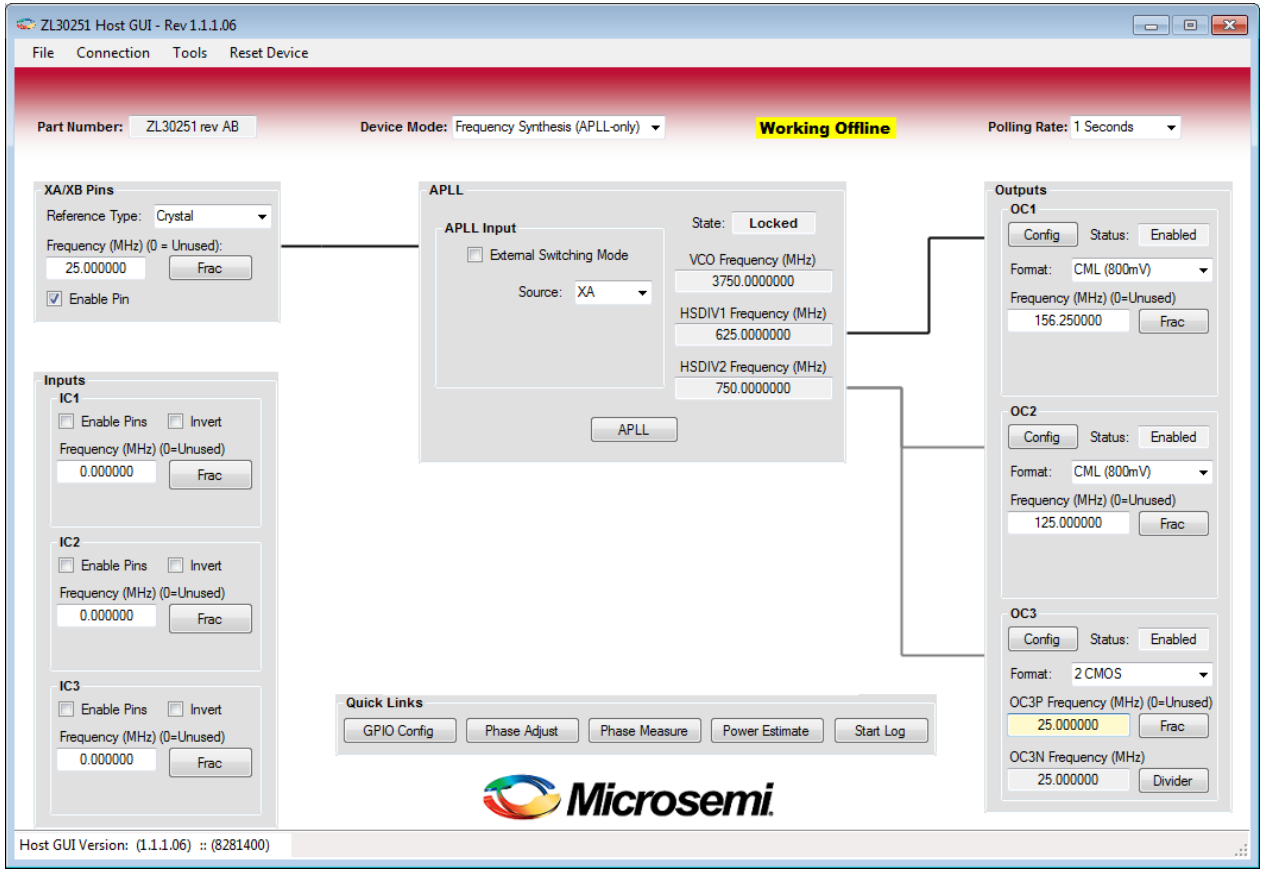
Configure the output clock frequencies and signal formats

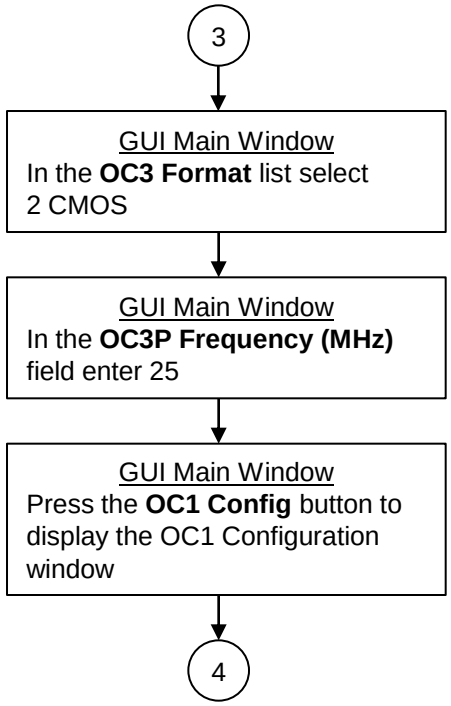




Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

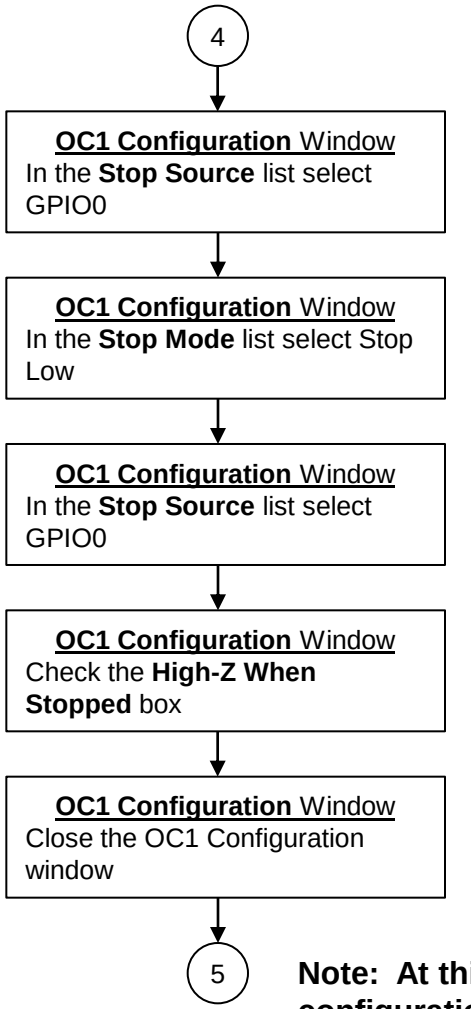
Configure the output clock frequencies and signal formats



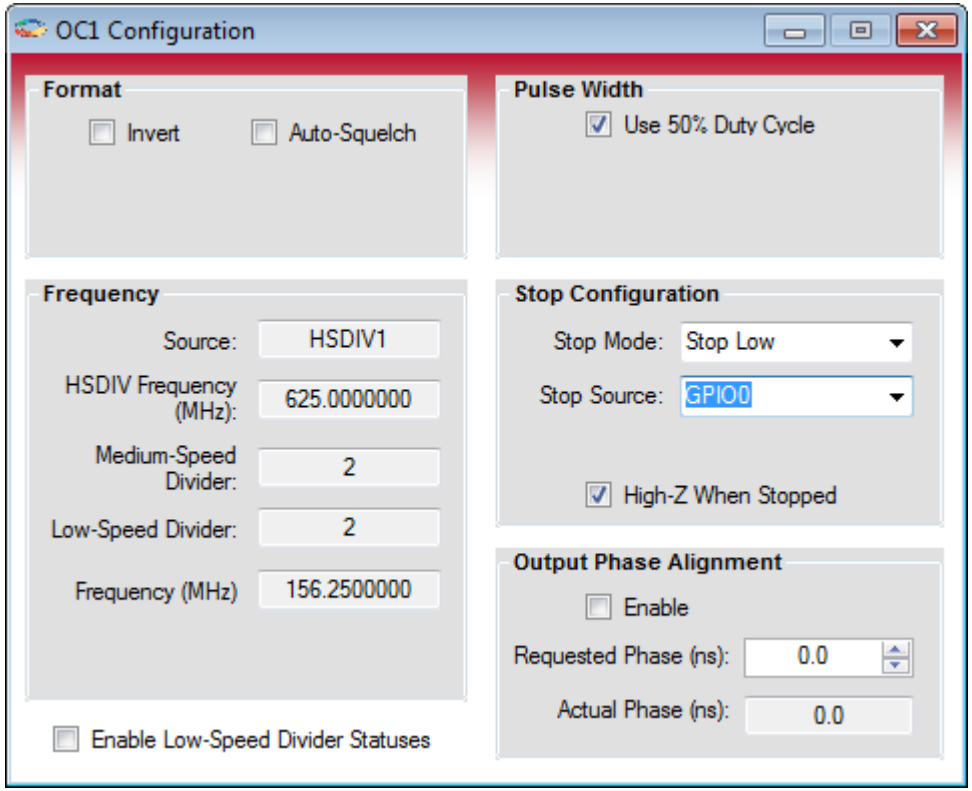


Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

Configure output clock OC1 enable/disable



Note: At this step device configuration is complete



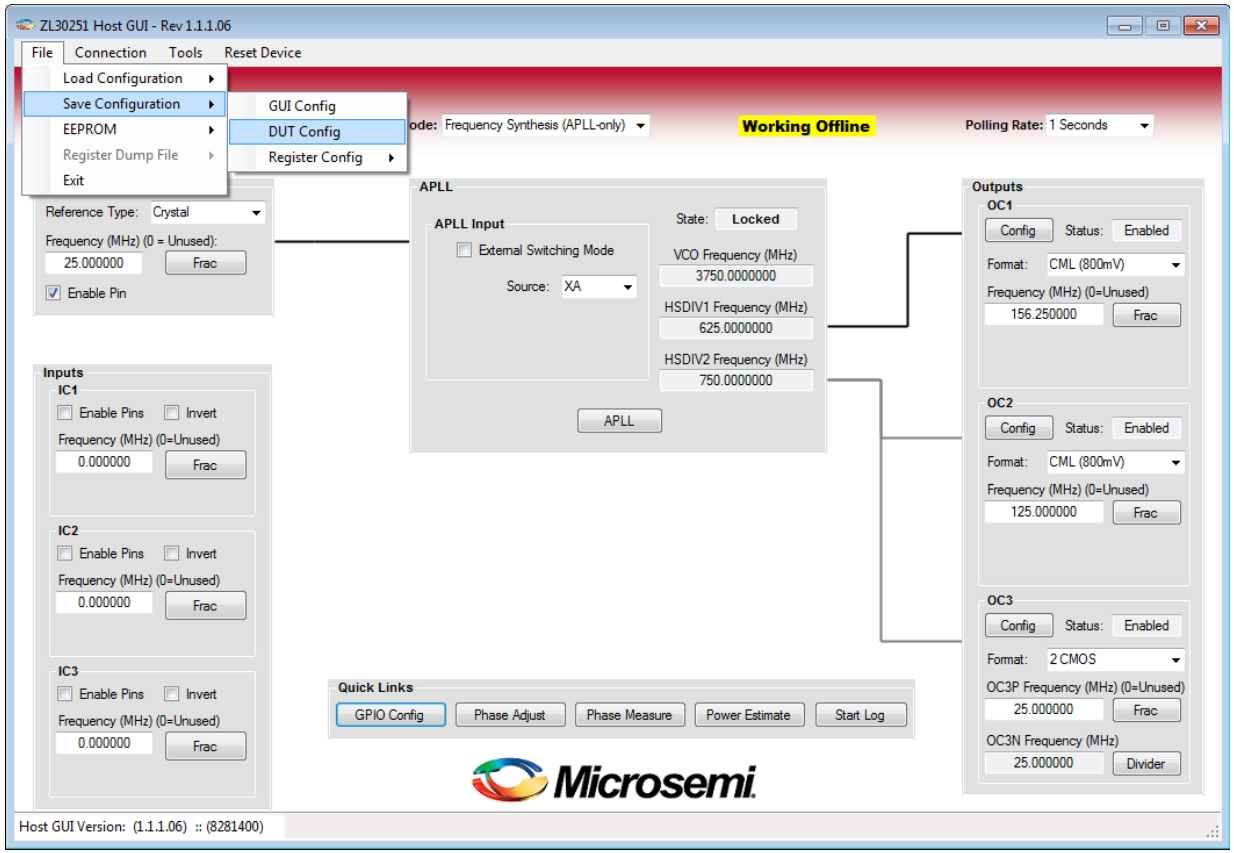
Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – Configuration File Creation

Create a device configuration (.mfg) file

5

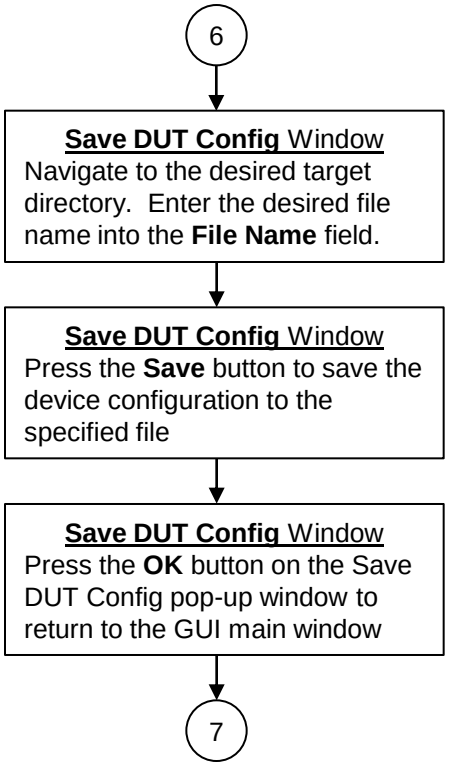
GUI Main Window
Open the **File -> Save Configuration -> DUT Config** window to save the current device configuration to a file

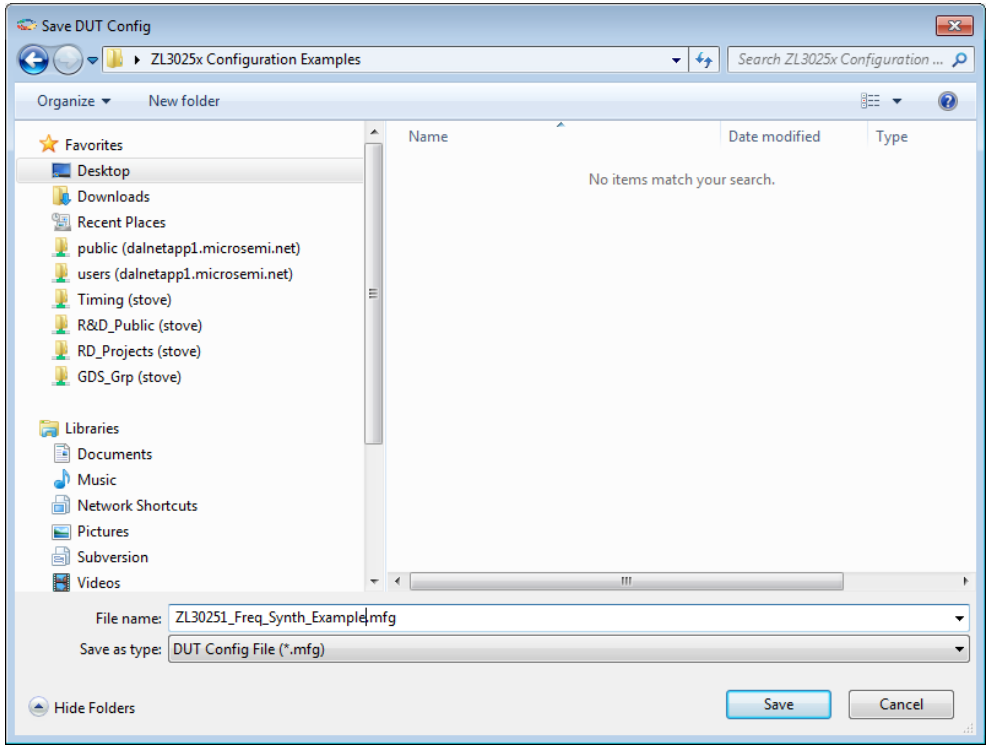
6

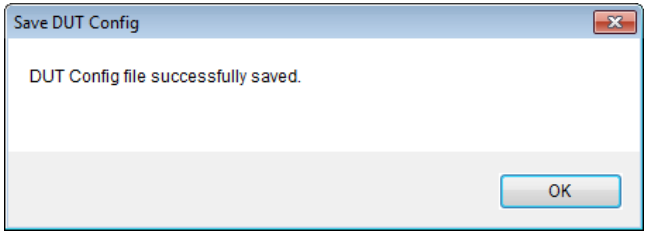


Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – Configuration File Creation

Create a device configuration (.mfg) file







Note: At this step the device configuration file has been created and saved

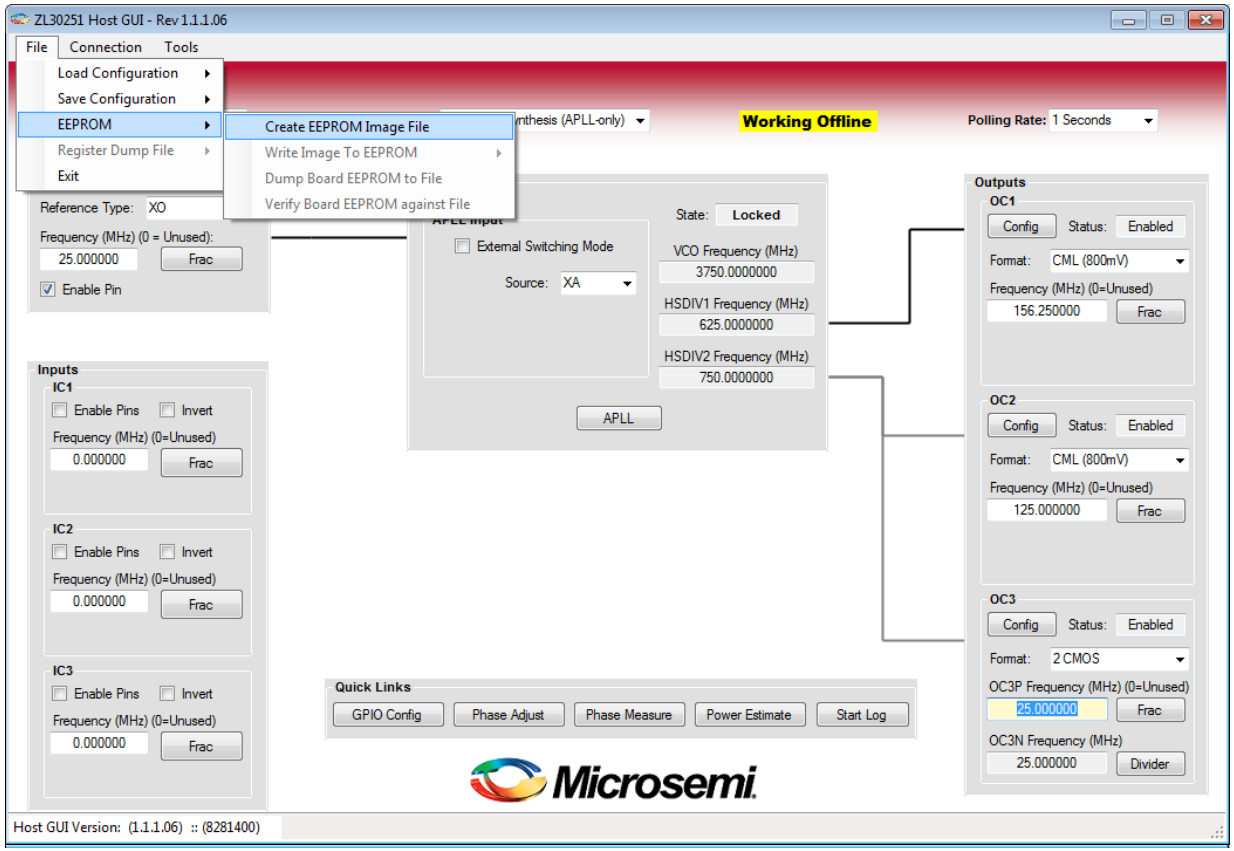
Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – EEPROM Image File Creation

Create an EEPROM image file

7

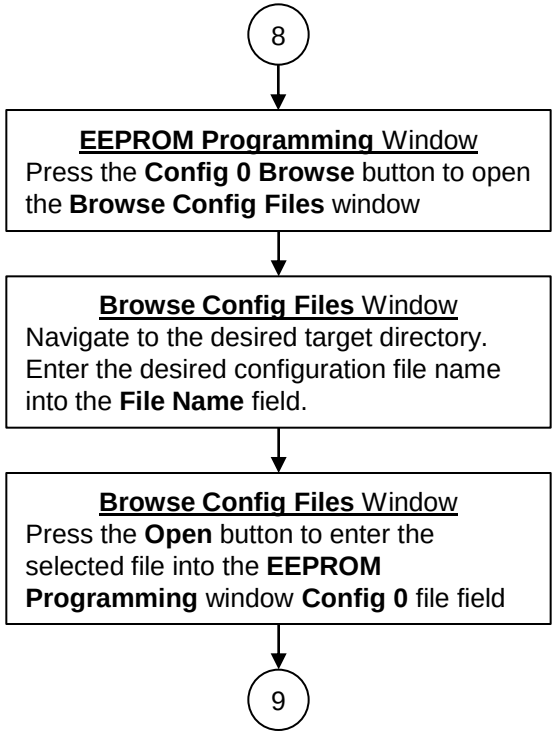
GUI Main Window
Open the **EEPROM -> Create EEPROM Image File** window to create an EEPROM image file from the saved device configuration file

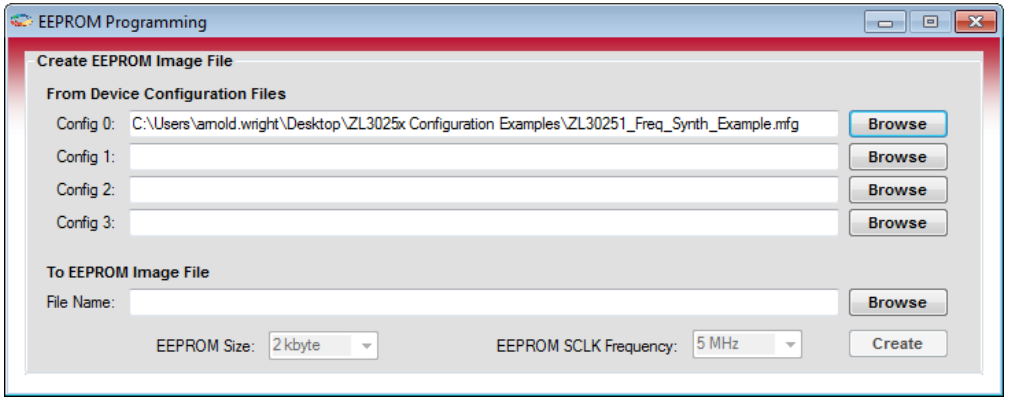
8

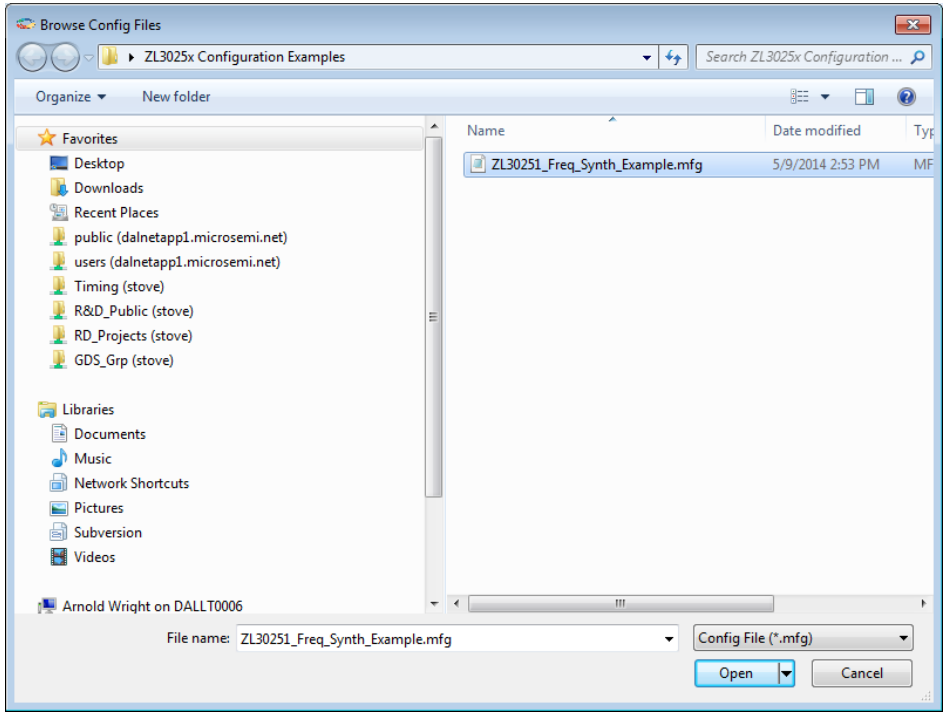


Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – EEPROM Image File Creation

Create an EEPROM image file

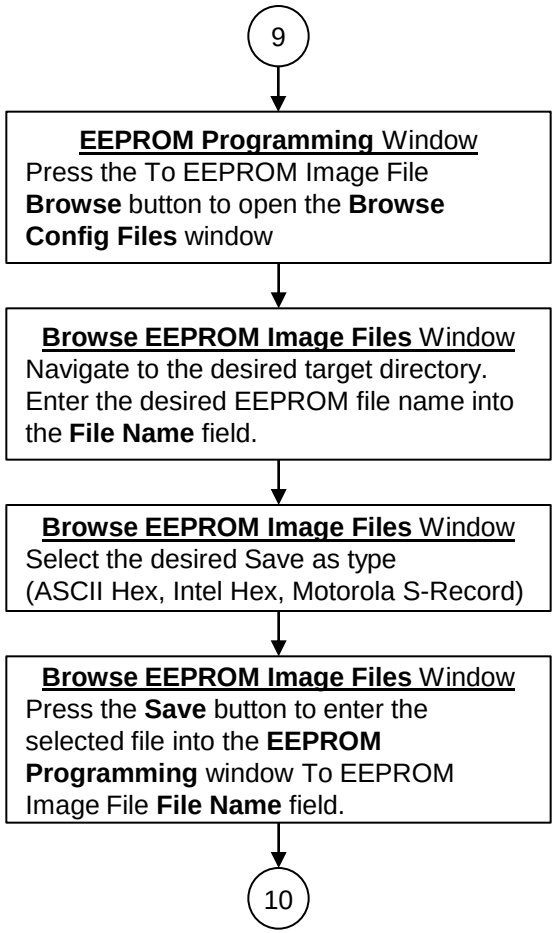


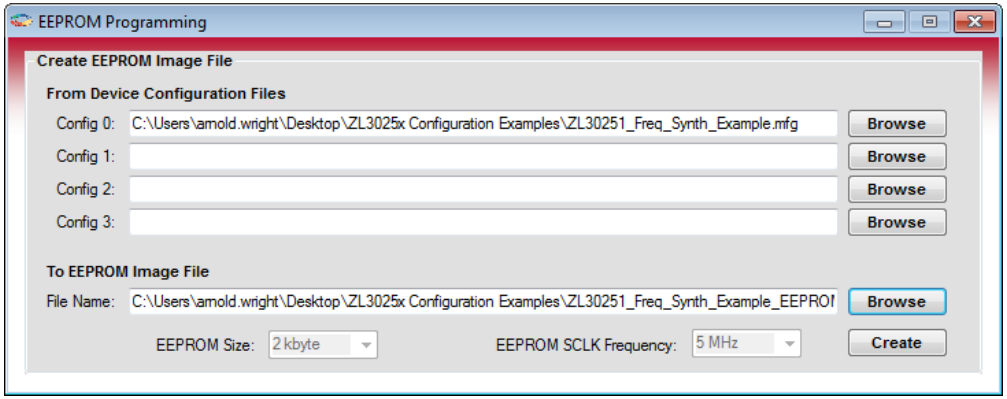


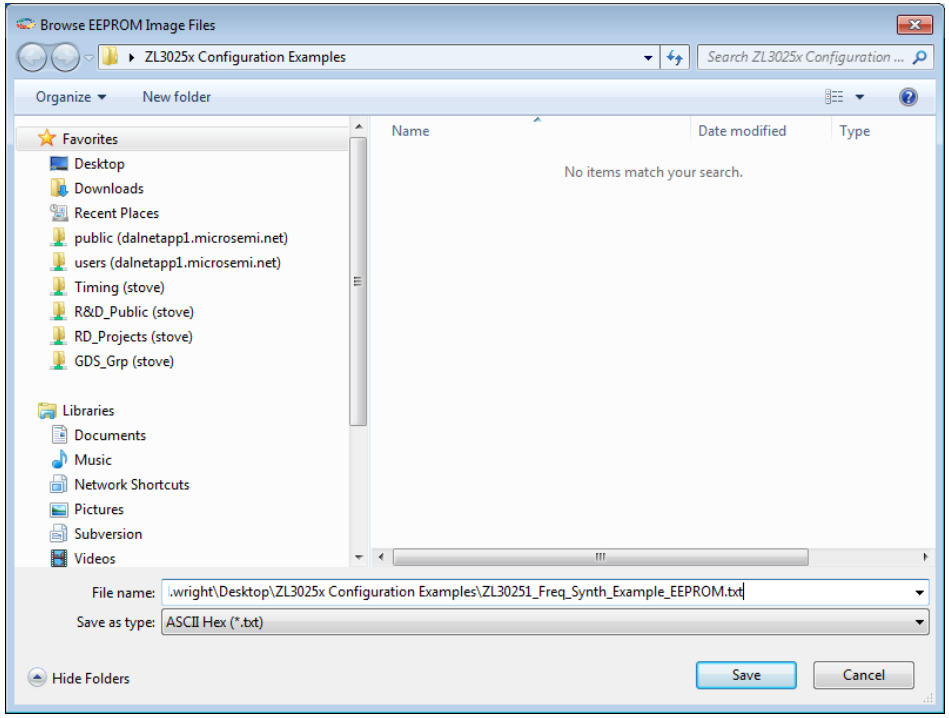


Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – EEPROM Image File Creation

Create an EEPROM image file

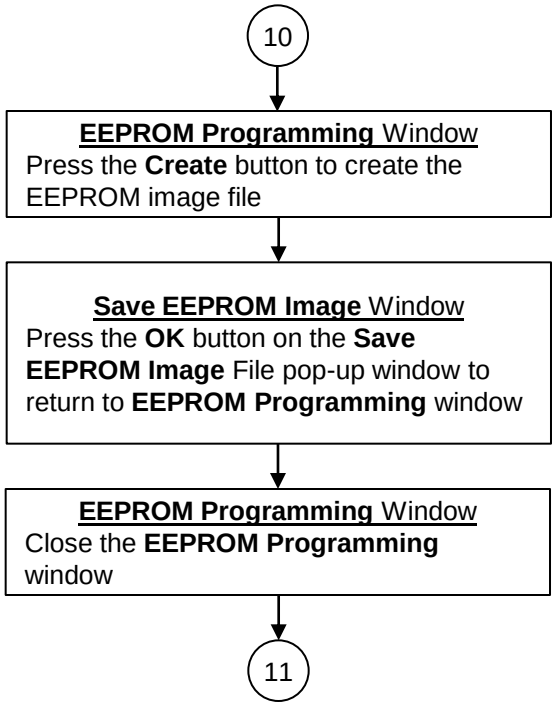


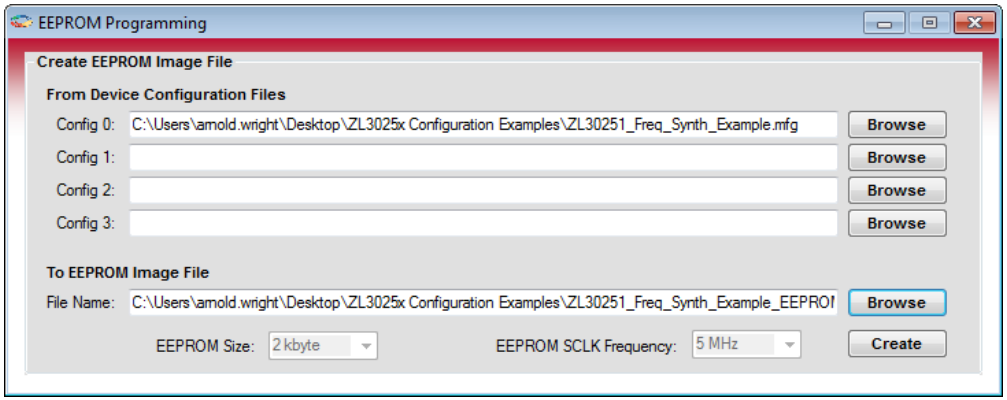


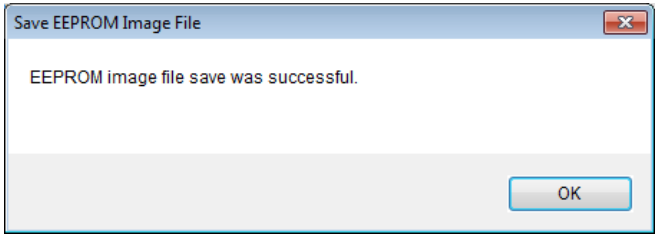


Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – EEPROM Image File Creation

Create an EEPROM image file



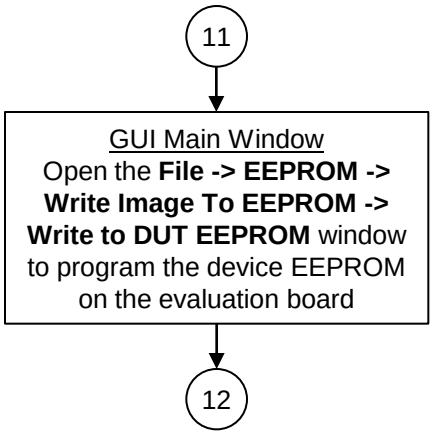


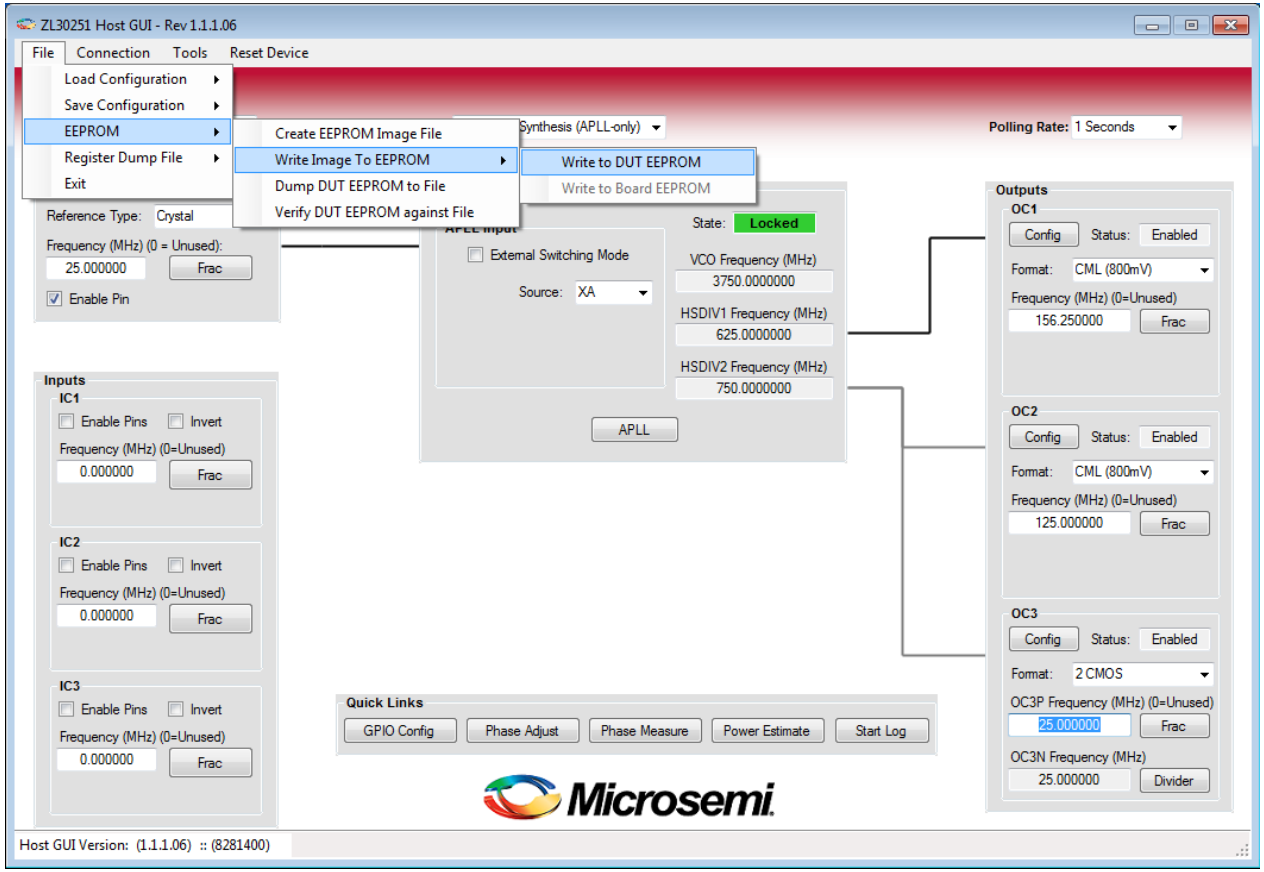


Note: At this step the EEPROM Image file has been created and saved

Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – EEPROM Programming

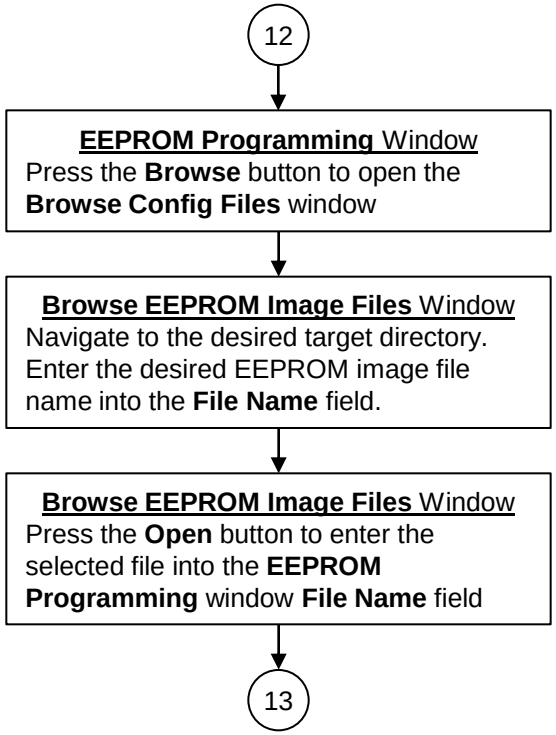
Program the Evaluation Board Device EEPROM
(GUI must be connected to the board)

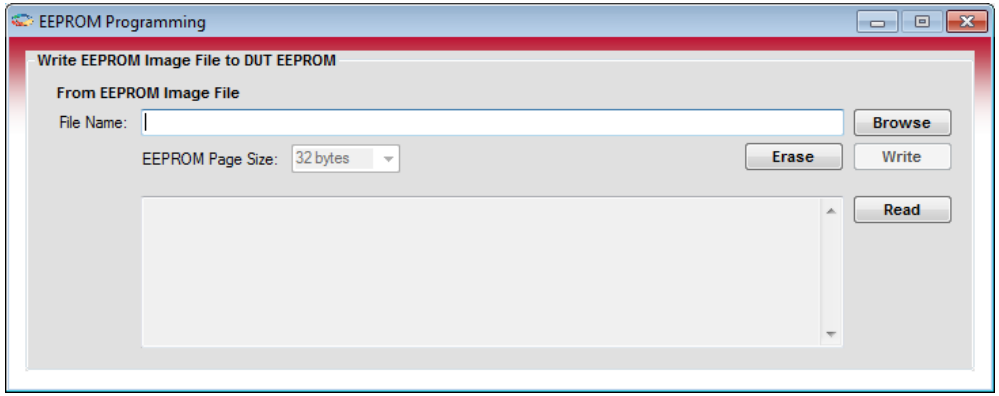


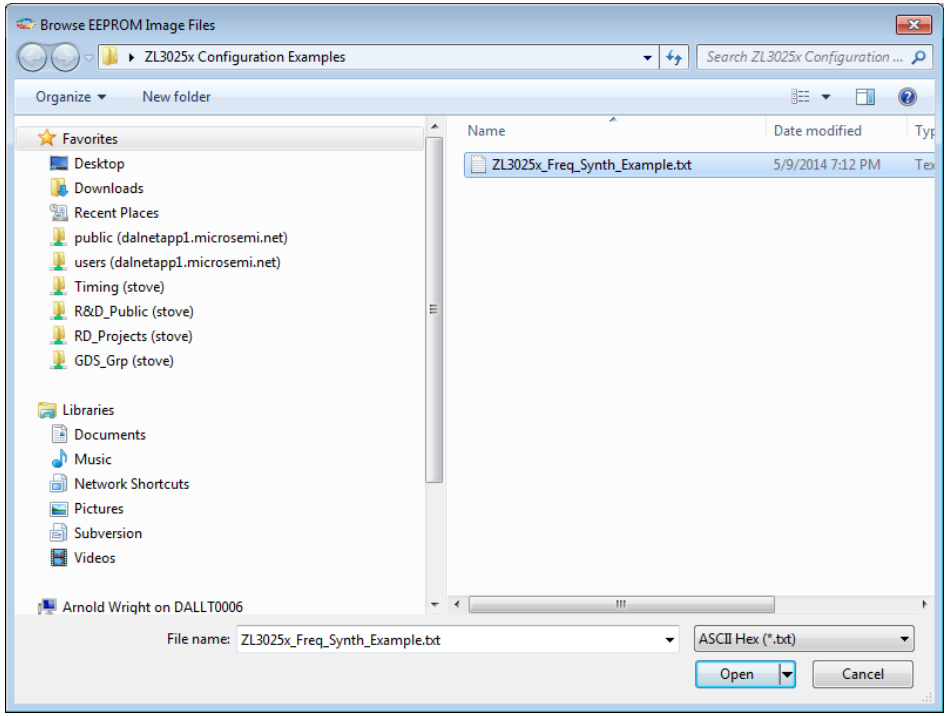


Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – EEPROM Programming

Program the Evaluation Board Device EEPROM (GUI must be connected to the board)

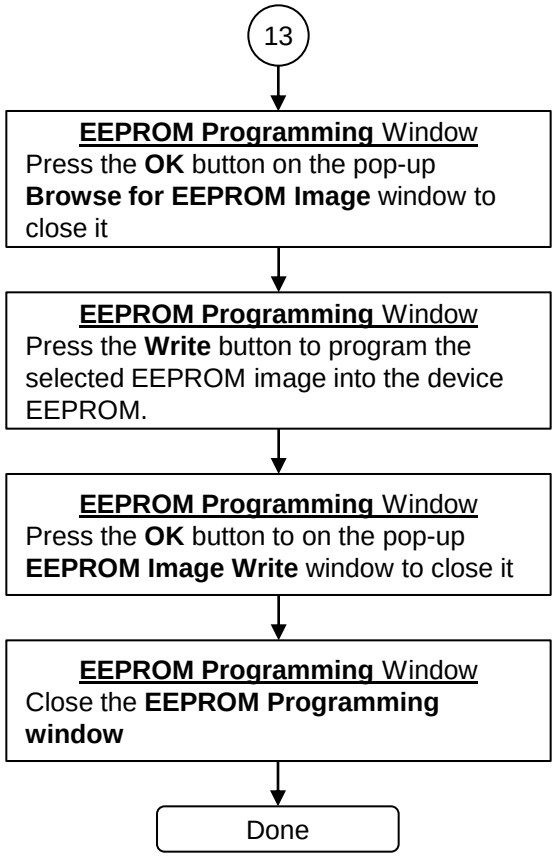




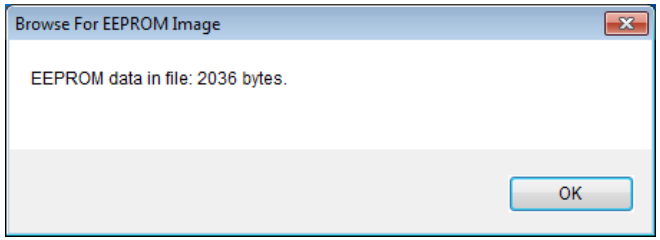


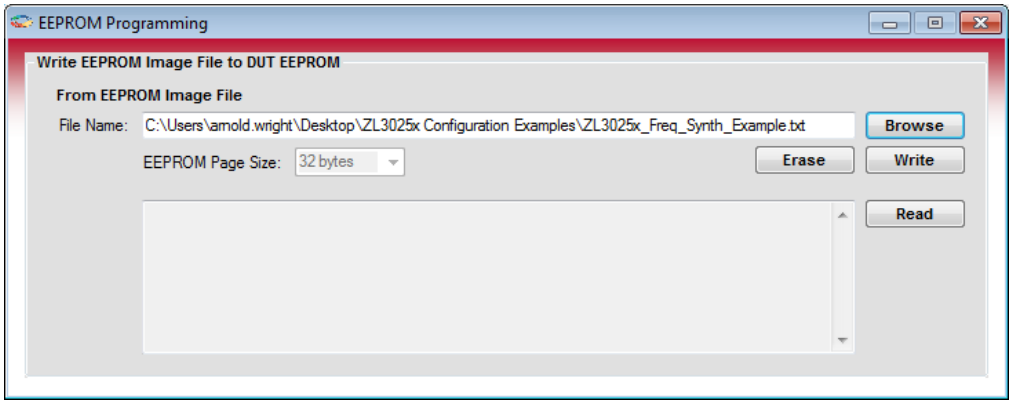
Creating a Frequency Synthesis Mode Device Configuration Step-by-Step Flow Chart – EEPROM Programming

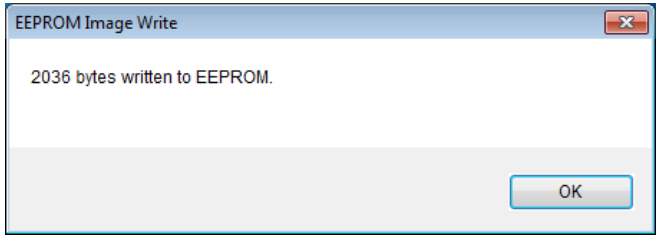
Program the Evaluation Board Device EEPROM (GUI must be connected to the board)



Note: At this step the device EEPROM has been programmed







Creating a Jitter Attenuation Mode Device Configuration

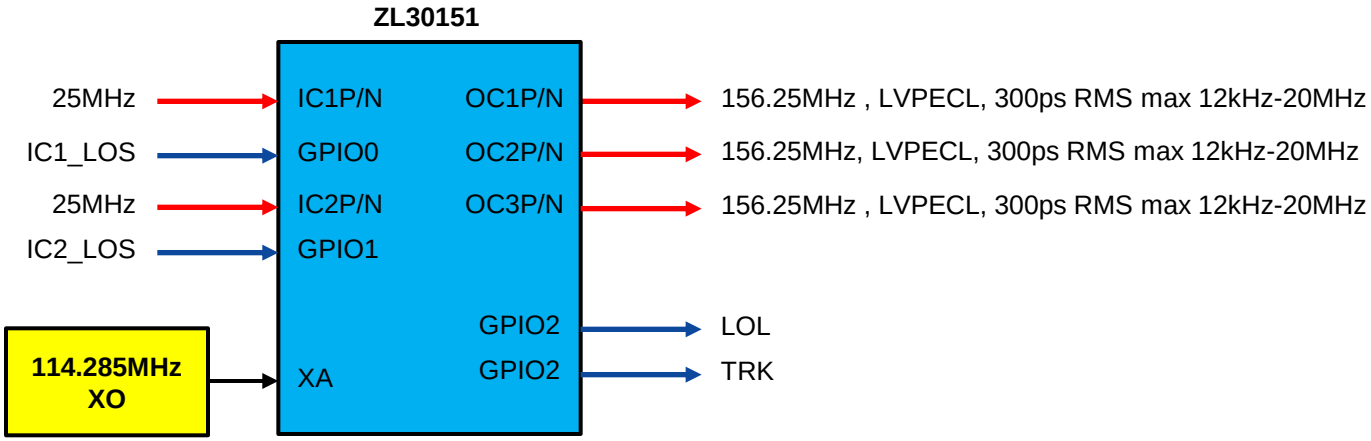
Creating a Jitter Attenuation Mode Device Configuration Overview

- Key application requirements
  - Self-configuration at startup
  - Input clocks require fast disqualification, LOS error status is available for use
  - Jitter requirement on all output clocks is 300ps RMS max 12kHz-20MHz
  - Input clock switching must be non-revertive
  - Output-to-output clock edge alignment is required
  - Hardware DPLL locked / not locked status

- Key implementation details
  - Recommended oscillator list VCC1-1535 114.25MHz XO used to meet jitter requirements
  - EEPROM configuration stored in slot 0
    - ZL30151 pins GPIO1/AC1 and GPIO1/AC0 must be low at RSTN de-assertion for device to load configuration from EEPROM slot 0
  - GPIO0 and GPIO1 used to input LOS error signals for fast input clock disqualification
    - LOS control inputs must be 0 at ZL30151 RSTN pin de-assertion for device load configuration from EEPROM slot 0
  - Input clock frequency monitors configured for fast invalidation
  - 800mV CML mode used to provide LVPECL compatible output clock signal levels
  - GPIO2 = DPLL LOL status (DSRR1.LOL); GPIO3 = DPLL tracking status (DSRR1.TRK)
    - DPLL Locked = !GPIO2 & GPIO3
    - GPIO3/TEST must be low at ZL30151 RSTN pin de-assertion for proper device operation

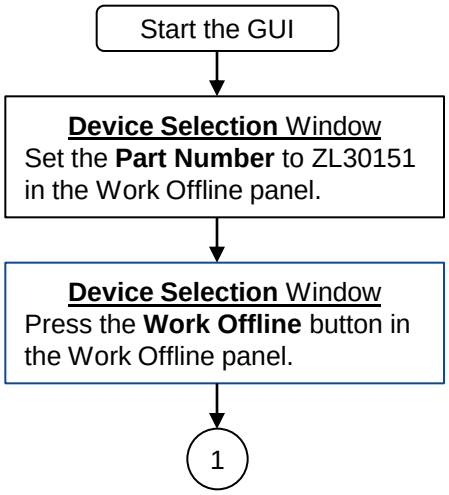
Creating a Jitter Attenuation Mode Device Configuration Overview

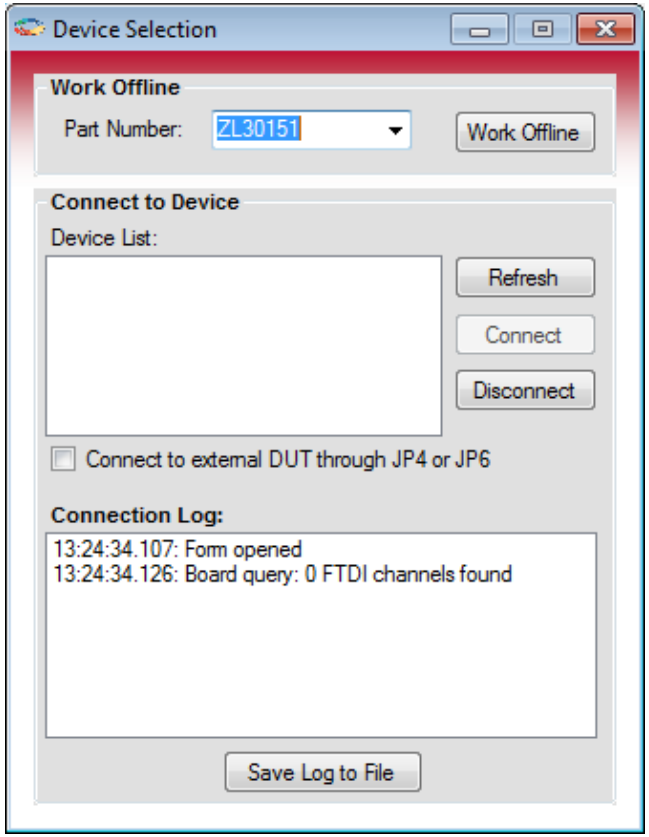
- ZL30151 Block Diagram



Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

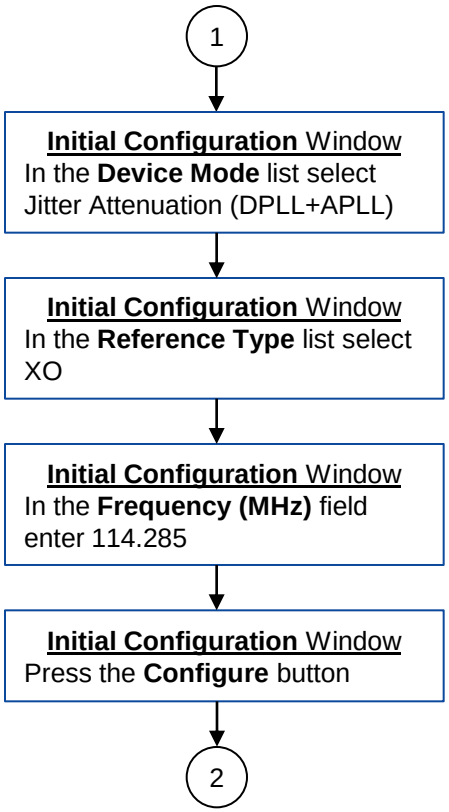
Select the device

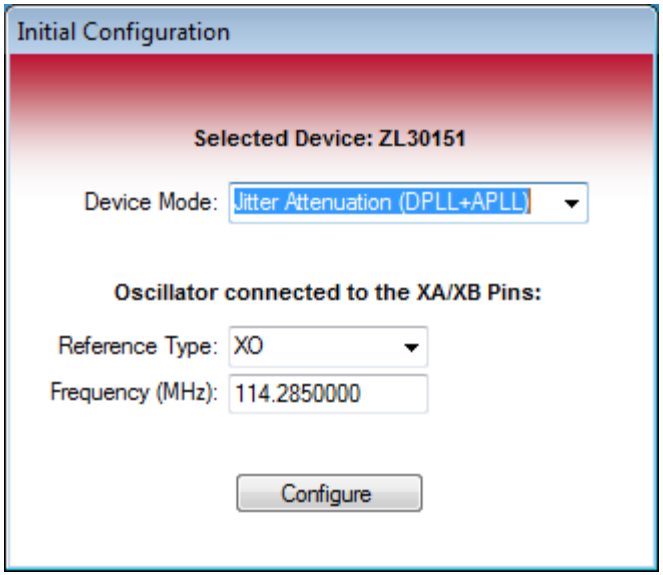




Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

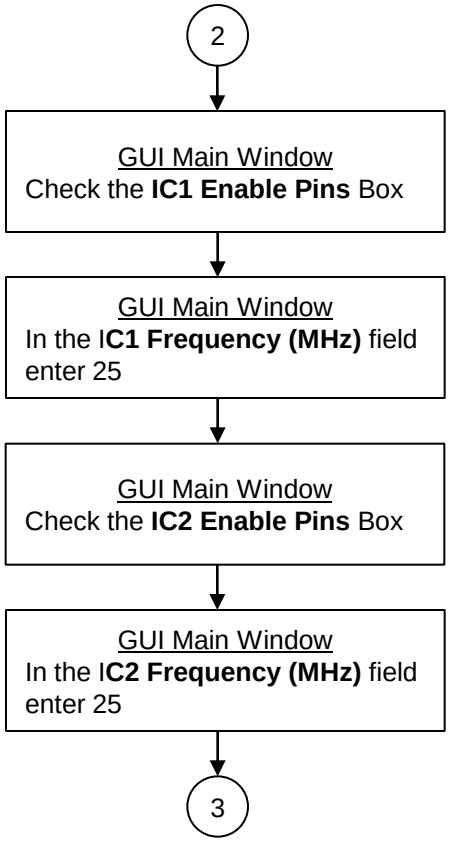
Configure the reference type and frequency

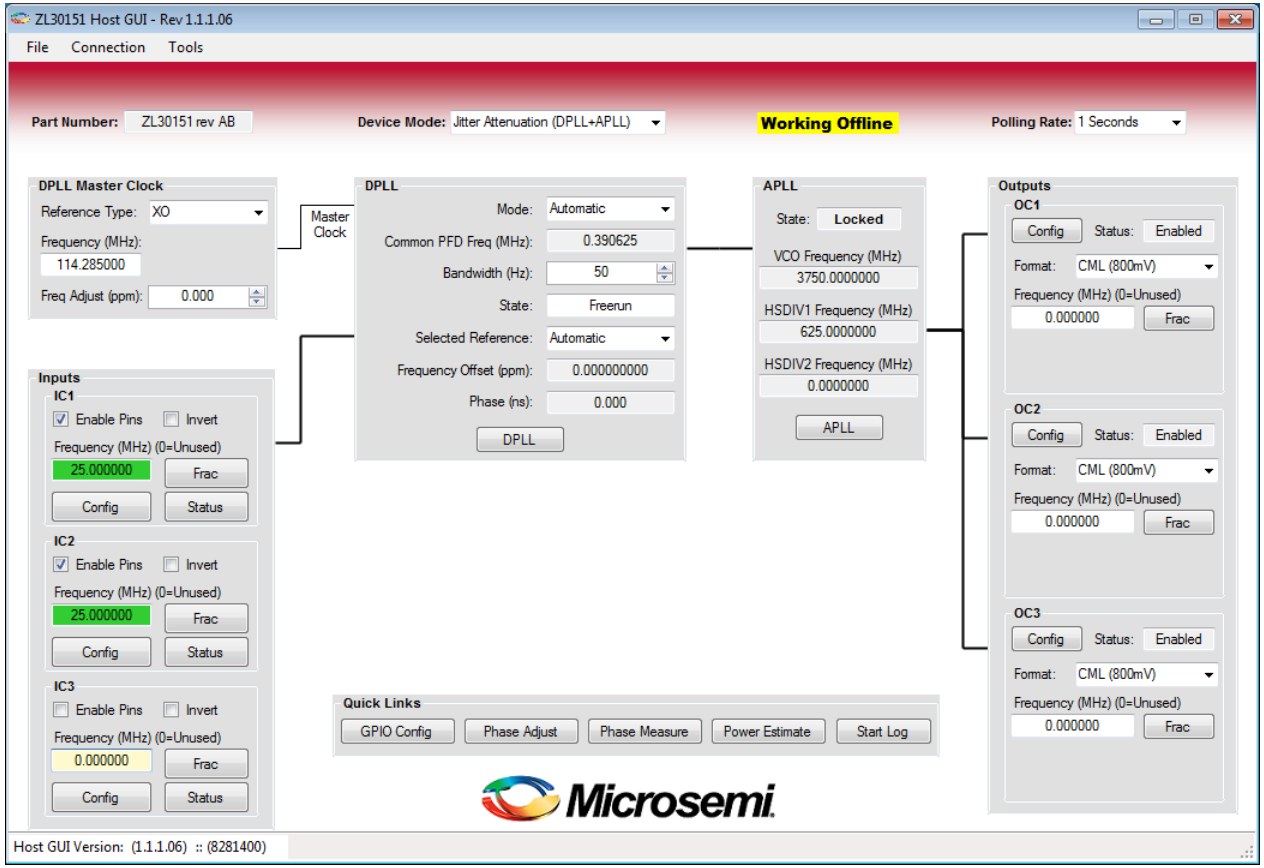




Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

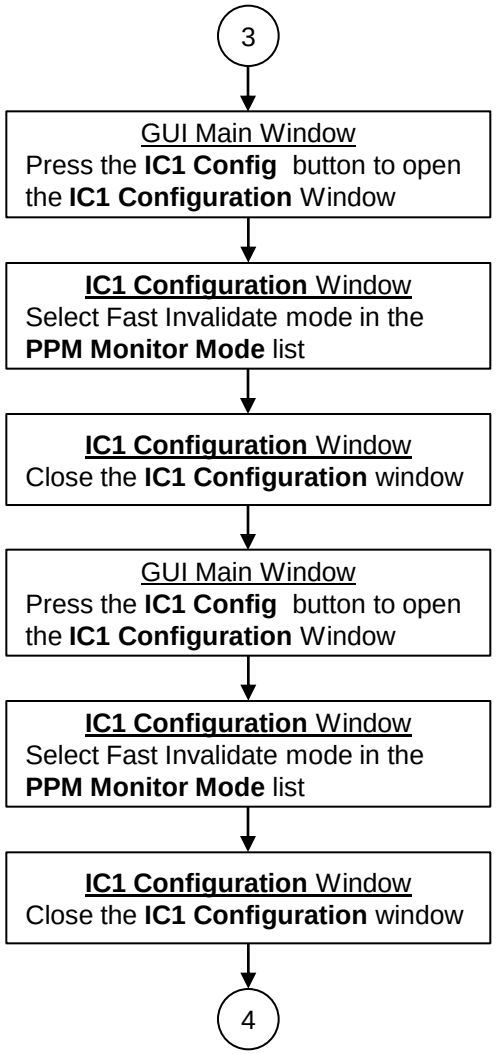
Configure the input clock frequencies

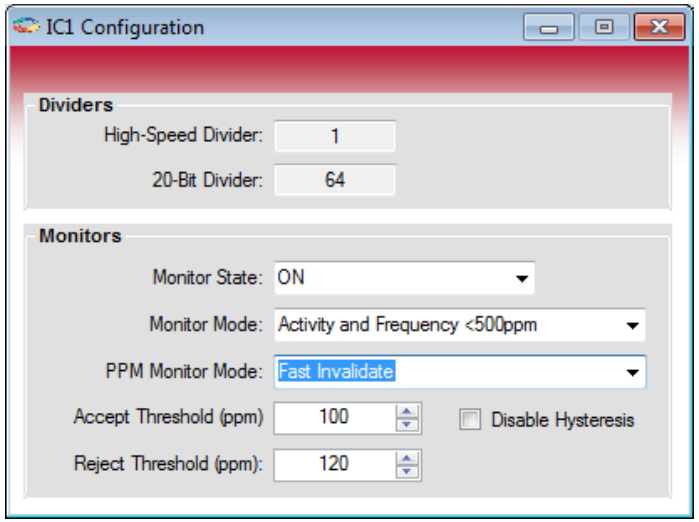


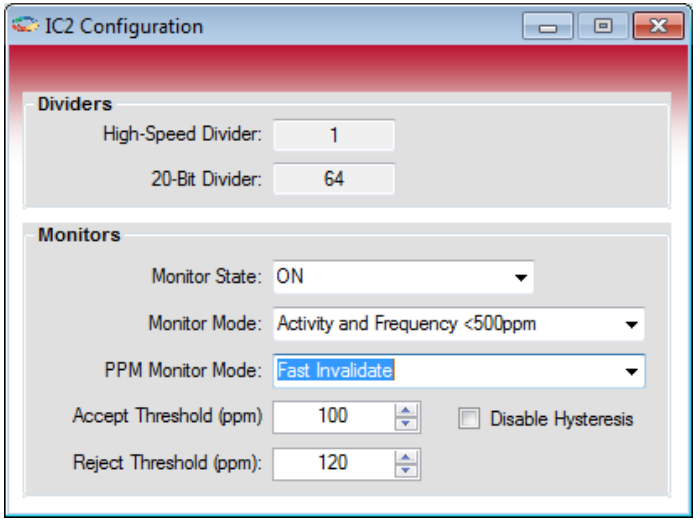


Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

Configure IC1 and IC2 monitors

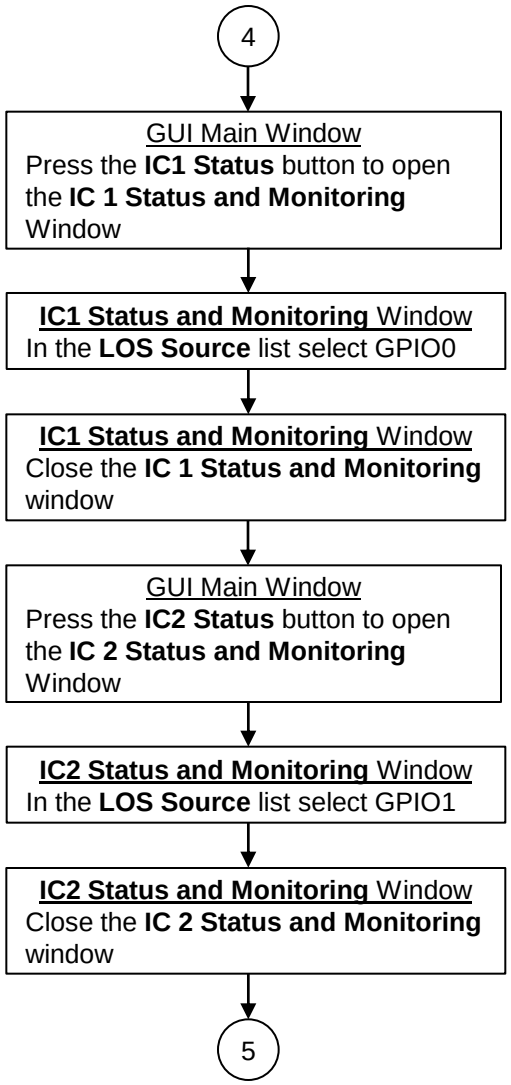


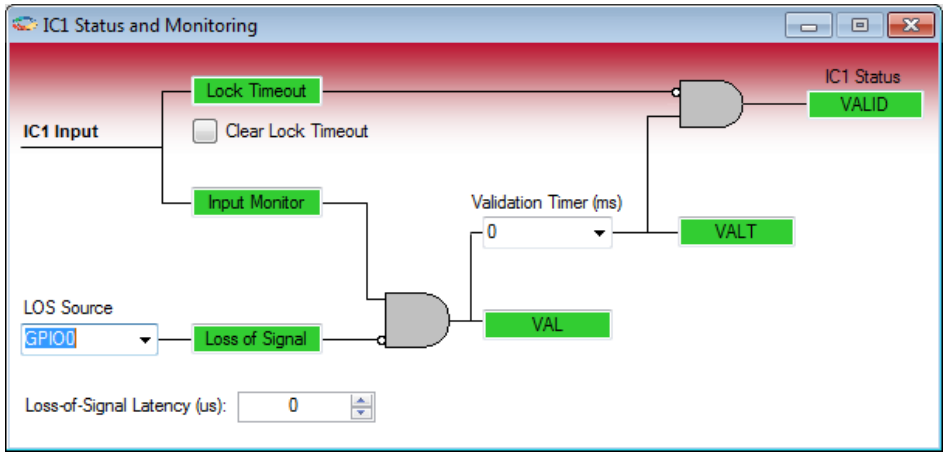


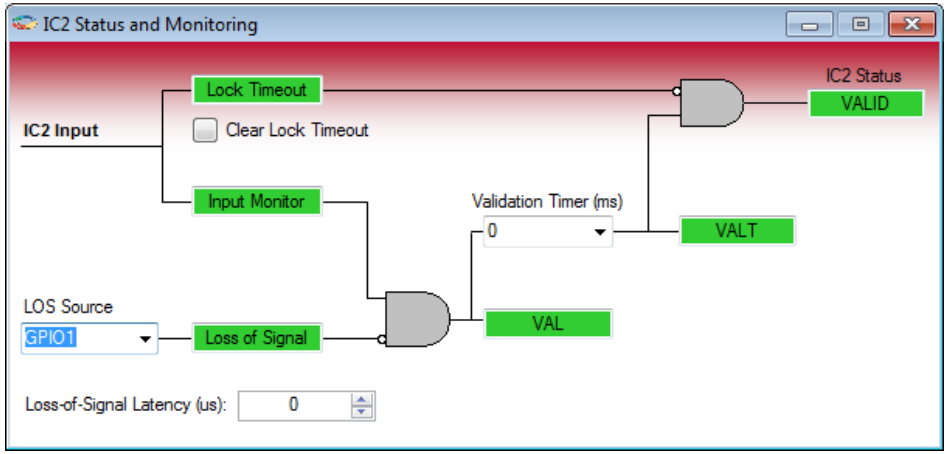


Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

Configure IC1 and IC2 LOS source

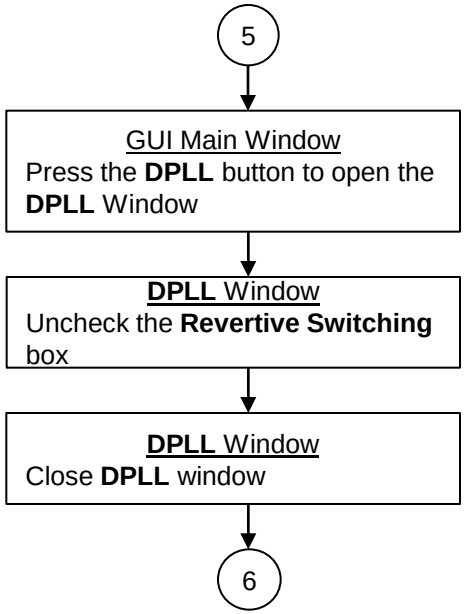


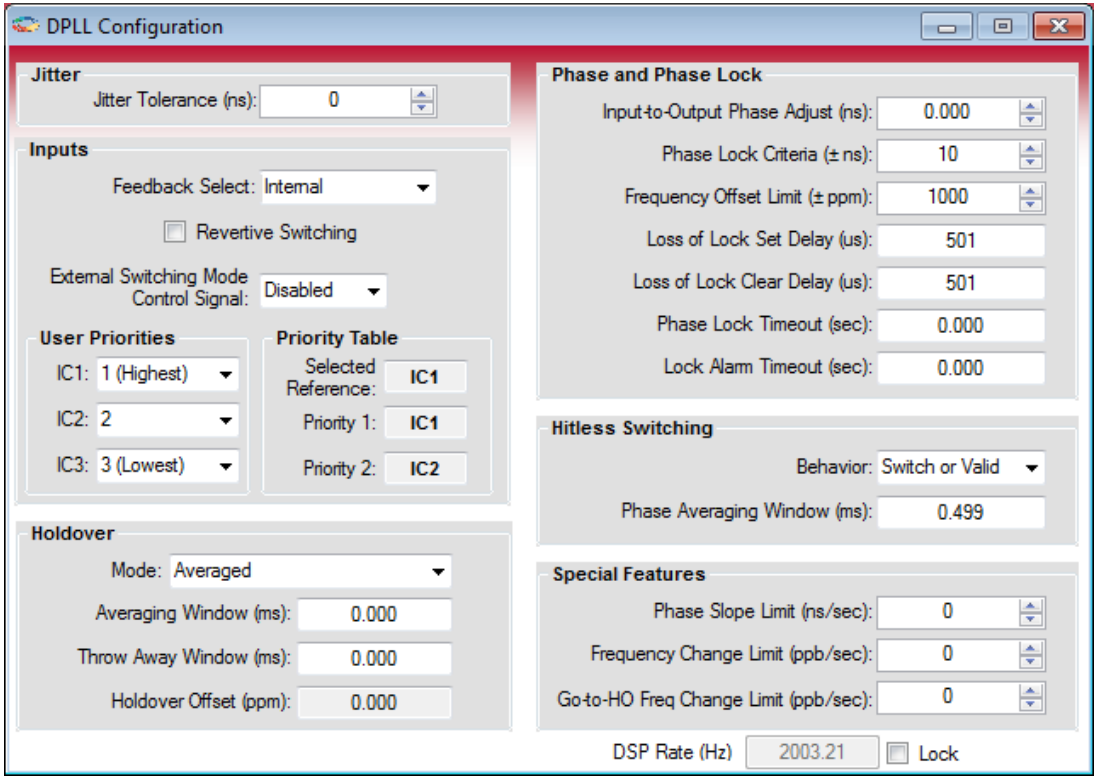




Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

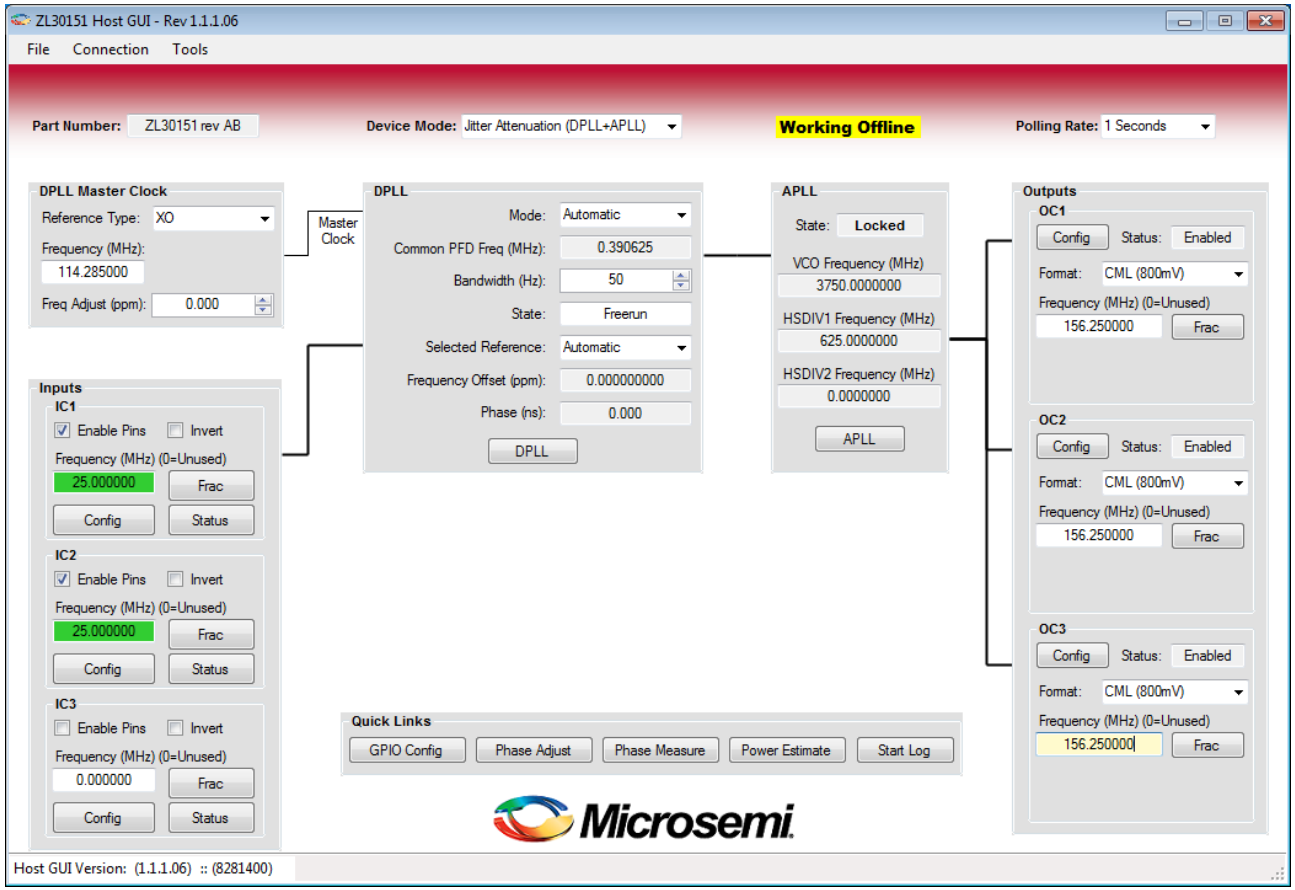
Configure the DPLL

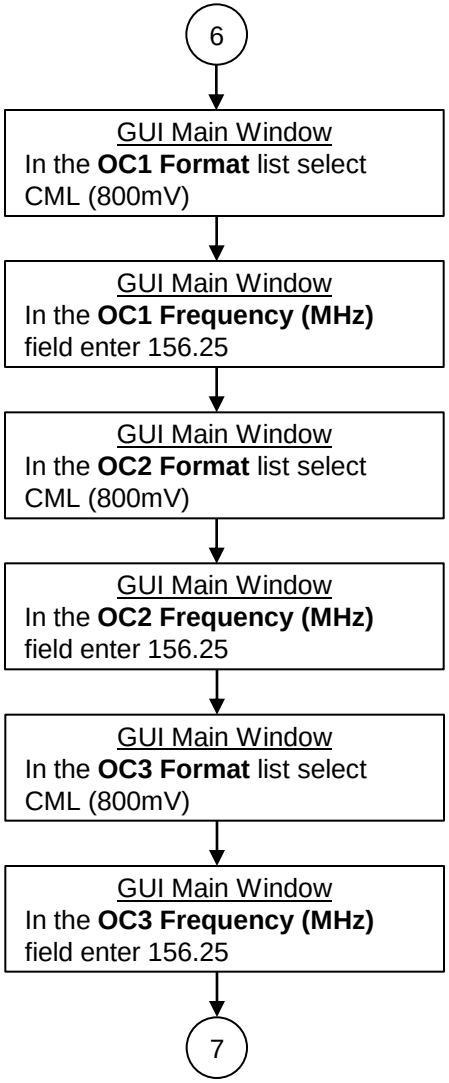




Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

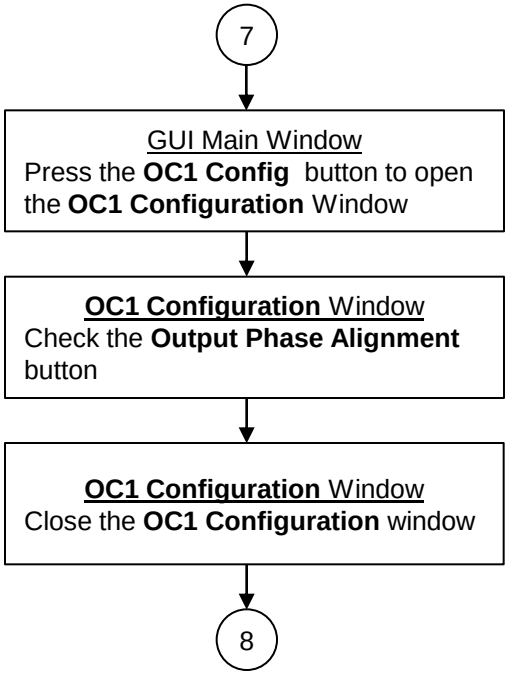
Configure output clock frequencies and signal formats

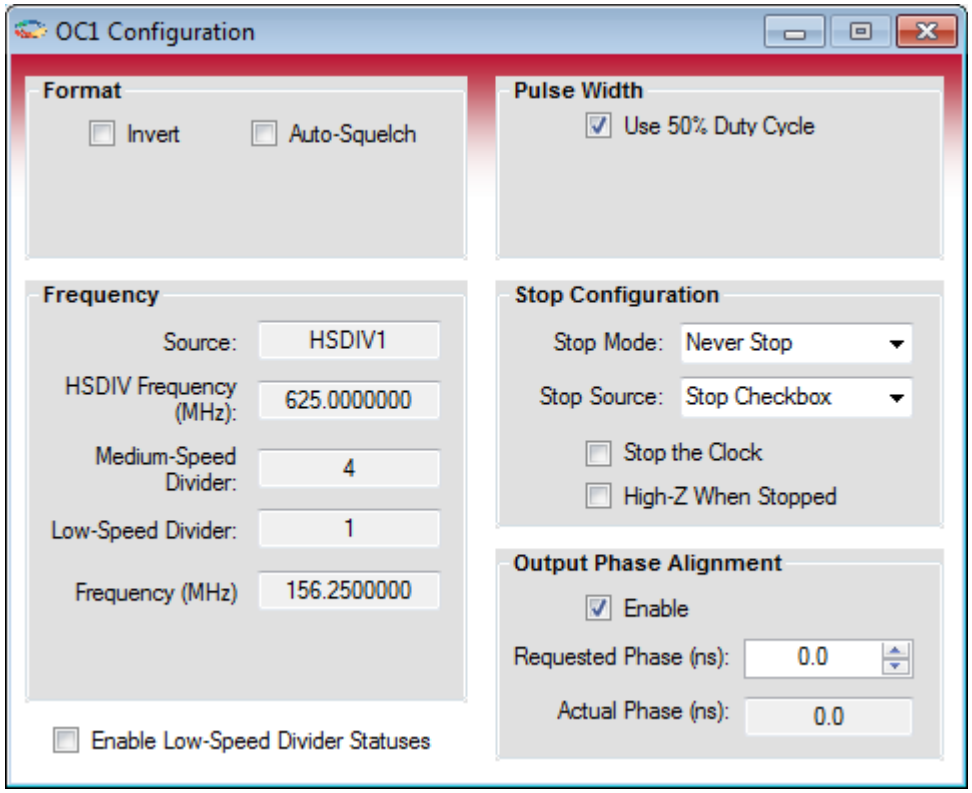




Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

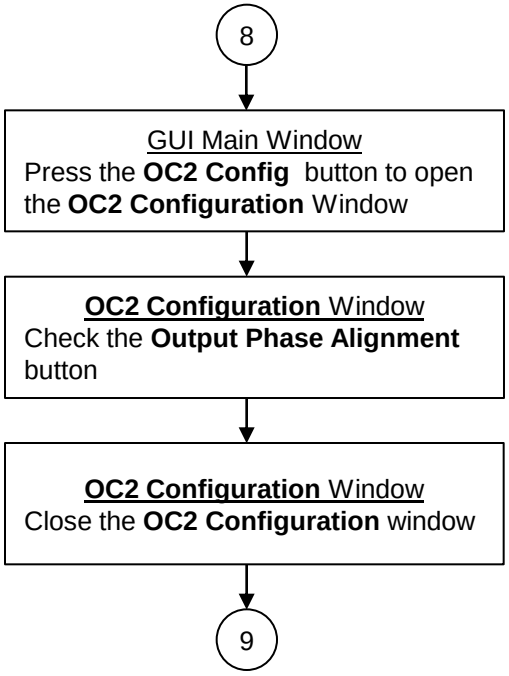
Configure output clock OC1 alignment

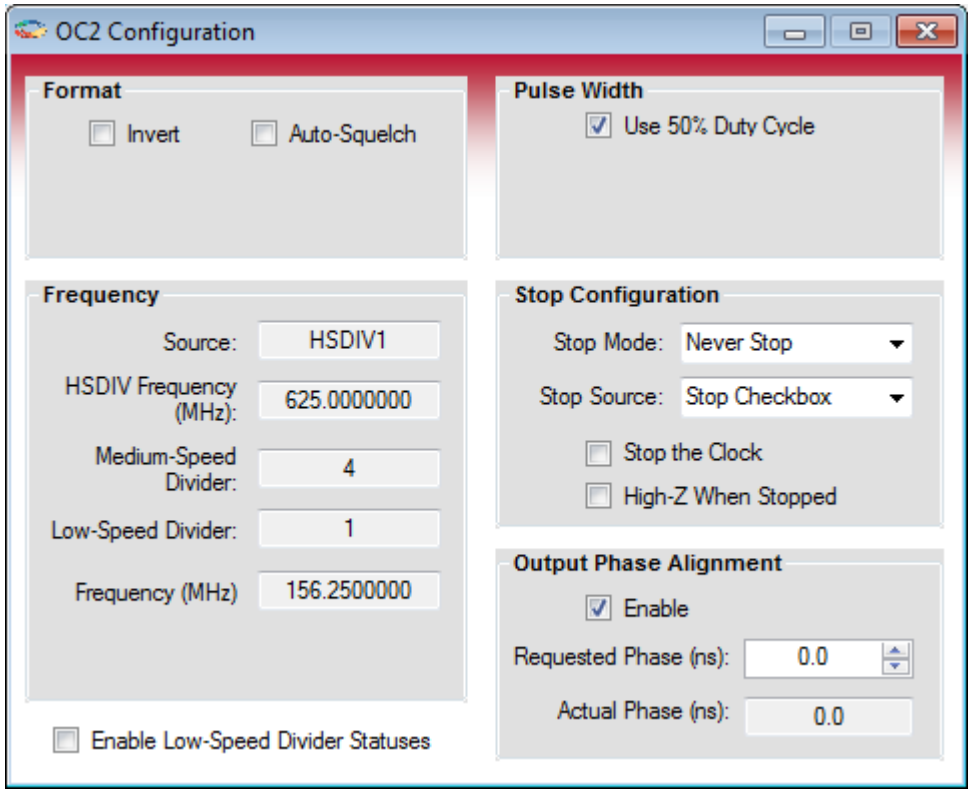




Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

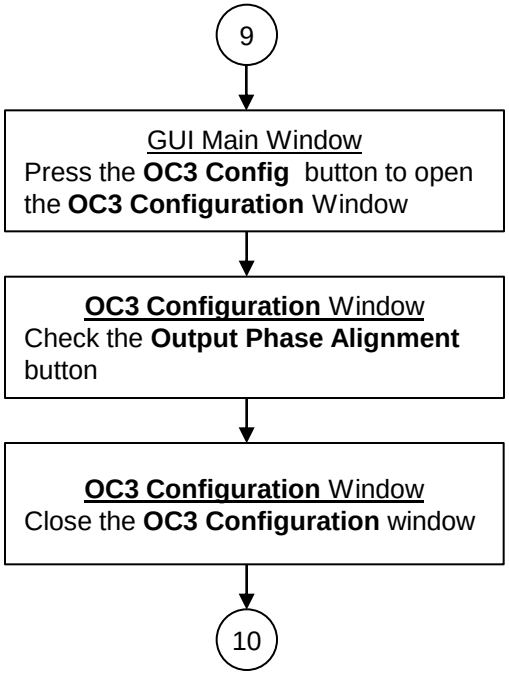
Configure output clock OC2 alignment

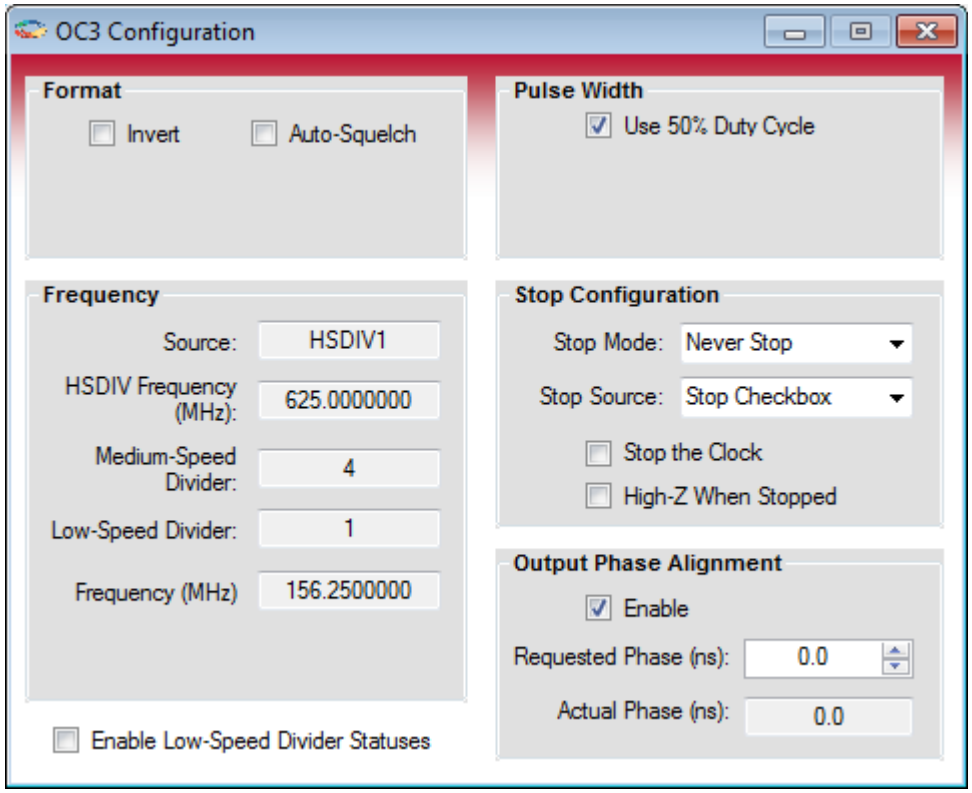




Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

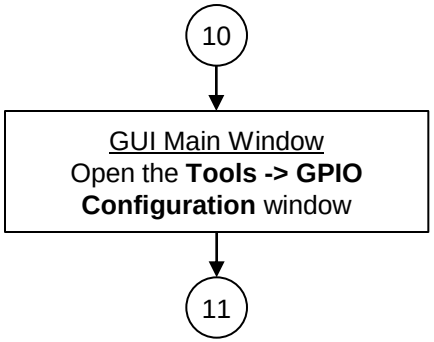
Configure output clock OC3 alignment

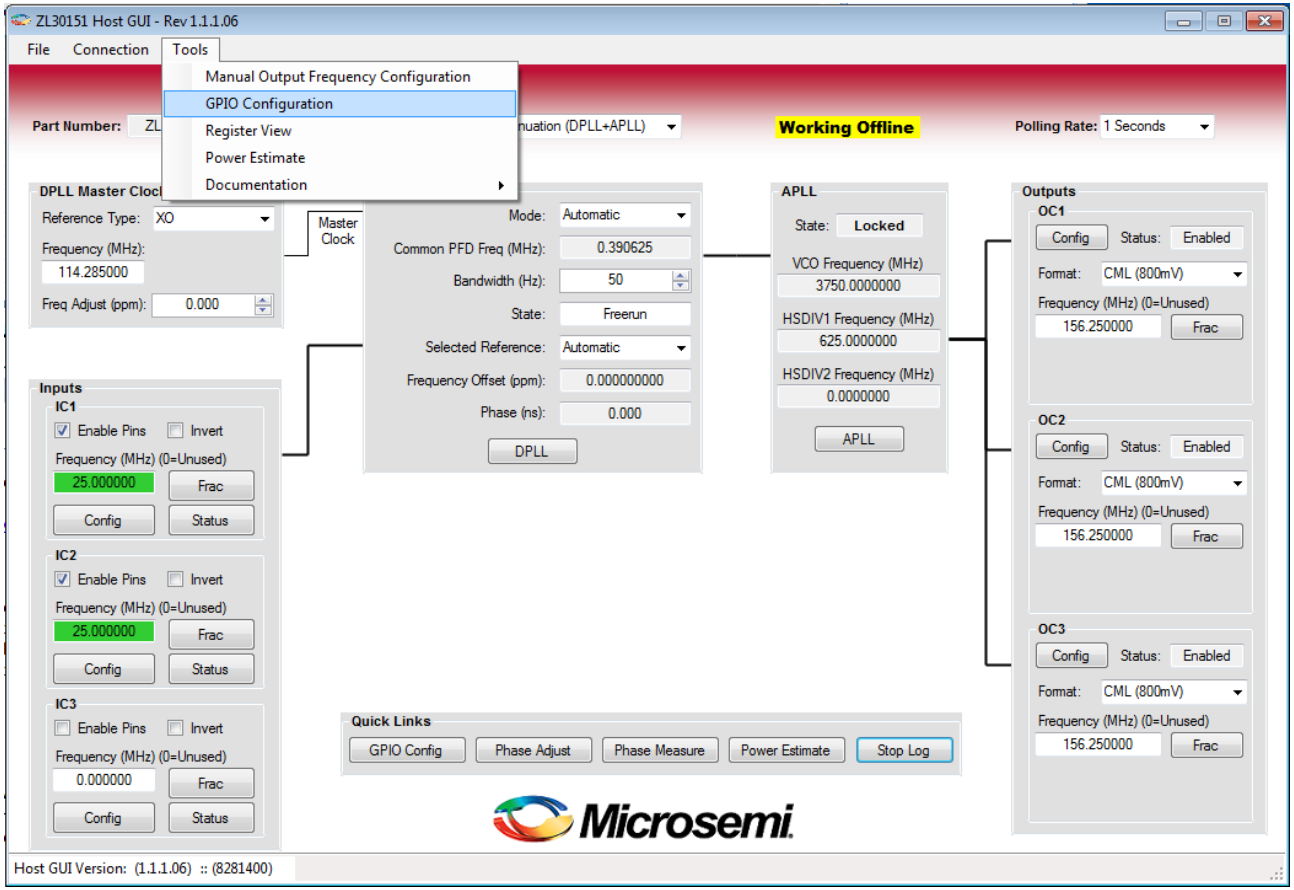




Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

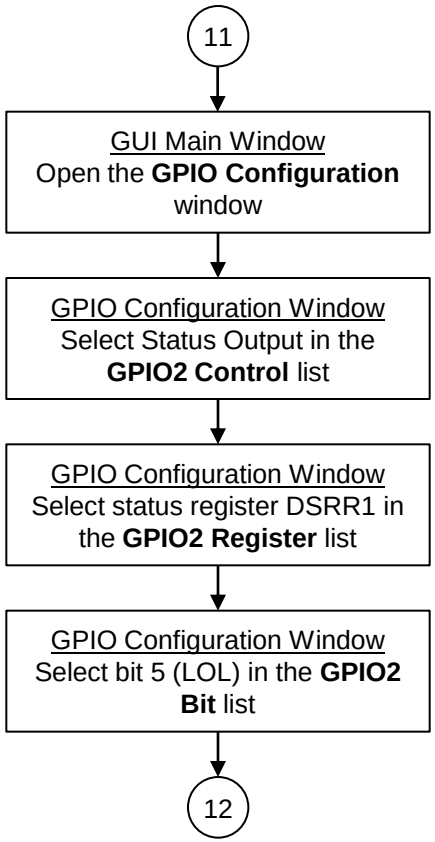
Configure GPIO lock status output

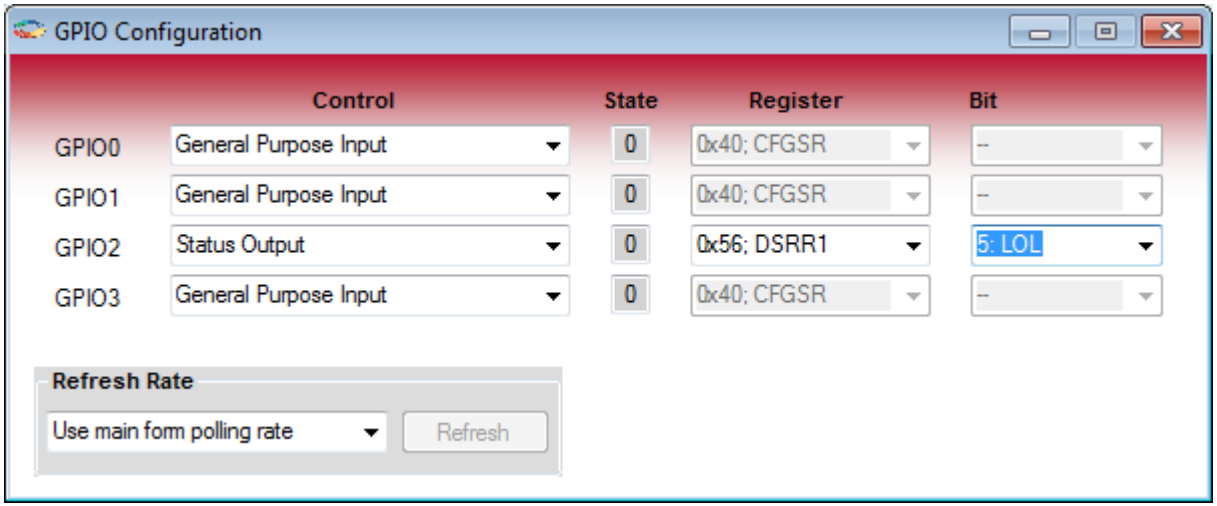




Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

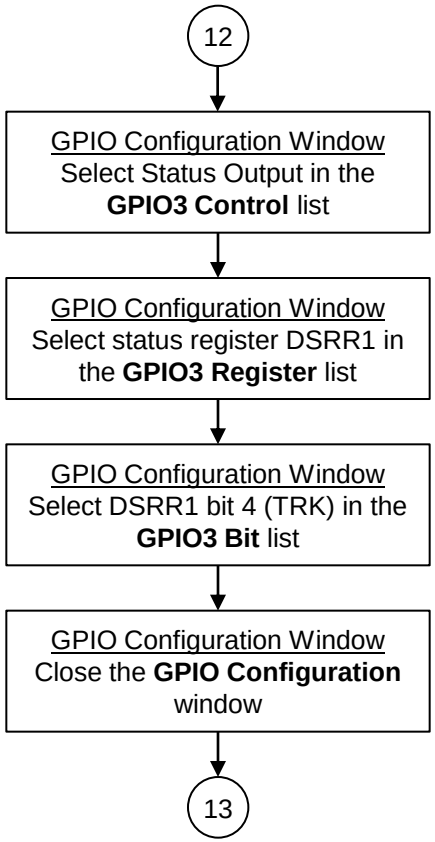
Configure GPIO2 LOL status output

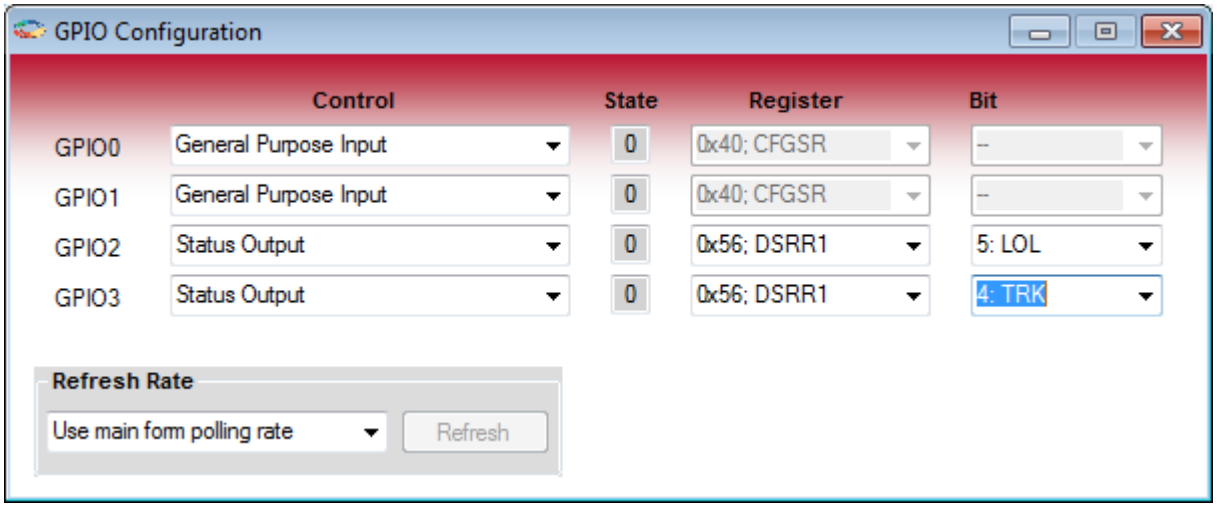




Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Device Configuration

Configure GPIO3 TRK status output





Note: At this step device configuration is complete

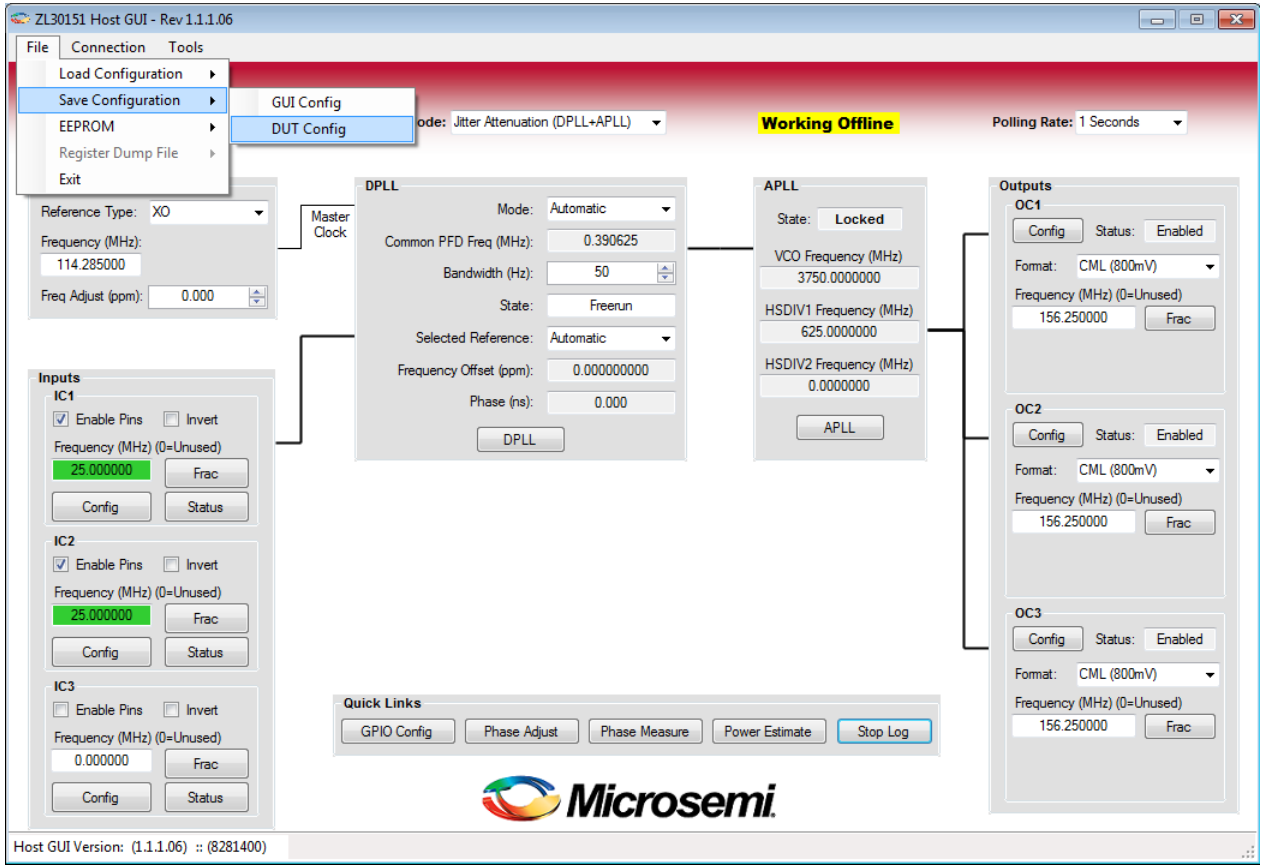
Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Configuration File Creation

Create a device configuration (.mfg) file

13

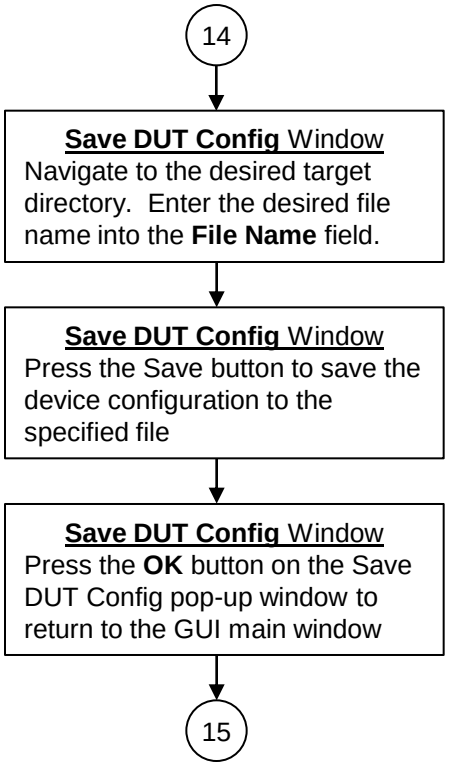
GUI Main Window
Open the **File -> Save Configuration -> DUT Config** window to save the current device configuration to a file

14

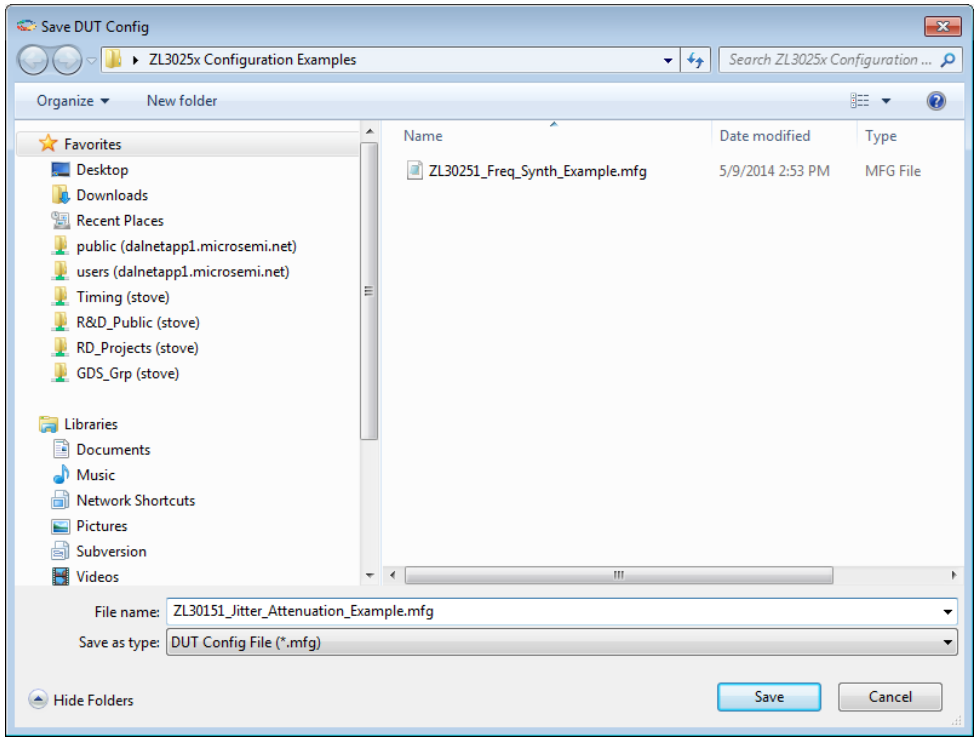


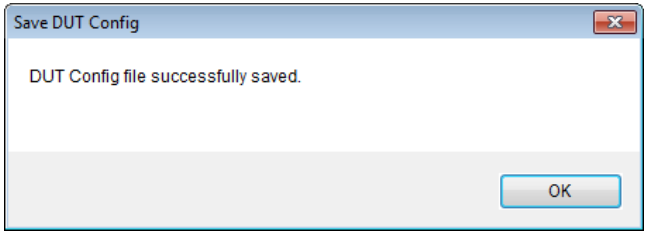
Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – Configuration File Creation

Create a device configuration (.mfg) file



Note: At this step the device configuration file has been saved





Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – EEPROM Image File Creation

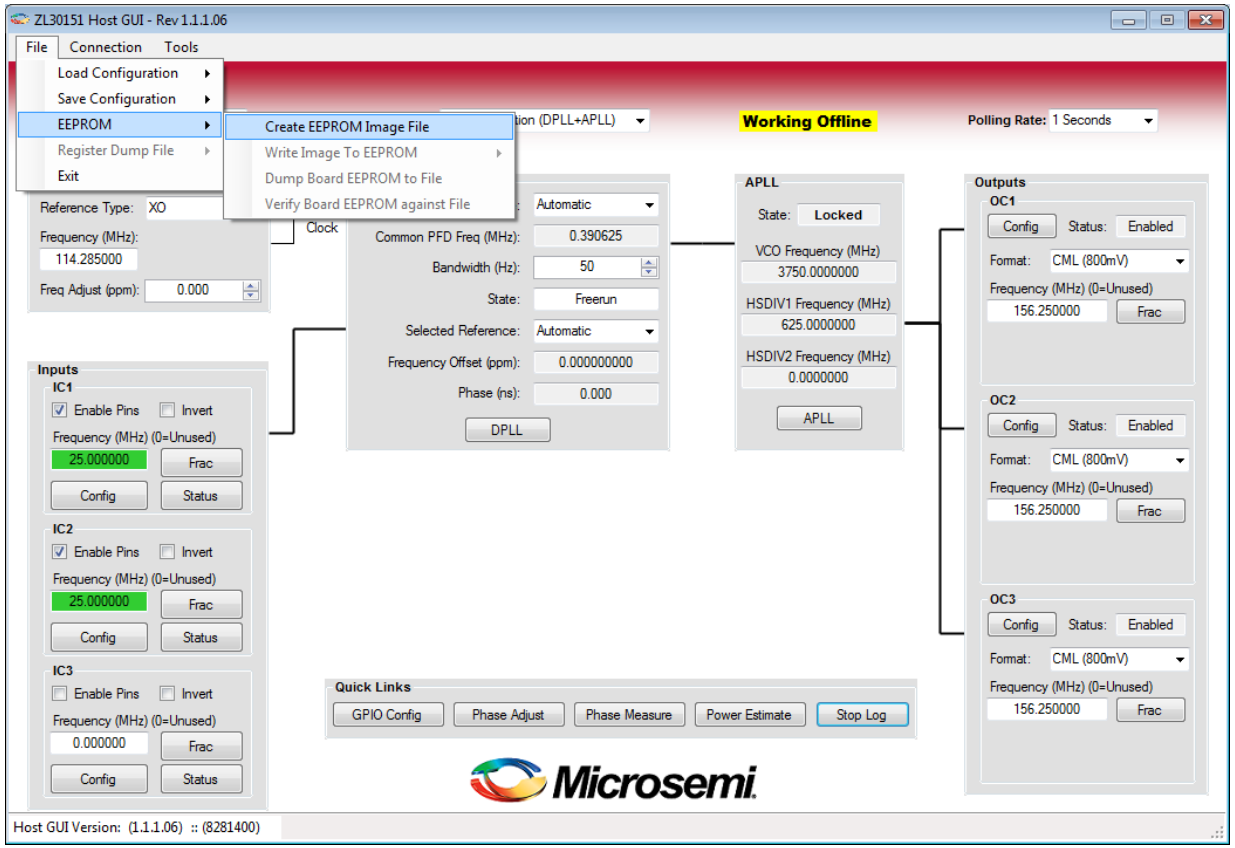
Create an EEPROM image file

15

GUI Main Window

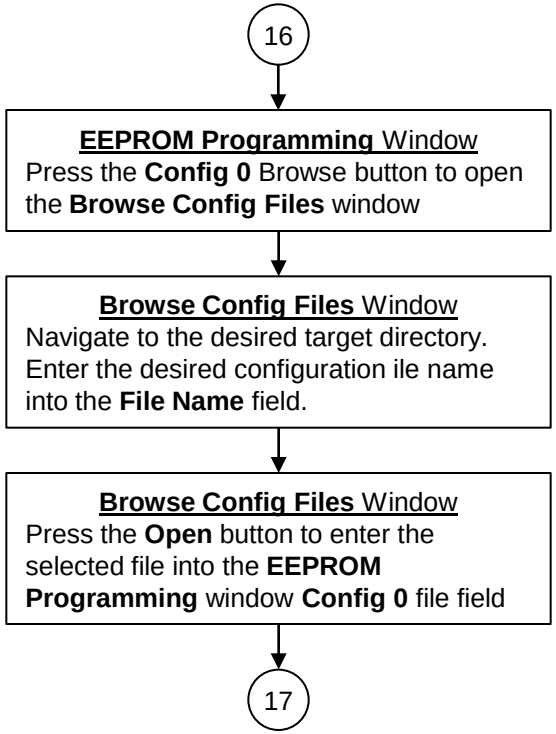
Open the **File -> EEPROM -> Create EEPROM Image File** window to create an EEPROM image file from the saved device configuration file

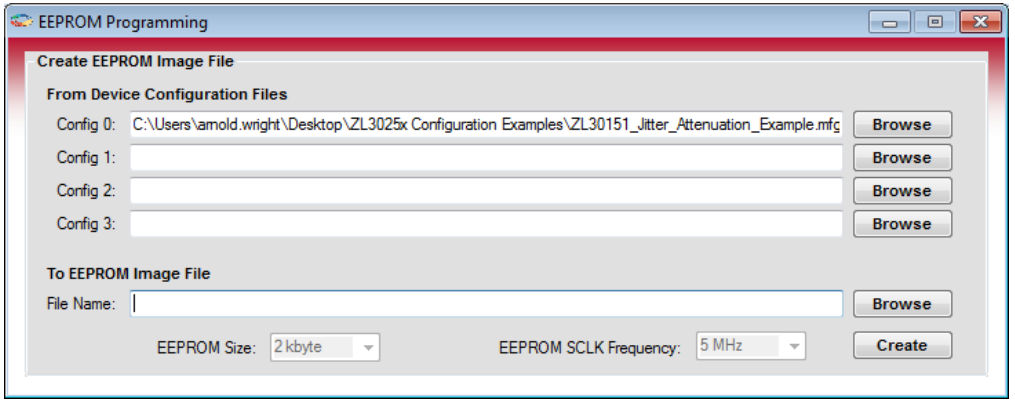
16

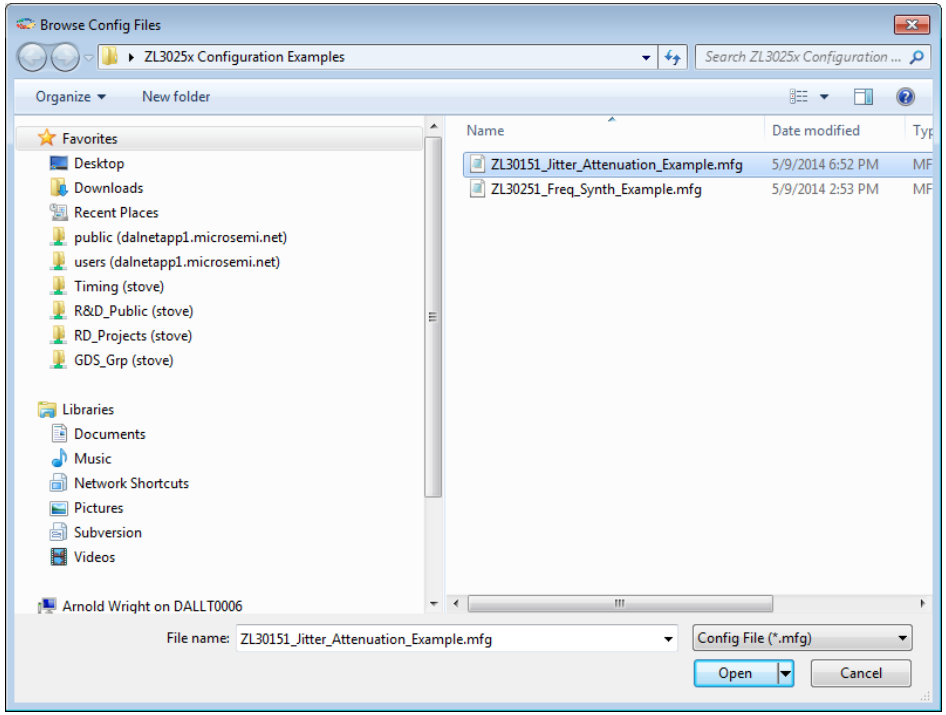


Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – EEPROM Image File Creation

Create an EEPROM image file

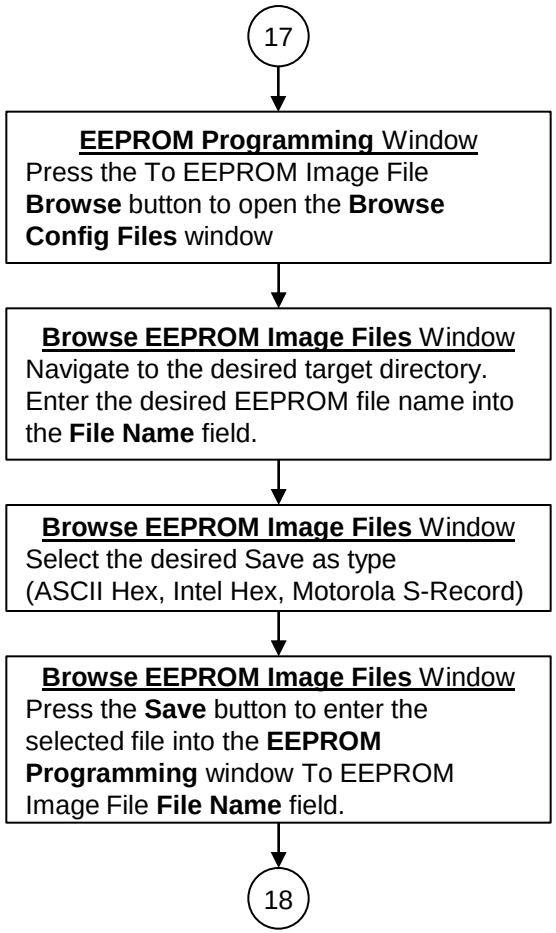


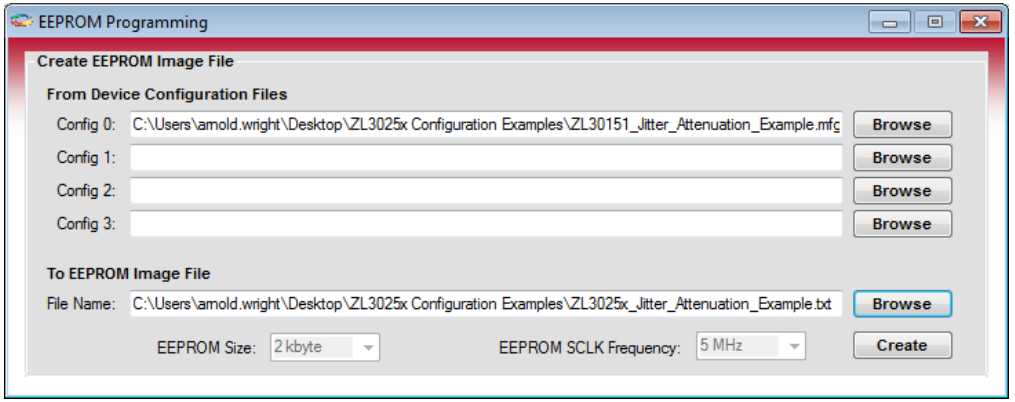


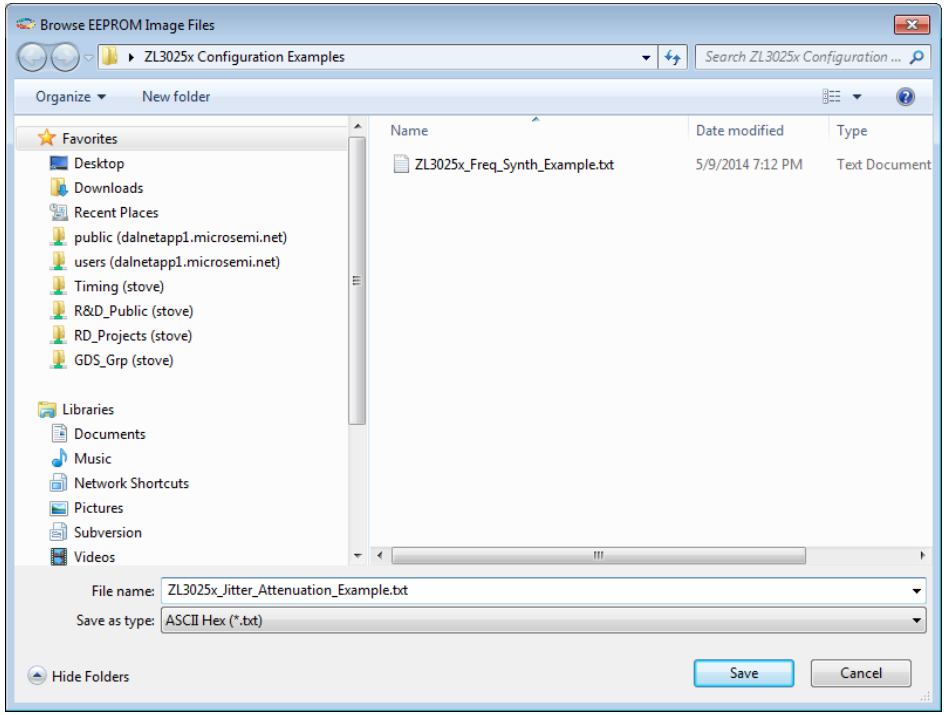


Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – EEPROM Image File Creation

Create an EEPROM image file

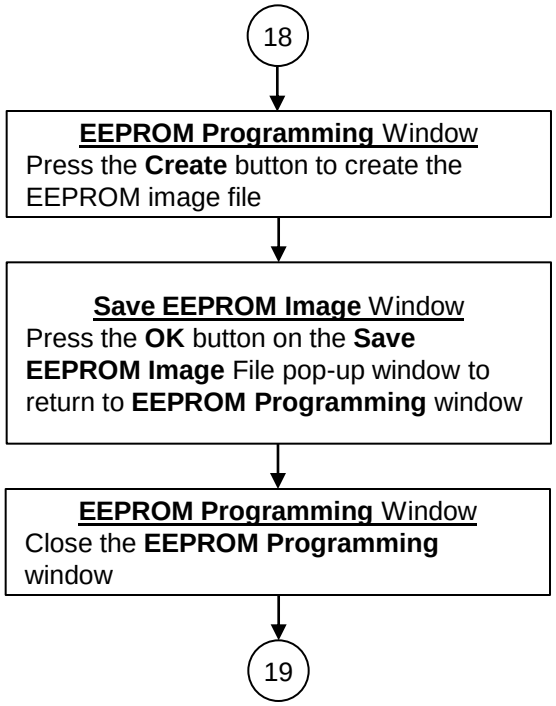




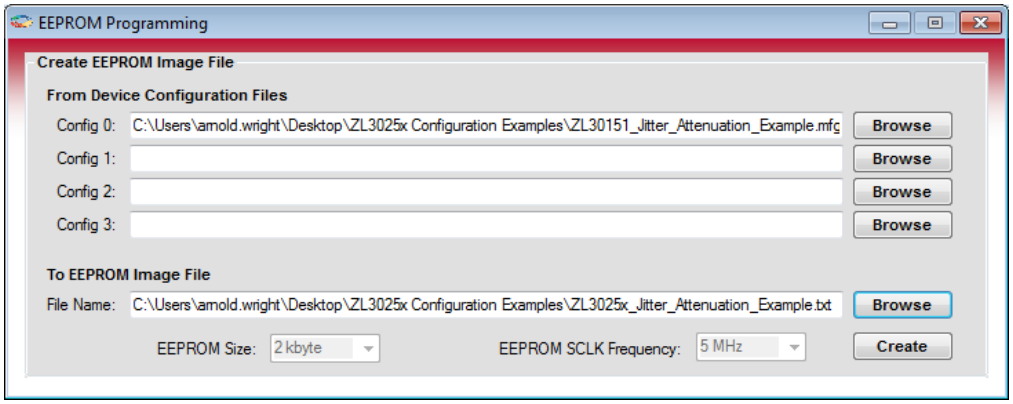


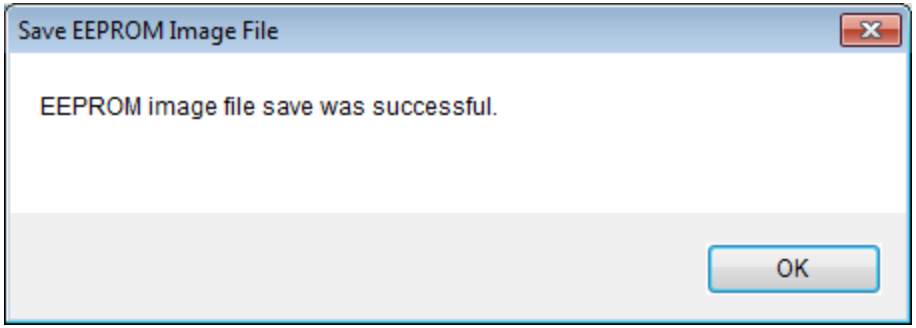
Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – EEPROM Image File Creation

Create an EEPROM image file



Note: At this step the EEPROM Image file has been created and saved





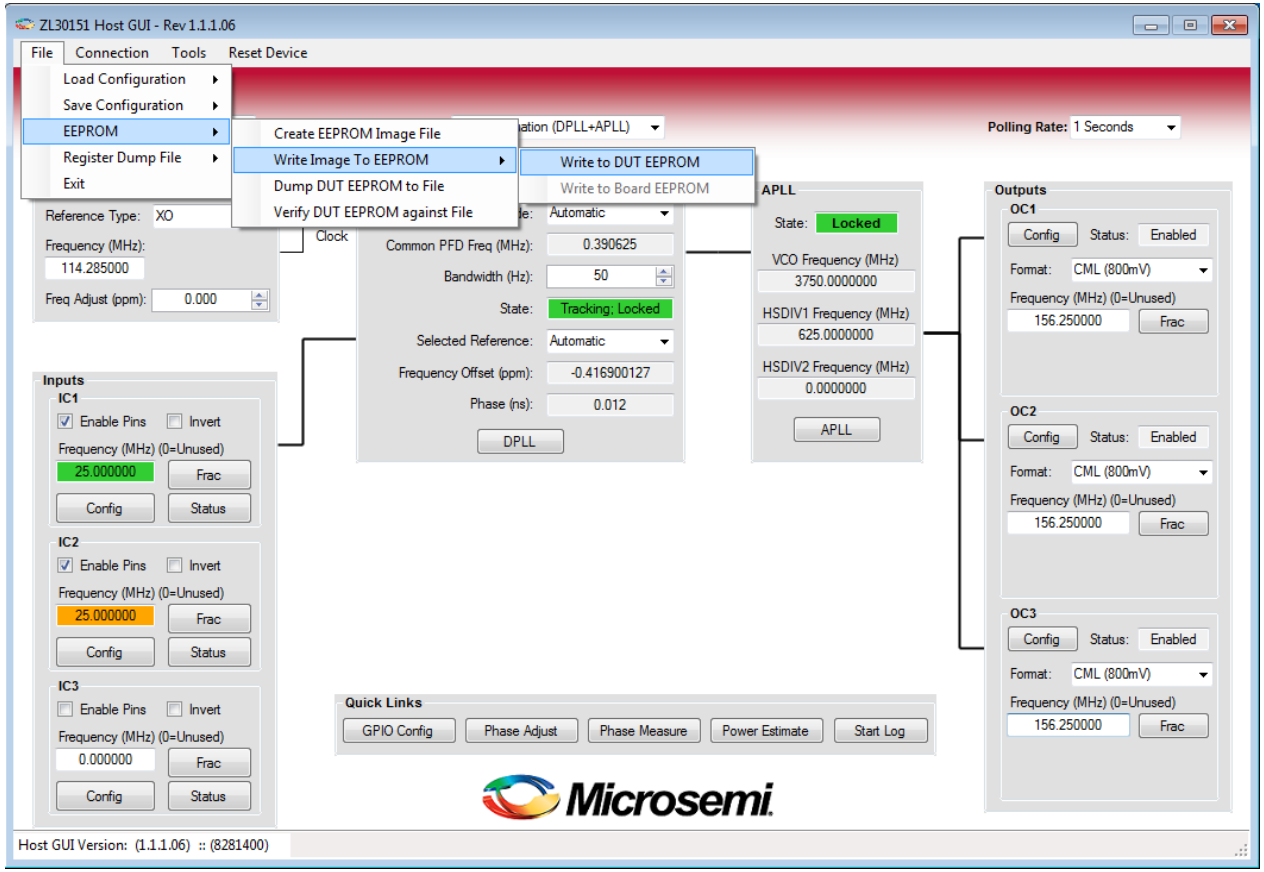
Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – EEPROM Programming

Program the Evaluation Board Device EEPROM
(GUI must be connected to the board)

19

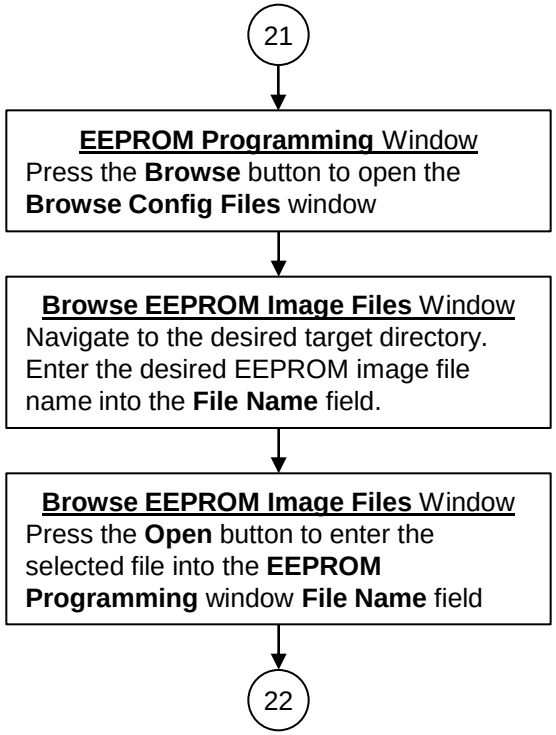
GUI Main Window
Open the **File -> Write Image to EEPROM -> Write to DUT EEPROM** window to program the device EEPROM on the evaluation board

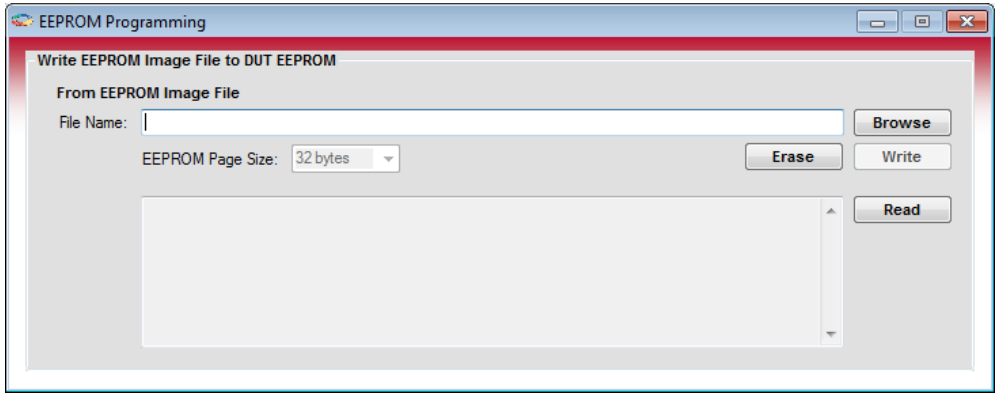
20

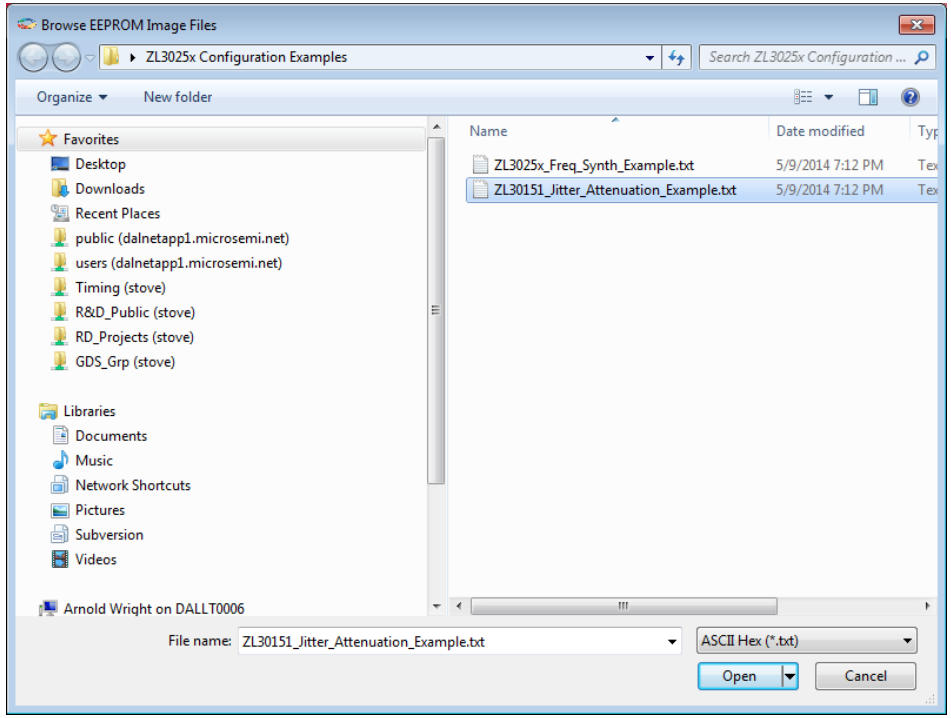


Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – EEPROM Programming

Program the Evaluation Board Device EEPROM (GUI must be connected to the board)

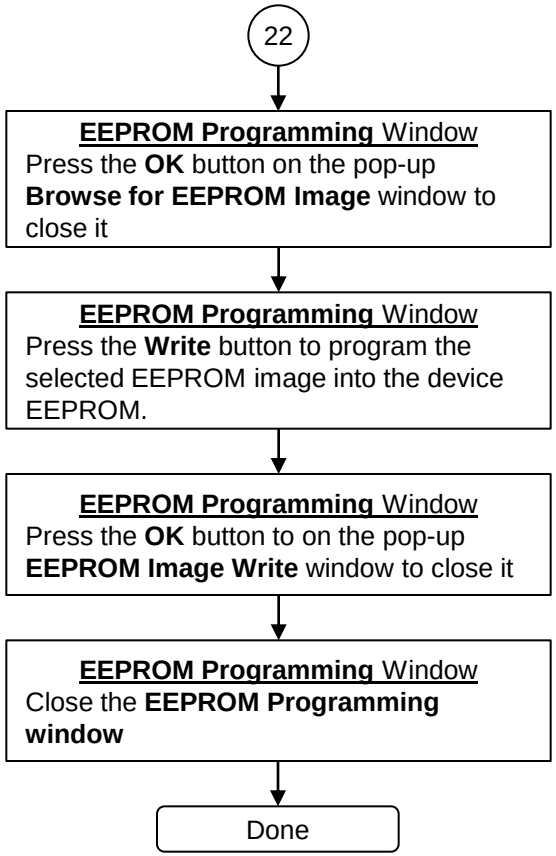




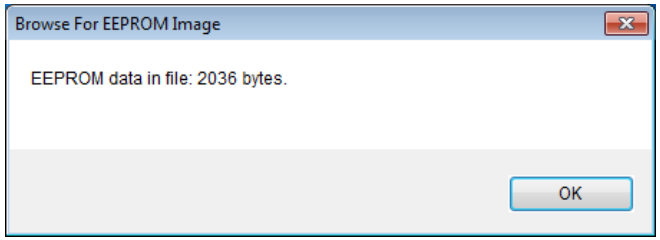


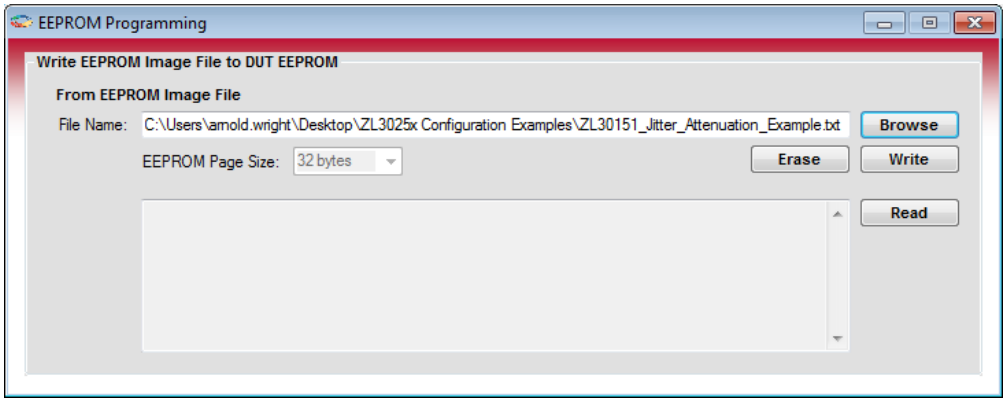
Creating a Jitter Attenuation Mode Device Configuration Step-by-Step Flow Chart – EEPROM Programming

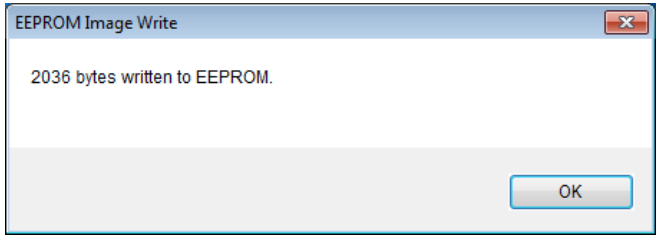
Program the Evaluation Board Device EEPROM (GUI must be connected to the board)



Note: At this step the device EEPROM has been programmed







Evaluation Board Overview and Key Features

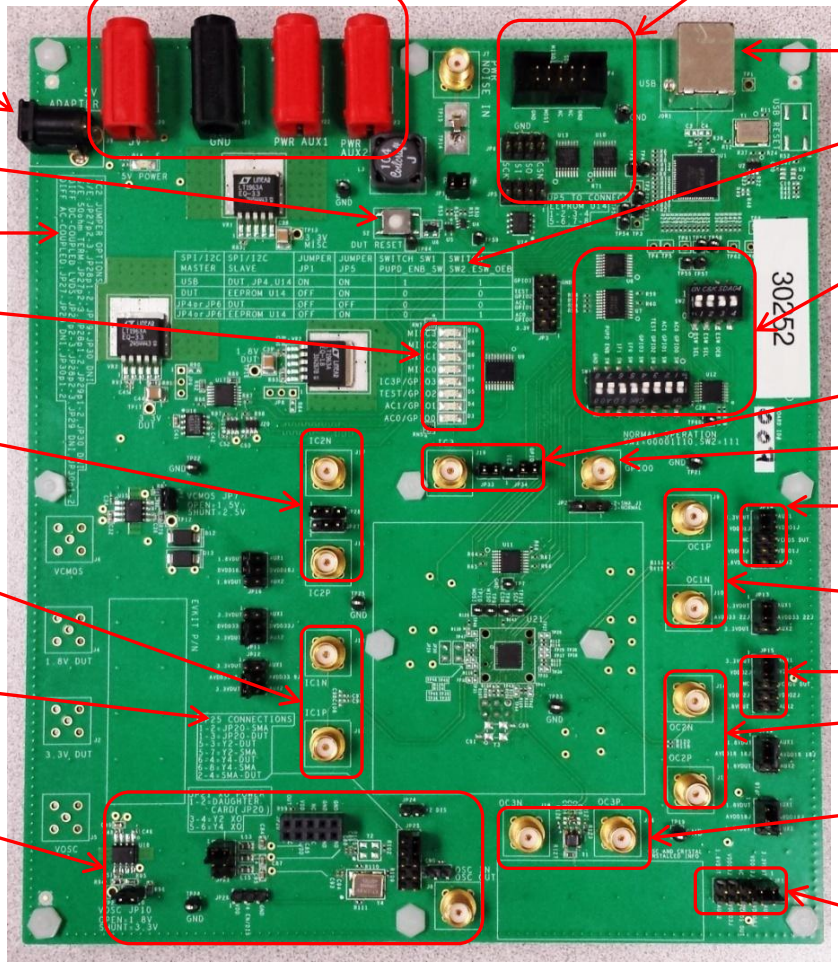
Evaluation Board
Overview

- Evaluation boards are available for the ZL30151, ZL30169, ZL30251, and ZL30253
- Highly configurable for easy evaluation of a wide range of target applications
- Silkscreen labels and instructions for common board configuration options
- Soldered ZL30151/ZL30169/ZL3025x device for best signal integrity
- Easy access to all device input and output clocks, and many device features
- On-board, low-jitter oscillator reference provided for easy device jitter performance evaluation

Evaluation Board
Overview

- Alternate reference clock options can be evaluated using the on-board 5x7mm and 3x5mm footprints, a plug-in oscillator/crystal daughter card, and SMA input connector
- Flexible input clock termination circuit on IC2P/N can be configured to accepts single-ended or differential clock signals, AC or DC coupled
- On-board balun on OC3P/N for easy evaluation of differential output clock jitter performance

Evaluation Board
Key Features

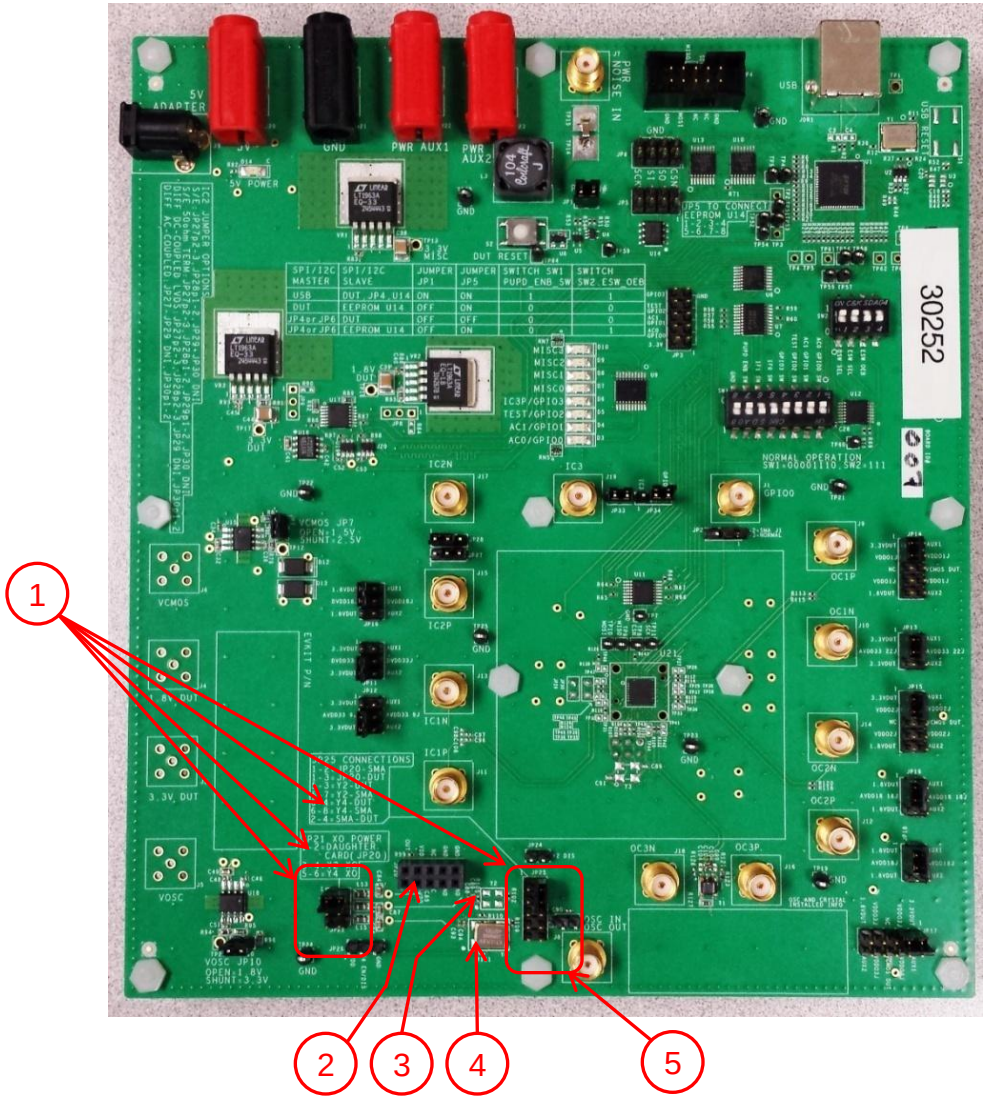


Evaluation Board

Key Features – Reference Clock Options (Top Side of Board)

Supported Options

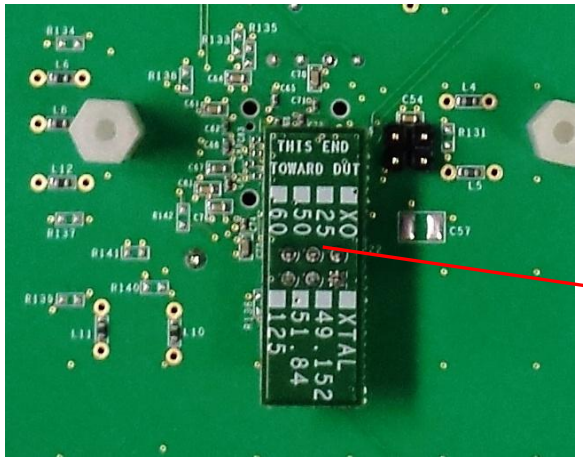
1) Reference clock selection is jumper configurable
   - Refer to silkscreen instructions for jumper configuration details
2) JP20: 5x2 socket for MAX24000 Series oscillator daughter card (not installed)
3) Y2: On-board 3.2x5mm 3.3V/1.8V CMOS oscillator (not installed)
4) Y4: On-board 5x7mm 3.3V/1.8V CMOS Oscillator
   - ZL30151, ZL30169, ZL30252, ZL30153 default installed XO frequency is 114.285MHz
   - ZL30250, ZL30151 default installed XO is 125MHz
5) J8: SMA connector
   - Can be used as an input to apply an external clock signal to the on-board DUT
   - Can be used as an output to access the on-board reference clock



Evaluation Board
Key Features – Reference Clock Options (Bottom Side of Board)

Supported Options Continued

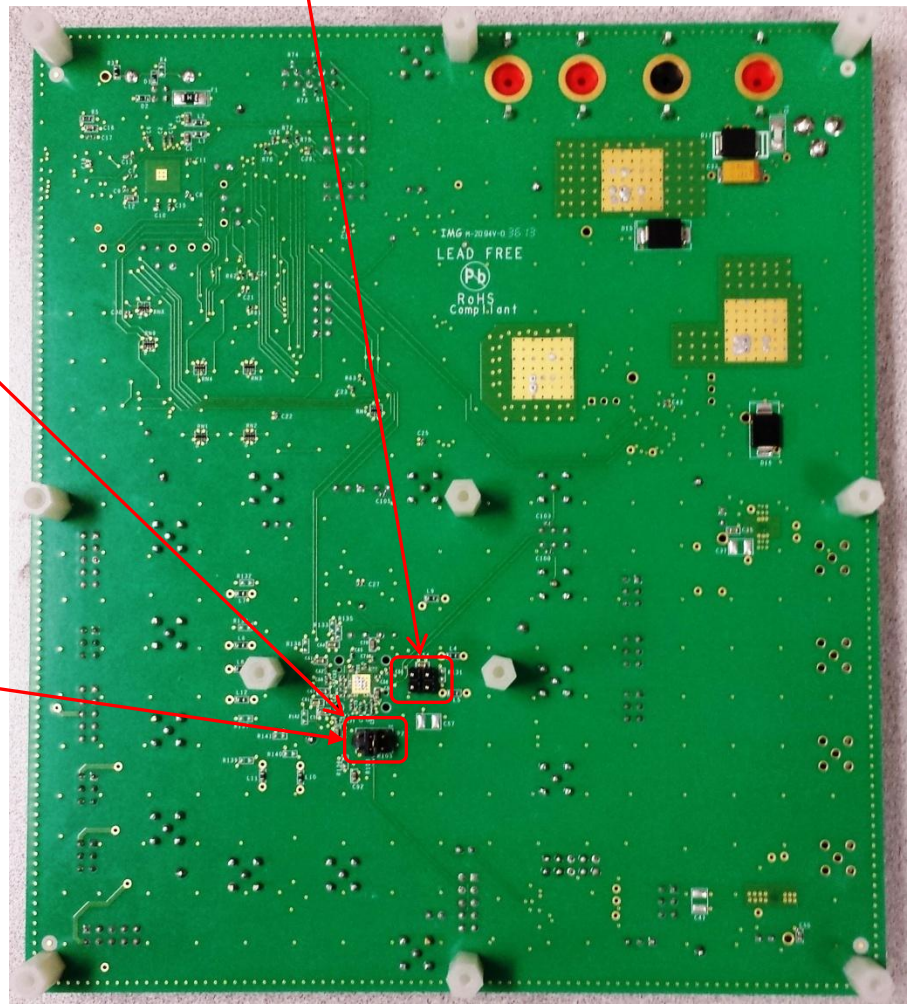
6) JP22: 3x2 header for Oscillator/Crystal daughter card (not installed)
   - A jumper must be installed in position 3-4 when J8 daughter card is not used



JP22 XO/Crystal daughter card installed

IC2P/N input termination network configuration jumpers J29, J30

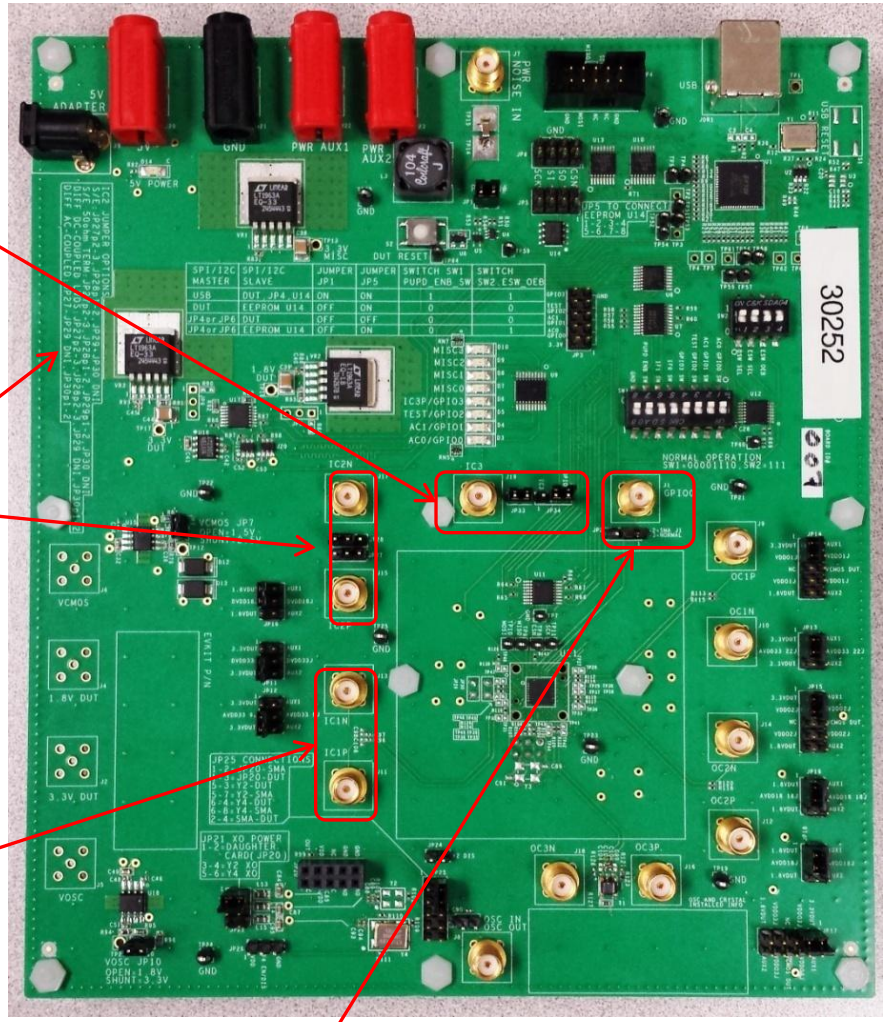
6



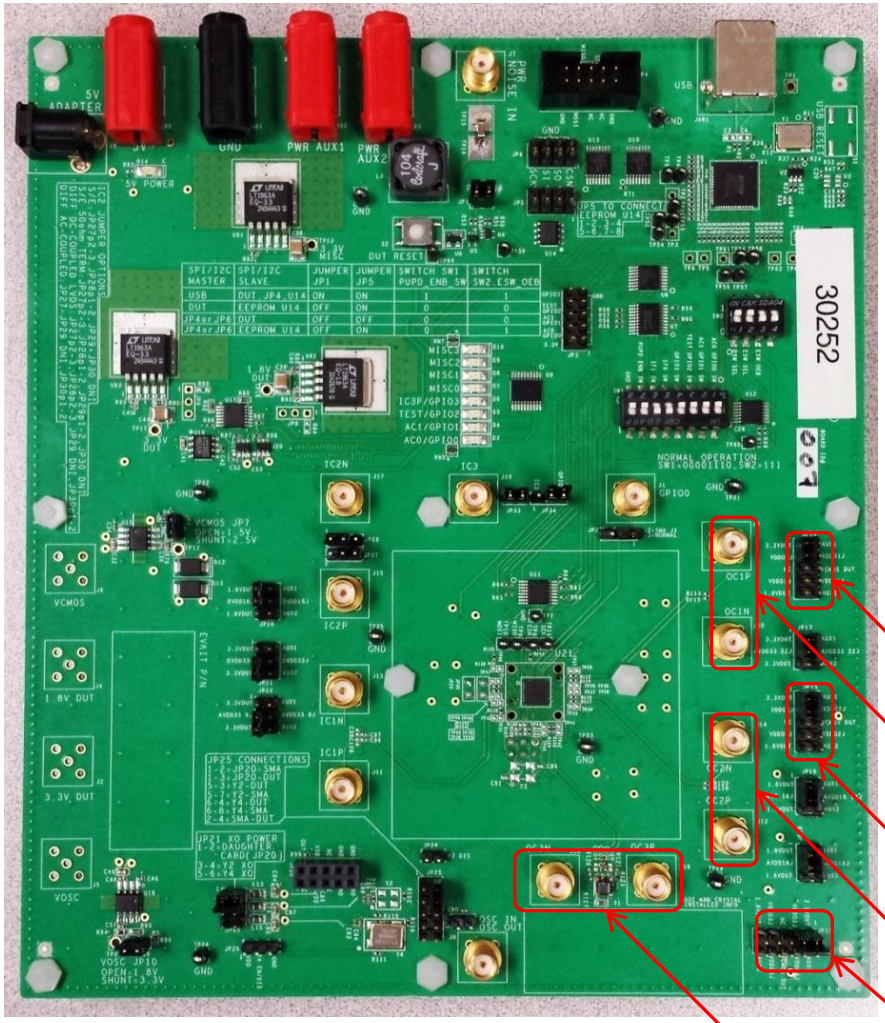
Evaluation Board
Key Features – Input Clock Options

Supported Options

- All 3 input clocks are available on SMA connectors
- IC3/GPIO3
  - Refer to silkscreen instructions for jumper configuration details
  - JP33 controls SMA J19 AC/DC coupling
  - JP34 connects IC3/GPIO to either SMA J19 or an on-board DIP switch
- IC2P/N has a jumper configurable input termination network
  - Refer to silkscreen instructions for jumper configuration details
  - Can be configured as differential or single-ended, AC or DC coupled
  - Jumpers JP29 and JP30 are located on the bottom side of the board (See Slide 81)
- IC1P/N is only AC-coupled, differential for best signal integrity
- GPIO0 accessible via SMA to support external control / monitoring



Evaluation Board
Key Features – Output Clock Options



Supported Options

- All 3 output clocks are available on SMA connectors
- Individually jumper configurable output pad supply voltage
  - On-board 3.3V or 1.8V regulator
  - Banana jack AUX1 or AUX2
- OC1P/N and OC2P/N
  - DC-coupled
  - No series source termination resistor
- OC3P/N
  - On-board balun for easy jitter performance evaluation of a differential mode output
  - Balun output is OC3P

OC1P/N, JP14 Pad Power Selection Jumper

OC2P/N, JP15 Pad Power Selection Jumper

OC3P/N, JP17 Pad Power Selection Jumper, Balun

Evaluation Board Kit Contents

- ZLE30250 Evaluation Board
- 5V DC Power Supply
  - Universal input supply with international AC plug adapters
- USB Cable
- 4 SMA-BNC Cables
- 2 Oscillator / Crystal Daughter Cards

- The GUI is provided separately through the Microsemi website
  - A MyMicrosemi account is required
  - A MyCMPG account is also required
  - With these two accounts the GUI can be downloaded from the website using the Software Delivery System (SDS)

Summary

- The GUI and evaluation board provide an easy-to-use, flexible platform for evaluating device features and performance

- GUI
  - Performs most device configuration details and optimizations automatically
  - Can be used with, or without, an evaluation board
  - Must be used to generate device configurations

- Evaluation Board
  - Easy access to all device input and output clocks, and many device features
  - Highly configurable for easy evaluation of a wide range of applications
  - Oscillator / Crystal daughter card provides an easy way for a customer to evaluate their preferred reference clock option

End