Power over Ethernet

PD69104B – 4 Port PoE Controller

Registers Map User Guide

Rev 0.5

Microsemi
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Introduction

This Register Mapping Matrix includes a detailed description of PD69104A 4-Port PoE device Registers Map**.**

General Note:

PD69104A communication protocol is based on I2C or UART, as illustrated in PD69104A datasheet.

Each Read or Write transaction is framed in a Byte Packets.

Applicable Documents

For additional information on PD69104A applications and functionallity please refer to the following documents:

- IEEE 802.3af-2003 standard, DTE Power via MDI
- IEEE802.3at-2009 standard, DTE Power via MDI
- PD69104A datasheet, catalogue number DS_PD69104A
- Application Note 198, PD69104A MSCC Auto Mode, catalogue number 06-0134-080
- Application Note 192, PD69104A Semi-Auto Mode, catalogue number 06-0128-080
- Evaluation Board User Guide, catalogue number TBD
- Technical Note TBD, Power Management catalogue number TBD

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I²C Protocol Structure with Host

The following diagram describes I²C Communication format of data write/read access:

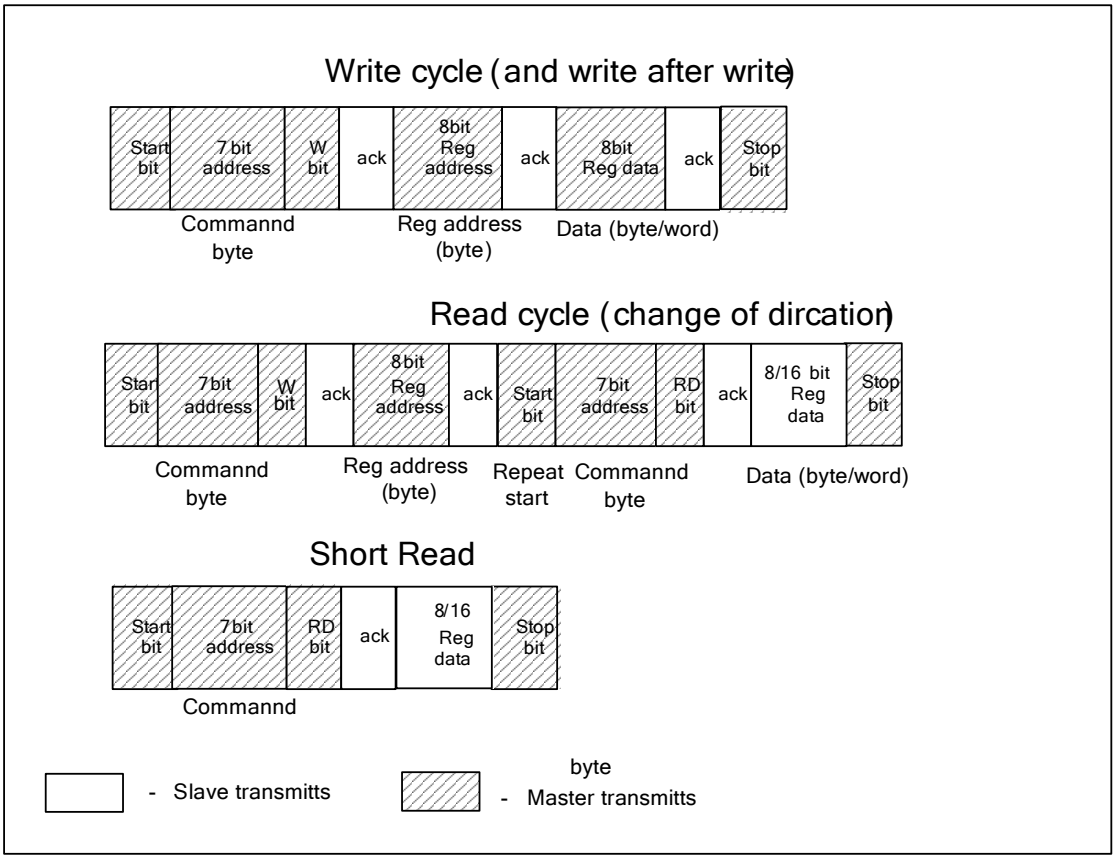

Figure 1: Packet Structure

Address Phase

This phase is common to both read and write accesses:

- Both accesses (read and write) begin with a START indication.
- Slave's address follows a START indication. In case of a miss match, the slave ignores the rest of the access and waits for a 'STOP' indication to close current access. However, in case the slave address matches, next bit indicates the type of the access (read or write).
- Matched slave acknowledges first byte.
- The byte that follows indicates internal register address. The slave should acknowledge the byte.

Data Phase

In this phase the read and write accesses behave differently.

Write access

1. A byte of write data is transmitted to the slave; the slave acknowledges it.
2. A stop indication from the master closes current access.

Read access

1. Another command byte is received, comprising slave address and real command type (in this case read). The slave acknowledges the byte.

2. At this stage, the master is ready to continue the communication and to sample read data; hence, read data must be ready on the next rise of the clock pulse.
3. A byte of data is transmitted to the master; the master acknowledges it.

I²C High Level Layer

The following diagram describes the supported I²C high-level packet structure.

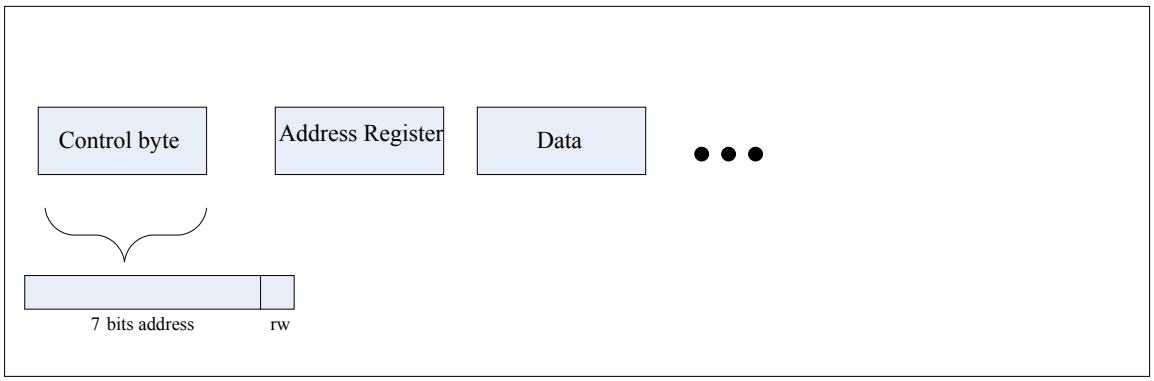

Figure 2: High Level Packet Structure

Byte/Word Read/Write Transaction

First byte is control byte that consists of the chip address and a read/write operation indication.

Second byte is internal chip's address register.

Bytes/words that follow are data bytes. In case of a read operation they are read from the slave and in case of a write operation they are written onto the slave.

Successive Read/Write Transaction

- The master can continue sending bytes that the slaves write, or continue receiving data from a slave during address phase.
- The slave will continue to send/receive data bytes from/to the master until a 'stop bit' is asserted by the master.
- Each byte received by the slave (or each byte from registers to be read) is received from next register address (each byte address is increased by 1).

Read Byte Transaction

The slave supports a 'send byte' transaction.

1. The master begins with a start bit. Byte that follows consists of chip address and a read bit.
2. If chip address is correct the slave acknowledges the byte and immediately (at next sck phase) sends a data byte from a constant address (address 7'h00)
3. A send byte transaction continues with successive read transactions (address 1, address 2 and so on) until the master asserts a stop bit.

Broadcast Support

All slaves answer a general address sent by the master. In case of Auto or Semi-Auto modes general address is 7'h30 and in case of MSCC Extended Auto mode general address is 7'h0.

The broadcast is for master writing only; read access is ignored in a broadcast transaction.

Time Out Mechanism

I²C has an internal counter of 14ms. The counter resets each time the SCL rises or falls. If SCL is “stuck” for 14ms, I²C returns to IDLE state and transaction is ignored (Time Out mechanism is active between start bit and stop bit).

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I^2C Timing Constraints

Table 1: Characteristics of the SDA and SCL Bus Lines for F/S-mode I2C-Bus

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I^2C-bus devices	$t_{HD;DAT}$	 5.0 0(2)	 – 3.45(3)	 – 0(2)	 – 0.9(3)	 µs µs
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	$20 + 0.1C_b$(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	$20 + 0.1C_b$(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	$0.2V_{DD}$	–	V

Notes

1. All values refer to V_{IHmin} and V_{ILmax} levels (as specified in PD69204A datasheet).
2. A device must internally provide a hold time of at least 300ns for the SDA signal (refers to V_{IHmin} of SCL signal) to bridge the undefined region of the falling edge of SCL.
3. Maximum $t_{HD;DAT}$ has to be met only if device does not stretch LOW period (t_{LOW}) of SCL signal.
4. A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement of 250ns $t_{SU;DAT}$ must then be met. This is the in case device does not stretch LOW period of SCL signal.
5. If device does stretch LOW period of SCL signal, it must output next data bit to SDA line $t_{r_max} + t_{SU;DAT} = 1000 + 250 = 1250$ns (according to Standard-mode I^2C-bus specification) before SCL line can be released.
6. n/a = not applicable

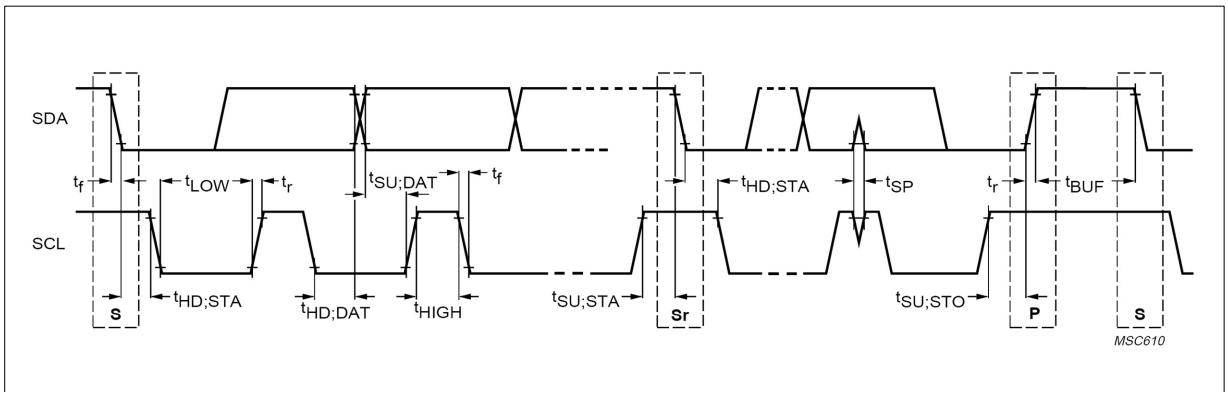

Figure 3: Definition of Timing for F/S-mode Devices on the I²C-bus

UART Communication

UART (Universal Asynchronous Receive Transmit) is supported by PD69104A platform to allow communication between PD69104A IC's and an external host, at Auto mode only.

PD69104A platform supports UART only as a slave.

Features List

- Slave mode.
- Supports 4,800 to115,200 Baud rate, auto learning mechanism
- Supports 8 bit address.
- Supports 8 bit data access.
- Supports general broadcast transmission.
- 8N1:
  - 8 bits data
  - No parity
  - 1 stop bit
- Frame transaction – header, payload and suffix.
- Time out mechanism (time out for frame and per byte).
- No successive read/write – one transaction per register (read/write).
- Half duplex implementation – Rx starts after Tx ends
- A filter for glitches cancelling on RX pin.

Physical Layer

The UART protocol has two data lines; Rx, from where PD69104A receives its data, and Tx, throughout where data is transmitted. UART is a byte protocol in which every byte starts with a 'start bit' and ends with a 'stop bit'.

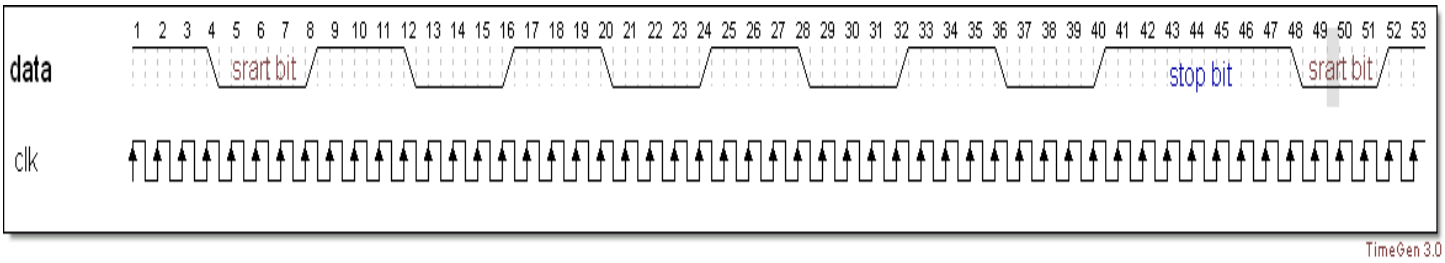

Figure 4: UART Read/Write Frame

Data is sent in a constant frame to be synchronized. Figure 5 and Figure 6 describe data read frame.

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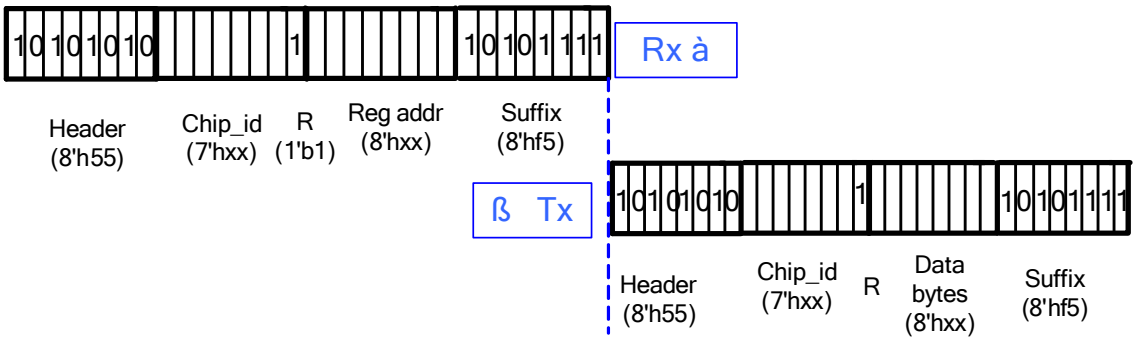

Figure 5: Master's Read Packet Structure

Figure 6: Master's Write Packet Structure

1. First byte is control byte consists of chip address and a read/write operation indication.
2. Second byte consists of chip's internal ram address.
3. Bytes that follow are data bytes. In case of a read operation they are read from the slave and in case of a write operation they are written onto the slave.

Broadcast Support

All slaves answer a general address sent by the master. The general address is 7'h0.

The broadcast is for master writing only; read accesses are ignored in a broadcast transaction.

Auto Baud Rate Learning

PD69104A has a self-learning baud rate mechanism that allows synchronizing all PD69104A slaves to the master's "real" baud rate and thus working with a higher baud rate.

First byte received by the slave is 8'hAA. At the rising or falling edge of each bit, an 8MHz counter starts counting the bit width (in a 125ns resolution). Average width of 8 header bits is actual bits rate. By using this mechanism, PD69104A slaves can be synchronized with the master and set back data at that rate. Header is a preamble bit that facilitates synchronization.

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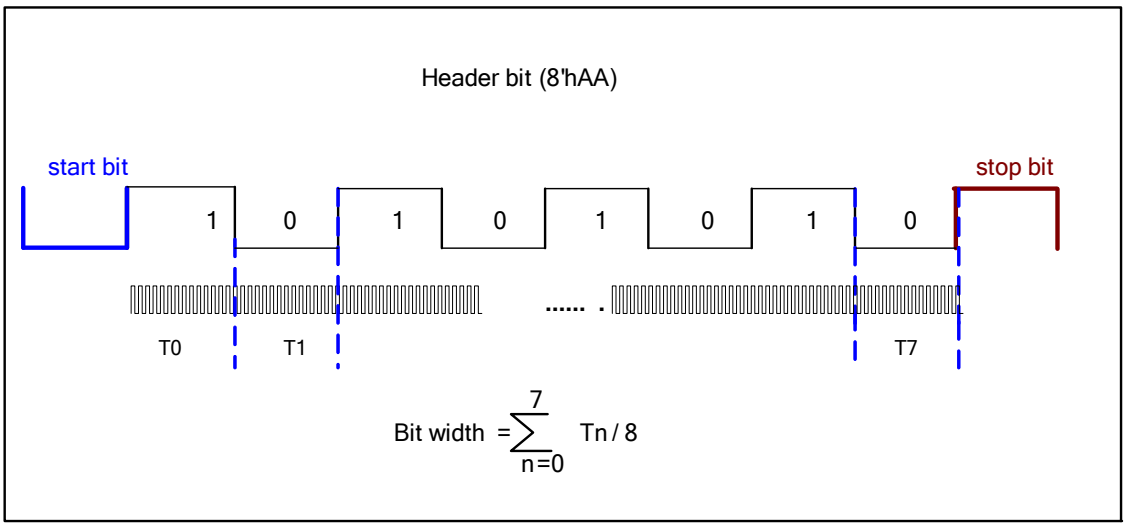

Figure 7: Header Bit Width

Timeout Mechanisms

UART protocol has a frame timeout mechanism. This mechanism has two purposes:

- **Distinguishing between frame's suffix of 8'f5 and a payload byte with the same value:** The mechanism identifies a frame suffix only when it arrives as 2-bytes in a read access or as 4-bytes in a write access; otherwise it is treated as a data byte.
- **Preventing UART communication from getting stuck:** A one second timeout counter is activated beginning with a start frame (end of header byte) till a suffix arrival. If a suffix byte does not arrive within that time the transaction is ignored and slave moves into an IDLE state.

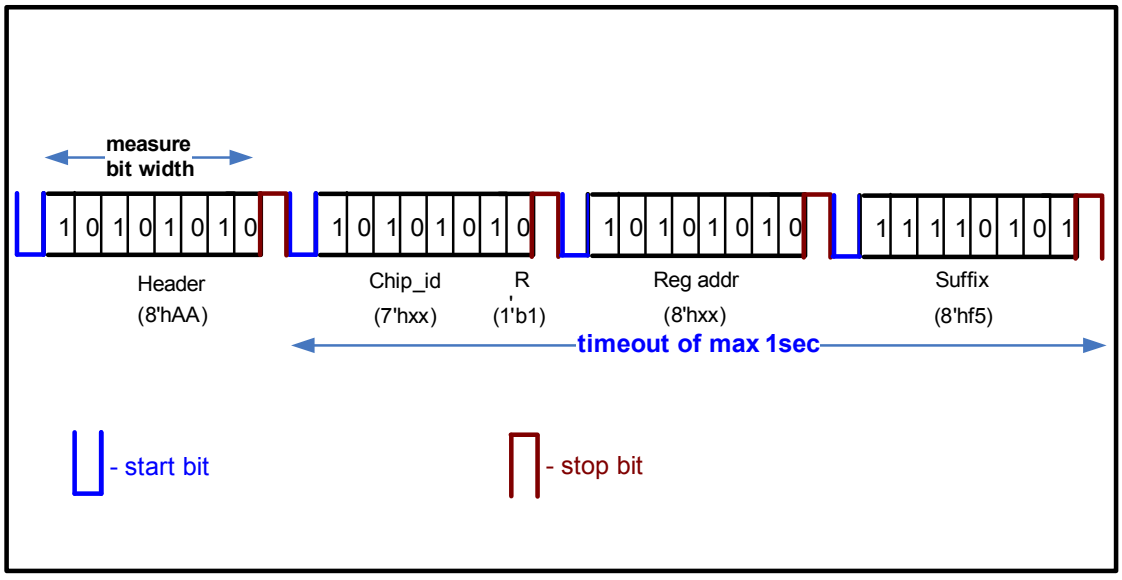

Figure 8: Timeout Mechanism

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Registers Mapping and Description

R/W ACCESS KEY:

COR Clear on Read. Register clears when read. Writing to these registers has no effect.
R/W Read/Write. Register can be read or write
RO Read Only. Register can be read only. Writing to these registers has no effect.
SO Set Only. Writing "1" - set the bit, Writing "0" – bit is unchanged (Data read from these registers is meaningless)
" / " Bit (or Byte) default value – depends on IC I/O configuration (pull up or pull down)

Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
0	INT	8	[0]	Power Enable Interrupt. Sets if any power status bit in PWREVN register (02h) is set.	Interrupt Status Register, Read Only. Summarizes events from registers 02h through 0Ah	0	RO
			[1]	Power Good Interrupt. Sets if any power good bit in PWREVN register (02h) is set.		0	RO
			[2]	Disconnect Interrupt. Sets if any disconnect bit in FLTEVN register (06h) is set.		0	RO
			[3]	Detect Interrupt. Sets if any detection bit i DETEVN register (04h) is set.		0	RO
			[4]	Class Interrupt. Sets if any class bit in DETEVN register (04h) is set.		0	RO
			[5]	t_{CUT} Interrupt. Sets if any t_{CUT} bit in FLTEVN register (06h) is set, or if any tLIM bit in TSEVN register (08h) is set.		0	RO
			[6]	t_{START} Interrupt. Sets if any t_{START} bit in TSEVN register (08h) is set.		0	RO
			[7]	Supply Interrupt. Sets if any bit in register 0Ah is set.		1	RO
1	INTMASK	8	[0]	When this bit is set Power Enable events can pull INT_OUT low.	Interrupt Mask Register, Read/Write. bits in this register are AND'ed with bits in register 00h and then OR'ed together; the result determines if the slave pulls INT_OUT line low; other slaves within the system may also be pulling INT_OUT low.	0	RW
			[1]	When this bit is set Power Good events can pull INT_OUT low.		0	RW
			[2]	When this bit is set Disconnect events can pull INT_OUT low.		1/0	RW
			[3]	When this bit is set Detect events can pull INT_OUT low.		0	RW
			[4]	When this bit is set Class events can pull INT_OUT low.		0	RW
			[5]	When this bit is set tCUT events can pull INT_OUT low.		1/0	RW
			[6]	When this bit is set tSTART events can pull INT_OUT low.		1/0	RW
			[7]	When this bit is set Supply events can pull INT_OUT low.		1	RW
2	PWREVN	8	[0..3]	Ports 1 to 4 power status change. (occurs when a port is turned on or off)	Power event Register, Read Only. Lower 4 bits indicate Power Enable events, which occur when a port is turned on or off. Upper 4 bits are set when Power Good status of the applicable	0	RO

Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
			[4..7]	Ports 1 to 4 power good change. (when power good status of the port changes)	port(s) change. See STATPWR register (10h)	0	RO
3	PWREVN_COR	8	[0..3]	Ports 1 to 4 power status change. (occurs when a port is turned on or off)	Power Event register, Clear on Read. Identical to PWREVN register (02h) except that reading of this register clears both power status and PWREVN_COR registers	0	COR
			[4..7]	Ports 1 to 4 power good change. (when power good status of the port changes)		0	COR
4	DETEVN	8	[0..3]	Ports 1 to 4 detection cycle completed.	Detection and Classification Event register, Read Only. Lower 4 bits indicate that port has completed a detection cycle. 4 upper bits indicate port has completed classifying the PD. Detection's/Classification's results are available in ports' STATP register (0Ch to 0Fh).	0	RO
			[4..7]	Ports 1 to 4 classification completed.		0	RO
5	DETEVN_COR	8	[0..3]	Ports 1 to 4 detection cycle completed.	Detect and Classification Event register, Clear on Read. Identical to DETEVN register (04h) except that reading of this register clears both DETEVN and DETEVN_COR registers.	0	COR
			[4..7]	Ports 1 to 4 classification completed.			
6	FLTEVN	8	[0..3]	Ports 1 to 4 over current time out (t_{CUT}).	Overload & Under-load Time Out register, Read Only. Lower 4 bits indicate port has been turned off because load current was above ICUT or ILIM lasted for longer than tCUT. Upper 4 bits indicate when port has been turned off because PD was disconnected.	0	RO
			[4..7]	Ports 1 to 4 disconnect time out (t_{DIS}).		0	RO
7	FLTEVN_COR	8	[0..3]	Ports 1 to 4 over current time out (t_{CUT}).	Overload & Under-load Time Out register, Clear on Read. Identical to FLTEVN Register (06h) except that reading of this register clears both FLTEVN and FLTEVN_COR registers	0	COR
			[4..7]	Ports 1 to 4 disconnect time out (t_{DIS}).			
8	TSEVN	8	[0..3]	Ports 1 to 4 over current during startup time out (t_{START}). A set bit indicates port has been turned off due to over current during start up for period longer than t_{START}.	Overload During Start Up Time Out register, Read Only. Lower 4 bits indicate port has been turned off because of an unsuccessful startup. Upper 4 bits indicate port has turned off because it was in current-limit for longer than tLIM.	0	RO
			[4..7]	Ports 1 to 4 current limit time out (t_{LIM}). A set bit indicates port has been turned off , since after startup it was forced to limit the current for a period longer than t_{LIM}		0	RO
9	TSEVN_COR	8	[0..3]	Ports 1 to 4 over current during startup time out (t_{START}).	Overload During Start Up Time Out register, Clear on Read. Identical to TSEVN register (08h) except that the reading of this register clears both TSEVN and TSEVN_COR registers.	0	COR
			[4..7]	Ports 1 to 4 current limit time out (t_{LIM}).			

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Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
A	SUPEVN	8	[0]	IC power is externally supplied from one of the ports – MSCC proprietary	Supply Event register, Read Only. Bits in this register indicate problems with power supplies, temperature, or MOSFET failures.	0	RO
			[1]	Reserved		1	RO
			[2]	Chip temperature is over the temperature alarm threshold (9Dh) – MSCC proprietary		0	RO
			[3]	Over Voltage Lock Out (OVLO) on main supply (V_{MAIN}) – MSCC proprietary		0	RO
			[4]	Under Voltage Lock Out (UVLO) on main supply (V_{MAIN}).		1	RO
			[5]	One port or more were denied to power up due to power management – MSCC proprietary		1	RO
			[6]	If this bit is set one or more MOSFETs may have failed. To determine which ports may have bad FETs read the HPSTAT registers (49h, 4Eh, 53h, and 58h).		0	RO
			[7]	This bit is set in case of a thermal shutdown. All ports are turned off. This bit can be cleared by reading supevn_cor but tsd bit in wdog register (42h) will remain set as long as temperature remains above threshold.		0	RO
B	SUPEVN_COR	8	[0..7]	Register 0Ah Clear On Read	Supply Event register, Clear on Read. Identical to SUPEVN register (0Ah) except that reading of this register clears both SUPEVN and SUPEVN_COR registers.	0	COR
C	STATP1	7	[2:0]	Result of last detection on Port 1: 0=Unknown; 1=Short; 2=Cpd too high; 3=RSIG too low; 4=Good; 5=RSIG too high; 6=Open circuit; 7=Reserved.	Port 1 Status register, Read Only. This register shows results of detection and classification.	0	RO
			[3]	Always returns 0.		0	RO
			[6:4]	Result of last classification on Port 1. 0=Unknown; 1=Class 1; 2=Class 2; 3=Class 3; 4=Class 4; 5=Reserved; 6=Class 0; 7=Over-current.		0	RO
D	STATP2	7	[2:0]	Result of last detection on Port 2. (For details see STATP1.)	Port 2 Status resgister, Read Only. This register shows results of detection and classification	0	RO
			[3]	Always returns 0.		0	RO
			[6:4]	Result of last classification on Port 2. (For details see STATP1.)		0	RO
E	STATP3	7	[2:0]	Result of last detection on Port 3. (For details see STATP1.)	Port 3 Status register, Read Only. This register shows results of detection and classification	0	RO
			[3]	Always returns 0.		0	RO
			[6:4]	Result of last classification on Port 3. (For details see STATP1.)		0	RO

Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
F	STATP4	7	[2:0]	Result of last detection on Port 4. (For details see STATP1.)	Port 4 Status register, Read Only. This register shows results of detection and classification	0	RO
			[3]	Always returns 0.		0	RO
			[6:4]	Result of last classification on Port 4. (For details see STATP1.)		0	RO
10	STATPWR	8	[0]	Power enabled on Port 1. Indicates port has been turned on. Sets to '0' when port is turned off	Power Status register, Read Only. This register indicates power status of each port	0	RO
			[1]	Power enabled on Port 2.		0	RO
			[2]	Power enabled on Port 3.		0	RO
			[3]	Power enabled on Port 4.		0	RO
			[4]	Power good on Port 1. Indicates power good (after successful startup)		0	RO
			[5]	Power good on Port 2.		0	RO
			[6]	Power good on Port 3.		0	RO
			[7]	Power good on Port 4.		0	RO
11	STATPIN	6	[0]	State of MODE1 pin: 1=DVDD; 0=Tied to GND. "0"- Semi Auto mode "1"- Auto mode	Pin Status register, Read Only		RO
			[1]	Always returns 0.			RO
			[3:2]	Indicates which slave (4-port controller) within the system is being addressed: (ADDR0:1) 00 =Ports A-D; 01 =Ports E-H; 10 =Ports I-L; 11 =Ports M-P.			RO
			[4]	State of the ADDR2 pin: 1=DVDD; 0=Tied to GND.			RO
			[5]	State of the ADDR3 pin: 1=DVDD; 0=Tied to GND			RO
12	OPMD	8	[1:0]	Operating mode for Port 1. 00 =Shutdown; 01 =Manual; 10 =Semi-auto; 11 =Auto.	Operating Mode register, Read/Write. This register sets operating mode for each port.	3/0	RW
			[3:2]	Operating mode for Port 2		3/0	RW
			[5:4]	Operating mode for Port 3		3/0	RW
			[7:6]	Operating mode for Port 4		3/0	RW
13	DISENA	8	[0]	Enables DC disconnect sensing on Port 1.	Disconnect Sensing Enable register, Read/Write. This register enables AC and/or DC disconnect sensing on each port. PD69104A doesn't have AC disconnect sensing capability, therefore it enables DC disconnect sensing when bits 4 to 7 are set.	0	RW
			[1]	Enables DC disconnect sensing on Port 2		0	RW
			[2]	Enables DC disconnect sensing on Port 3		0	RW
			[3]	Enables DC disconnect sensing on Port 4		0	RW
			[4]	Enables AC disconnect sensing on Port 1. (will always be '0')		1/0	RW
			[5]	Enables AC disconnect sensing on Port 2 (will always be '0')		1/0	RW
			[6]	Enables AC disconnect sensing on Port 3 (will always be '0')		1/0	RW
			[7]	Enables AC disconnect sensing on Port 4 (will always be '0')		1/0	RW
14	DETENA	8	[0]	Enables detection on Port 1. • In Auto and Semi-auto modes setting this bit enables detection; the slave will periodically perform a detection cycle	Detection and Classification Enable register, Read/Write. These bits can also be set by writing to DETPB register	1/0	RW

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Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
				and report a result. • In Manual mode port will perform only one detection cycle each time this bit is set. Bit will be cleared afterwards. • In Shutdown mode this bit has no effect.	(18h). Behavior of these bits depends on ports' operating mode		
			[1]	Enables detection on Port 2			
			[2]	Enables detection on Port 3			
			[3]	Enables detection on Port 4			
			[4]	Enable classification on Port 1. • In Auto and Semi-auto modes setting this bit enables classification that follows a successful detection. • In Manual mode port will perform only one classification each time this bit is set. Bit will be cleared afterwards. • In Shutdown mode this bit has no effect.			
			[5]	Enables classification on Port 2			
			[6]	Enables classification on Port 3			
			[7]	Enables classification on Port 4			
15	MIDSPAN	4	[0]	Enables midspan back-off timer on Port 1.	Midspan Back-off Enable register. "1" - (Pin @ VDD) = ALT A No Midspan Mode (pin status = 1 => MIDSPAN bit = 0) "0" - (Pin @ GND) = ALT B Midspan Mode (pin status = 0 => MIDSPAN bit = 1)	Defined by ALT A/B pin	RW
			[1]	Enables midspan back-off timer on Port 2.			RW
			[2]	Enables midspan back-off timer on Port 3.			RW
			[3]	Enables midspan back-off timer on Port 4.			RW
16	TCONF	8	[7:0]	Reserved		0	RW
17	MCONF	8	[0]	Reserved (should be set to "0")	Miscellaneous Configuration register, Read/Write.	0	RW
			[1]	Reserved (should be set to "0")		0	RW
			[2]	Reserved (should be set to "0")		0	RW
			[3]	Reserved (should be set to "0")		0	RW
			[5:4]	Reserved (should be set to "10")		2	RW
			[6]	When this bit is set, detect events are generated only when result is different from previous detection on this port. When this bit is cleared, a ports' bit in the DETEVN register (04h) is set every time the slave completes a detection cycle.		0	RW
			[7]	When this bit is cleared the slave will not pull INT_OUT line.		1	RW
18	DETPB	8	[3:0]	Sets bits [3:0] in DETENA register (14h) which enables detection on ports.	Detection and Classification Restart Pushbutton register, Set Only. This pushbutton register is used to set corresponding bits in DETENA register (14h). Lower 4 bits enable detection while upper 4 bits enable classification. For a port in Manual mode, writing 1 to a bit in this pushbutton register will start a single	0	SO
			[7:4]	Sets bits [7:4] in DETENA register (14h) which enables classification on ports			

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Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
					detection or classification cycle; DETENA bit for the port will be set by this pushbutton and automatically cleared after detection or classification cycle is completed. For a port in Auto or Semi-auto mode detection and/or classification will run until disabled.		
19	PWRPB	8	[3:0]	Turns on corresponding port	Power On/Off Pushbutton register, Set Only. If a port is in Manual mode this register can be used to force it to turn on; if a port is in Auto or Semi-auto mode it won't turn on until a valid PD signature is detected. Setting any of the Off bits turns off corresponding port and also clears related Detect and Fault Event bits, Port Status register, and Detection and Classification enable bits for that port.	0	SO
			[7:4]	Turns off corresponding port			
1A	RSTPB	8	[0]	Resets Port 1. Setting this bit also clears the following bits: Power Enable bit in STATPWR register; Detection and Fault Event bits; Port Status register; and Detection and Classification Enable bits	Reset Pushbutton register, Set Only	0	
			[1]	Resets Port 2		0	
			[2]	Resets Port 3		0	
			[3]	Resets Port 4		0	
			[4]	Resets all four ports.		0	
			[5]	Reserved – Always returns 0		0	
			[6]	Clears interrupt pin. Setting this bit releases INT_OUT line (if it is being pulled low by this slave). When INT_OUT line is released in this way, condition(s) causing the slave to assert INT_OUT must be removed before the slave can assert INT_OUT again.		0	
			[7]	Clears all event registers (02h through 0Bh).		0	
1B	ID	8	[7:0]	Identification register REV: [2:0] DEV: [7:3]		2E	RO
1E	TLIM12	8	[3:0]	t_{LIM} timer for Port 1. Timer duration is 1.71 (typ) times the value of this field in [ms]. When this field is 0, timer is disabled and t_{CUT} timer limits overloads' duration.	t_{LIM} Timer register, Ports 1 and 2, Read/Write	0	RW
			[7:4]	t_{LIM} timer for Port 2		0	RW
1F	TLIM34	8	[3:0]	t_{LIM} timer for Port 3. Timer duration is 1.71 (typ) times the value of this field in [ms]. When this field is 0, timer is disabled and t_{CUT} timer limits overloads' duration.	t_{LIM} Timer register, Ports 3 and 4, Read/Write	0	RW
			[7:4]	t_{LIM} timer for Port 4		0	RW
30	IP1LSB	8	[7:0]	Port 1 Current LSB. Read this byte before IP1MSB.	Port 1 Current Measurement, LSB register, Read Only. LSB = 122.07µA	0	RO

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Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
31	IP1MSB	8	[7:0]	Port 1 Current MSB.		0	RO
32	VP1LSB	8	[7:0]	Port 1 Voltage LSB. Read this byte before VP1MSB.	Port 1 Voltage Measurement, LSB register, Read Only. LSB = 5.835mV	0	RO
33	VP1MSB	8	[7:0]	Port 1 Voltage MSB.		0	RO
34	IP2LSB	8	[7:0]	Port 2 Current LSB. Read this byte before IP2MSB.	Port 2 Current Measurement, LSB register register, Read Only. LSB = 122.07µA	0	RO
35	IP2MSB	8	[7:0]	Port 3 Current MSB.		0	RO
36	VP2LSB	8	[7:0]	Port 2 Voltage LSB. Read this byte before VP2MSB.	Port 2 Voltage Measurement, LSB register, Read Only LSB = 5.835mV	0	RO
37	VP2MSB	8	[7:0]	Port 2 Voltage MSB.		0	RO
38	IP3LSB	8	[7:0]	Port 3 Current LSB. Read this byte before IP3MSB.	Port 3 Current Measurement, LSB register, Read Only LSB = 122.07µA	0	RO
39	IP3MSB	8	[7:0]	Port 3 Current MSB.		0	RO
3A	VP3LSB	8	[7:0]	Port 3 Voltage LSB. Read this byte before VP3MSB.	Port 3 Voltage Measurement, LSB register, Read Only LSB = 5.835mV	0	RO
3B	VP3MSB	8	[7:0]	Port 3 Voltage MSB.		0	RO
3C	IP4LSB	8	[7:0]	Port 4 Current LSB. Read this byte before IP4MSB.	Port 4 Current Measurement, LSB register, Read Only LSB = 122.07µA	0	RO
3D	IP4MSB	8	[7:0]	Port 4 Current MSB.		0	RO
3E	VP4LSB	8	[7:0]	Port 4 Voltage LSB. Read this byte before VP4MSB.	Port 4 Voltage Measurement, LSB register, Read Only LSB = 5.835mV	0	RO
3F	VP4MSB	8	[7:0]	Port 4 Voltage MSB.		0	RO
41	FIRMWARE	8	[7:0]		Firmware Revision register, Read Only	0A	RO
42	WDOG	8	[0]	Watchdog timer's status. When the watchdog times out this bit is set and all ports are reset. This bit must be cleared before any ports can be re-enabled		0	RW
			[4:1]	Watchdog Disable. Set this field to 1011b to disable watchdog; any other setting enables watchdog.		B	RW
			[5]	Reserved		0	RO
			[6]	Reserved		0	RO
			[7]	Thermal Shutdown. Same as bit 7 of register 0Bh except this bit stays set as long as over-temperature condition persists		0	RO
43	DEVID	8	[2:0]	MSCC specific device revision code	44 (HEX)	4	RO
			[4:3]	Reserved –always returns 0		0	RO
			[7:5]	MSCC specific identification code		2	RO
44	HPEN	4	[0]	Enables high power features on Port 1. When this bit is cleared high power disabled and registers 46h through 49h have no effect.	High Power Enable register, Read/Write. This register enables high power features controlled by registers 46h through 5Fh. If MODE1 is tied to GND then host	defined by MODE1 and CURRENT_SE	RW

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Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
					computer must write 0Fh to this register after power-up. '0' – High power disable '1' – High power enable	T pins	
			[1]	Enables high power features on Port 2. When this bit is cleared high power features are disabled and registers 4Bh through 4Eh have no effect.		defined by MODE1 and CURRENT_SET pins	RW
			[2]	Enables high power features on Port 3. When this bit is cleared high power features are disabled and registers 50h through 53h have no effect.		defined by MODE1 and CURRENT_SET pins	RW
			[3]	Enables high power features on Port 4. When this bit is cleared high power features are disabled and registers 55h through 58h have no effect.		defined by MODE1 and CURRENT_SET pins	RW
46	HPMD1	2	[0]	Enables 2-event (ping pong) classification on Port 1. '0' = disables 2-event classification '1' = enables 2-event classification	High Power Modes Port 1 register, Read/Write. This controls the high power modes on Port 1	1/0	RW
			[1]	Enables detection of legacy PDs by using a large cap as the detection signature. When this bit is set, a PD with large common-mode capacitance is reported as valid (code 4 in STATP1 register). '0' = disables large capacitor class '1' = enables large capacitor class **No MSCC CAP detection!** Note that IC does not comply with IEEE standard while this bit is set since IEEE specifically declares these legacy PDs to be invalid		0	RW
47	CUT1	8	[5:0]	Sets cutoff current threshold (I_{CUT}) on Port 1. Conversion scale is: 37.5mA/count when bit [6]=0; and 18.75mA/count when bit[6]=1.	Port 1 Over-Current Cutoff Level register, Read/Write	14	RW
			[6]	I_{CUT} is doubled when this bit is 0. 0 = I_{CUT} scale is 37.5mA/count 1 = I_{CUT} scale is 18.75mA/count		1/0	RW
			[7]	Sets current sense scale on Port 1. Always set this bit to 1.		1/0	RW
48	LIM1	8	[7:0]	Current limit and fold-back setting for port 1. When 80h -> set I_{lim} reference to AF When C0h -> take I_{lim} reference from I_LIM_AT_MAX register (9Bh)	Current Limit and Fold-back Control register for Port 1, Read/Write	80/0	RW
49	HPSTAT1	2	[0]	Set when 2-event (ping pong) classification has occurred. **– port is AT**	Status of High Power Features for Port 1, Read Only	0	RO
			[1]	When set, this bit indicates MOSFET for this port may have failed. Set according to analog FET temperature sensor. '0' – FET ok '1' – FET bad/overtemp		0	RO
4B	HPMD2	2	[0]	Enables 2-event (ping pong) classification on Port 2.	High Power Modes Port 2, Read/Write register. This	1/0	RW

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Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
				'0' = disables 2-event classification '1' = enables 2-event classification	register controls high power modes on Port 2		
			[1]	Enables detection of legacy PDs by using a large cap as a detection signature. When this bit is set, a PD with large common-mode capacitance is reported as valid (code 4 in the STATP2 register). '0' = disables large capacitor class '1' -=enables large capacitor class NOT MSCC CAP detection! Note that IC does not comply with IEEE standard while this bit is set since IEEE specifically declares these legacy PDs to be invalid		0	RW
4C	CUT2	8	[5:0]	Sets cutoff current threshold (I_{CUT}) on Port 2. Conversion scale is: 37.5mA/count when bit [6]=0; and 18.75mA/count when bit[6]=1.	Port 2 Over-current Cutoff Level register, Read/Write	14	RW
			[6]	I_{CUT} is doubled when this bit is 0. '0' = I_{CUT} scale is 37.5mA/count '1' = I_{CUT} scale is 18.75mA/count		1/0	RW
			[7]	Sets current sense scale on Port 2. Always set this bit to 1.		1/0	RW
4D	LIM2	8	[7:0]	Current limit and fold-back setting for port 2. When 80h -> set I_{lim} reference to AF When C0h -> take I_{lim} reference from I_LIM_AT_MAX register (9Bh)	Current Limit and Fold-back Control register for Port 2, Read/Write	80/0	RW
4E	HPSTAT2	2	[0]	Set when 2-event (ping pong) classification occurs. **Port is AT**	Status of High Power Features register for Port 2, Read Only	0	RO
			[1]	When set, this bit indicates MOSFET for this port may have failed. Set according to analog FET temperature sensor. '0' – FET ok '1' – FET bad/overtemp		0	RO
50	HPMD3	2	[0]	Enables 2-event (ping pong) classification on Port 3. '0' = Disables 2-event classification '1' = Enables 2-event classification	High Power Modes Port 3 register, Read/Write. This register controls the high power modes on Port 3	1/0	RW
			[1]	Enables detection of legacy PDs by using a large cap as a detection signature. When this bit is set, a PD with large common-mode capacitance is reported as valid (code 4 in STATP3 register). '0' = disables large capacitor class '1' =enables large capacitor class **No MSCC CAP detection!** Note that IC does not comply with IEEE standard while this bit is set since IEEE specifically declares these legacy PDs to be invalid		0	RW
51	CUT3	8	[5:0]	Sets cutoff current threshold (I_{CUT}) on Port 3. Conversion scale is: 37.5mA/count when bit [6]=0; and 18.75mA/count when bit[6]=1.	Port 3 Overcurrent Cutoff Level register, Read/Write	14	RW
			[6]	I_{CUT} is doubled when this bit is 0. '0' = I_{CUT} scale is 37.5mA/count '1' = I_{CUT} scale is 18.75mA/count		1/0	RW
			[7]	Sets current sense scale on Port 3. Always set this bit to 1.		1/0	RW
52	LIM3	8	[7:0]	Current limit and fold-back setting for port 3. When 80h -> set I_{lim} reference to AF When C0h -> take I_{lim} reference from	Current Limit and Fold-back Control register for Port 3, Read/Write	80/0	RW

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Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
				I_LIM_AT_MAX register (9Bh)			
53	HPSTAT3	2	[0]	Set when 2-event (ping pong) classification occurs. **Port is AT**	Status of High Power Features register for Port 3, Read Only	0	RO
			[1]	When set, this bit indicates the MOSFET for this port may have failed. Set according to analog FET temperature sensor. '0' – FET ok '1' – FET bad/overtemp		0	RO
55	HPMD4	2	[0]	Enables 2-event (ping pong) classification on Port 4. '0' = Disables 2-event classification '1' = Enables 2-event classification	High Power Modes register for Port 4, Read/Write. This register controls high power modes on Port 4	1/0	RW
			[1]	Enables detection of legacy PDs by using a large cap as a detection signature. When this bit is set, a PD with large common-mode capacitance is reported as valid (code 4 in STATP4 register). '0' = disable large capacitor class '1' = enable large capacitor class **No MSCC CAP detection!** Note that IC does not comply with IEEE standard while this bit is set since IEEE specifically declares these legacy PDs to be invalid		0	RW
56	CUT4	8	[5:0]	Sets cutoff current threshold (I_{CUT}) on Port 4. Conversion scale is: 37.5mA/count when bit [6]=0; and 18.75mA/count when bit[6]=1.	Port 4 Overcurrent Cutoff Level register, Read/Write	14	RW
			[6]	I_{CUT} is doubled when this bit is 0. '0' = I_{CUT} scale is 37.5mA/count '1' = I_{CUT} scale is 18.75mA/count		1/0	RW
			[7]	Sets current sense scale on Port 1. Always set this bit to 1.		1/0	RW
57	LIM4	8	[7:0]	Current limit and fold-back setting for port 4. When 80h -> set I_{lim} reference to AF When C0h -> take I_{lim} reference from I_LIM_AT_MAX register (9Bh)	Current Limit and Fold-back Control register for Port 4, Read/Write	80/0	RW
58	HPSTAT4	2	[0]	Set when 2-event (ping pong) classification has occurred. **Port is AT**	Status of High Power Features register for Port 4, Read Only	0	RO
			[1]	When set, this bit indicates MOSFET for this port may have failed. Set according to analog FET temperature sensor. '0' – FET ok '1' – FET bad/overtemp		0	RO

All register henceforth are relevant to MSCC Extended Auto mode ONLY							
70	VTEMP	8	[7:0]	Temperature Sensor Data	IC Junction Temperature Measurement register. IC temperature= ((VTEMP*0.96) - 27) deg Celsius If measurement is under -27deg Celsius reg. is 8'd0 Example: VTEMP=64HEX = 100 DEC Temp = 69 deg C		RO
71	VMAIN_LSB	8	[7:0]	V_{main} voltage measurement LSB. Read this byte before VMAIN_MSB.	V_{MAIN} Measurements register. Read Only. LSB = 5.835mV		RO

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Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
72	VMAIN_MSB	8	[7:0]	V_{main} voltage measurement MSB			RO
75	PORT_SR12	8	[0]	Port 1 MOSFET over temperature event. MOSFET turned off due to over temperature	Port1 and Port 2 Status register. Read Only.	0	RO
			[1]	Port 1 is OFF Due to PM		0	RO
			[2]	Port 1 passed MSCC cap detection		0	RO
			[3]	Port 1 failed in detection/class/startup		0	RO
			[4]	Port 2 MOSFET over-temperature event. MOSFET turned off due to over temperature		0	RO
			[5]	Port 2 is OFF Due to PM		0	RO
			[6]	Port 2 passed MSCC cap detection		0	RO
			[7]	Port 2 failed in detection/class/startup		0	RO
76	PORT_SR34	8	[0]	Port 3 MOSFET over temperature event. MOSFET turned off due to over temperature	Port3 and port 4 status register. Read Only.	0	RO
			[1]	Port 3 is OFF Due to PM		0	RO
			[2]	Port 3 passed MSCC cap detection		0	RO
			[3]	Port 3 failed in detection/class/startup		0	RO
			[4]	Port 4 MOSFET over temperature event. MOSFET turned off due to over temperature		0	RO
			[5]	Port 4 is OFF Due to PM		0	RO
			[6]	Port 4 passed MSCC cap detection		0	RO
			[7]	Port 4 failed in detection/class/startup		0	RO
77	INVD_CNT	8	[1:0]	Port 1 invalid detection counter - wrap around (cyclic) counter	Invalid Detection Counter register. Read Only.	0	RO
			[3:2]	Port 2 invalid detection counter		0	RO
			[5:4]	Port 3 invalid detection counter		0	RO
			[7:6]	Port 4 invalid detection counter		0	RO
78	PWRD_CNT	8	[1:0]	Port 1 power denied counter	Power Denied Counter register. Read Only.	0	RO
			[3:2]	Port 2 power denied counter		0	RO
			[5:4]	Port 3 power denied counter		0	RO
			[7:6]	Port 4 power denied counter		0	RO
79	OVL_CNT	8	[1:0]	Port 1 overload event counter	Overload Event Counter register. Read Only.	0	RO
			[3:2]	Port 2 overload event counter		0	RO
			[5:4]	Port 3 overload event counter		0	RO
			[7:6]	Port 4 overload event counter		0	RO
7A	UDL_CNT	8	[1:0]	Port 1 under-load event counter	Under-load Event Counter register. Read Only.	0	RO
			[3:2]	Port 2 under-load event counter		0	RO
			[5:4]	Port 3 under-load event counter		0	RO
			[7:6]	Port 4 under-load event counter		0	RO
7B	SC_CNT	8	[1:0]	Port 1 short circuit event counter	Short Circuit Event Counter register. Read Only.	0	RO
			[3:2]	Port 2 short circuit event counter		0	RO
			[5:4]	Port 3 short circuit event counter		0	RO
			[7:6]	Port 4 short circuit event counter		0	RO
7C	CLS_CNT	8	[1:0]	Port 1 class error event counter	Class Error Event Counter register. Read Only.	0	RO
			[3:2]	Port 2 class error event counter		0	RO

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Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
			[5:4]	Port 3 class error event counter		0	RO
			[7:6]	Port 4 class error event counter		0	RO
7D	INTR_EN	1	[0]	1=pin "res_cap_int_out" is set to use as INT_OUT output 0=pin "res_cap_int_out" is set to use as RES_CAP input	Interrupt Enable register. Read/Write.	0	RW
7E	SYS_CFG	8	[0]	MSCC capacitor detection enable for all ports. Default value is Cap pin state. '1' – Resistor detection only '0' – Resistor & legacy detection	System Configuration register. Read/Write.	According to RES_CAP pin	RW
			[2:1]	Reserved		0	RW
			[3]	Reserved – Should be set to "1"		1	RW
			[4]	Set PS_PG pin source or communication '0' – PS_PG state is set only by PS_PG[3:0] pins '1' – PS_PG state is set by communication (see Address 91)		0	RW
			[5]	Communication protocol select Set according to COMM_MODE pin state (Software Overwrite Pin Level) '1' – I2C (*) '0' – UART (*)		defined by COMM_MODE pin	RW
			[6]	Pin PS_PG3 pin state overwrite '1' – PS_PG3 pin is '1' (*) '0' – PS_PG3 pin is '0' (*)		defined by PGD3 pin	RW
			[7]	Set ports startup current limit to AF (IEEE standard compliant) or set startup current limit at startup to high current (not compliant with IEEE standard) '0' – i_{lim} AF during startup '1'– i_{lim} AT during startup		0	RW
7F	SW_CFG	8	[0]	Define whether to set I_{cut} level to maximum or calculate it according to TPPL (registers 85h to 88h) '0' – Set I_{cut} according to TPPL '1' – Set I_{cut} to max according to ICUT_AT_MAX registers (99h and 9Ah)	IC Port Behavior Configuration register. Read/Write.	1	RW
			[1]	Set calculation method of power management '0' – Static (according to class or PPL) '1' – Dynamic (according to real port consumption)		1	RW
			[2]	When class 0 is detected enable high power port. In Auto mode and Semi-Auto mode reset value is 1. In MSCC Extended Auto mode reset value is 0. '0' – Class 0 is detected as high power (*) '1' – Class 0 is detected as AF (*)		defined by operation mode	RW
			[3]	When port is set to be high power enable class 123 as high power. In Auto mode and Semi-Auto mode reset value is 1. In MSCC Extended Auto mode reset value is 0. '0' – Class 123 detected as high power (*) '1' – Class 123 detected as AF (*)		defined by operation mode	RW

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Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
			[4]	Class error configuration bit. If the result of the second class event is not equal to the first event then fail the detection or set is as valid detection. '0' – Two different results are invalid '1' – Two different results are valid		0	RW
			[6:5]	If class current is higher than class 4 limit set class result as either error, class0 or class4. 00/11 – Set class as error 10 – Set high current class as class 0 01 – Set high current class as class 4		0	RW
						0	RW
			[7]	When startup power is not enough for current port, check whether the following ports can be started up or mark them all as PM '0' – Don't try to start the following ports '1' – Check whether startup power is enough for lower priority ports		1	RW
80	PRIO_CR	8	[1:0]	Port 1 priority 0 – High priority 1 – Medium priority 2 – Low priority	Port Priority register. Read/Write. Port priority will determine ports disconnection order in case of a PM event. Ports with same priority will disconnect according to position order.	2	RW
			[3:2]	Port 2 priority 0 – High priority 1 – Medium priority 2 – Low priority		2	RW
			[5:4]	Port 3 priority 0 – High priority 1 – Medium priority 2 – Low priority.		2	RW
			[7:6]	Port 4 priority 0 – High priority 1 – Medium priority 2 – Low priority		2	RW
81	PWR_CR1	6	[5:0]	Port 1 Power Allocation Limit (PPL). Reset value set according to CURRENT SET pin DVDD – 44W Open – 36W GND – 20W	Port 1 Power Allocation Limit register for PM Mechanism. Read/Write. A port that exceeds this power level when power budget is limited will be disconnected due to power management. LSB = 1W	defined by CURRENT_SET pin	RW
82	PWR_CR2	6	[5:0]	Port 2 Power Allocation Limit (PPL). Reset value set according to CURRENT SET pin DVDD – 44W Open – 36W GND – 20W	Port 2 Power Allocation Limit register for the PM Mechanism. Read/Write. A port that exceeds this power level when power budget is limited will be disconnected due to power management. LSB = 1W	defined by CURRENT_SET pin	RW
83	PWR_CR3	6	[5:0]	Port 3 Power Allocation Limit (PPL). Reset value set according to CURRENT SET pin DVDD – 44W Open – 36W GND – 20W	Port 3 Power Allocation Limit register for the PM Mechanism. Read/Write. A port that exceeds this power level when power budget is limited will be disconnected due to power management. LSB = 1W	defined by CURRENT_SET pin	RW
84	PWR_CR4	6	[5:0]	Port 4 Power Allocation Limit (PPL). Reset value set according to CURRENT SET pin DVDD – 44W Open – 36W GND – 20W	Port 4 Power Allocation Limit register for the PM Mechanism. Read/Write. A port that exceeds this power level when power budget is	defined by CURRENT_SET pin	RW

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Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
					limited will be disconnected due to power management. LSB = 1W		
85	TMP_PWR_CR1	6	[5:0]	Port 1 Temporary Port Power Allocation Limit (TPPL - for layer 2 LLDP support)	Port 1 Temporary Port Power Allocation Limit register for Layer 2 Classification Support. Read/Write. These registers can be used by an external CPU (host) for setting port power allocation for Power Management Mechanism. A port that exceeds this power level when power budget is limited might be disconnected due to power management. LSB = 1W	0	RW
86	TMP_PWR_CR2	6	[5:0]	Port 2 Temporary Port Power Allocation Limit (TPPL - for layer 2 LLDP support)	Port 2 Temporary Port Power Allocation Limit register for Layer 2 Classification Support. Read/Write. These registers can be used by an external CPU (host) for setting port power allocation for Power Management Mechanism. A port that exceeds this power level when power budget is limited might be disconnected due to power management. LSB = 1W	0	RW
87	TMP_PWR_CR3	6	[5:0]	Port 3 Temporary Port Power Allocation Limit (TPPL - for layer 2 LLDP support)	Port 3 Temporary Port Power Allocation Limit register for Layer 2 Classification Support. Read/Write. These registers can be used by an external CPU (host) for setting port power allocation for Power Management Mechanism. A port that exceeds this power level when power budget is limited might be disconnected due to power management. LSB = 1W	0	RW
88	TMP_PWR_CR4	6	[5:0]	Port 4 Temporary Port Power Allocation Limit (TPPL - for layer 2 LLDP support)	Port 4 Temporary Port Power Allocation Limit register for Layer 2 Classification Support. Read/Write. These registers can be used by an external CPU (host) for setting port power allocation for Power Management Mechanism. A port that exceeds this power level when power budget is limited might be disconnected due to power management.	0	RW

Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
					LSB = 1W		
89	PWR_BNK0	8	[7:0]	System power budget for state 0 of PGD[2:0] lines. Reset value set according to CURRENT_SET pin: DVDD – 176W Open – 144W GND – 144W	Power Bank 0 Set register Read/Write. LSB = 1W Register Value = B0 (HEX) for 176w 90 (HEX) for 144w	defined by CURRENT_SET pin	RW
8A	PWR_BNK1	8	[7:0]	System power budget for state 1 of PGD[2:0] lines. Power budget for bank 1	Power Bank 1 Set register Read/Write. LSB = 1W	8C	RW
8B	PWR_BNK2	8	[7:0]	System power budget for state 2 of PGD[2:0] lines. Power budget for bank 2	Power Bank 2 Set register Read/Write. LSB = 1W	88	RW
8C	PWR_BNK3	8	[7:0]	System power budget for state 3 of PGD[2:0] lines Power budget for bank 3	Power Bank 3 Set register Read/Write. LSB = 1W	84	RW
8D	PWR_BNK4	8	[7:0]	System power budget for state 4 of PGD[2:0] lines Power budget for bank 4	Power Bank 4 Set register Read/Write. LSB = 1W	80	RW
8E	PWR_BNK5	8	[7:0]	System power budget for state 5 of PGD[2:0] lines Power budget for bank 5	Power Bank 5 Set register Read/Write. LSB = 1W	7C	RW
8F	PWR_BNK6	8	[7:0]	System power budget for state 6 of PGD[2:0] lines Power budget for bank 6	Power Bank 6 Set register Read/Write. LSB = 1W	78	RW
90	PWR_BNK7	8	[7:0]	System power budget for state 7 of PGD[2:0] lines power budget for bank 7	Power Bank 7 Set register Read/Write. LSB = 1W	74	RW
91	PWRGD	7	[2:0]	Power Good actual status - according to communication or PS_PG pins status.	Power Good Status register. Read/Write.	0	RW
			[6:3]	Power Supply Power Good pins 0 to3 status	Power Supply Power Good Pins Status register. Read Only	PS_PG [3:0]	RO
92	PORT1_CONS	6	[5:0]	Port 1 power consumption calculation Calculated according to $I_{port} * V_{port}$	Port 1 Real Power Consumption register. Read Only. LSB = 1W	0	RO
93	PORT2_CONS	6	[5:0]	Port 2 power consumption calculation Calculated based on $I_{port} * V_{port}$	Port 2 Real Power Consumption register. Read Only. LSB = 1W	0	RO
94	PORT3_CONS	6	[5:0]	Port 3 power consumption calculation Calculated according to $I_{port} * V_{port}$	Port 3 Real Power Consumption register. Read Only. LSB = 1W	0	RO
95	PORT4_CONS	6	[5:0]	Port 4 power consumption calculation Calculated according to $I_{port} * V_{port}$	Port 4 Real Power Consumption register. Read Only. LSB = 1W	0	RO
96	TOTAL_PWR_CONS	8	[7:0]	IC ports total power consumption	Ports Total Power Consumption register. Read Only. LSB = 1W	0	RO
97	TOTAL_PWR_CALC	8	[7:0]	Total calculated ports power – according to TPPL sum	Ports Total Power Calculation based on TPPL Register. Read Only. LSB = 1W	0	RO
98	CHIP_PWR_REQ	8	[7:0]	Total power requested – sum of power requested from ports after detection and before startup	IC Power Request register for External Power Management. Read Only. LSB = 1W	0	RO

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Address (HEX)	Register Name	Width	Bits	Detailed Description	General/Equation	Reset Value (HEX)	Read / Write
99	ICUT_AT_MAX_LSB	8	[7:0]	Sets maximum cutoff current threshold (I_{CUT}) together with ICUT_AT_MAX_MSB register (9Ah) Reset value is set by CURRENT_SET pin. 'GND' – 375mA 'Open' – 643mA. DVDD-771mA.	I_{CUT} Maximum Current Setting register. Read/Write. LSB = 122.07µA	defined by CURRENT_SET pin	RW
9A	ICUT_AT_MAX_MSB	8	[7:0]	Sets maximum cutoff current threshold (I_{CUT}).together with ICUT_AT_MAX_LSB register (99h) Reset value is set by CURRENT_SET pin. 'GND' – 375mA 'Open' – 643mA. DVDD – 771mA.	I_{CUT} Maximum Current Setting register. Read/Write. LSB = 122.07µA	defined by CURRENT_SET pin	RW
9F	POE_MAX_LED_GB	6	[5:0]	If (budget - consumption) < POE_MAX_LED_GB led will turn on LED OFF – consumption is below guard band LED ON - consumption is below budget and above guard band LED BLINK – consumption is above the budget	POE_MAX LED Guard Band Setting register. Read/Write. LSB = 1W	0F	RW
CB	VMAIN_LOW_TH_LSB	8	[7:0]	Sets V_{MAIN} low threshold together with VMAIN_LOW_TH_MSB register (CCh) Reset value is 40V.	V_{MAIN} Low Threshold Setting register. Read/Write LSB = 0.186V	D7	RW
CC	VMAIN_LOW_TH_MSB	3	[2:0]	Sets V_{MAIN} low threshold together with VMAIN_LOW_TH_LSB register (CBh) Reset value is 40V.	V_{MAIN} Low Threshold Setting register. Read/Write LSB = 0.186V	0	RW

(*) Writing to this Bit Overwrites Hardware Pin Pre-Settings

R/W ACCESS KEY:

COR Clear on Read. Register clears when read. Writing to these registers has no effect.
R/W Read/Write. Register can be read or write
RO Read Only. Register can be read only. Writing to these registers has no effect.
SO Set Only. Writing “1” - set the bit, Writing “0” – bit is unchanged (Data read from these registers is meaningless)

In the RESET state column, reset state for the STATPIN register (11h) is 00WXYZ00 where:
W=the state of the ADDR3 pin;
X=the state of the ADDR2 pin;
YZ=00 for ports A-D;
YZ=01 for ports E-H;
YZ=10 for ports I-L;
YZ=11 for ports M-P.

The following Registers are designed to be Set by External EPROM upon Power Up Sequence:

Address 44, 46, 4B, 50, 55, 6F, 7D, 7E, 7F, 80 to 90, 99 to 9F,

Revision History

Revision Level / Date	Description
0.1 / Nov. 2010	Initial Release
0.2 / Dec. 2010	Update registers description
0.3 / Jan. 2011	Update
0.4 / Dec. 2011	Adding Registers Description per Customer Care Requests
0.5 / Dec. 2011	Change Power Supply Power Good Pins Names

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