DS0130
Datasheet
RTG4 FPGA Pin Descriptions

a Microchip company

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 7.0

The following is a summary of the changes in revision 7.0 of this document.

- Information about JTAG_TCK pin was updated. See Table 6, page 8.
- Information about SPI slave programming was removed.
- Information about RTG4 Naming convention was updated. See Naming Convention, page 4.
- Information about DEVRST_N pin description was updated. See Special Pins, page 9.
- Information about Unused global pins was updated. See Dedicated Global I/O Naming Convention, page 4.
- Information about CQ352 I/O Bank Locations was added. See Figure 2, page 3.

1.2 Revision 6.0

Re-organized the placement of I/O banks. For more information, see Figure 1, page 2.

1.3 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Updated placement of SerDes blocks. For more information, see Figure 1, page 2.
- Replaced DDR and DDR1 with LPDDR. For more information, see Table 1, page 3.
- Added VDD_MONITOR and VSS_MONITOR pin details. For more information, see Table 8, page 9.
- Added SerDes ESD support information. For more information, see SerDes I/Os, page 9.
- Added SerDes RXD pads information. For more information, see SerDes I/Os, page 9.

1.4 Revision 4.0

Updated PROBE_READ_DATA and PROBE_CAPTURE port name description in Table 8, page 9.

1.5 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- Updated Dedicated Global I/O Naming Convention, page 4.
- Updated Fabric DDR Interface, page 4 (SAR 73567).
- Updated Table 5, page 7 (SAR 75640).
- Updated Table 8, page 9 (SAR 71145).

1.6 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Updated Bank Location Diagrams, page 2
- Updated Dedicated Global I/O Naming Convention, page 4 (SAR 70427).
- Updated FDDR Controller Pins, page 5
- Updated SpaceWire Interface, page 6
- Updated Supply Pins, page 7 (SAR 66310).
- Updated JTAG Pins, page 8
- Updated SerDes I/Os, page 9 (SAR 65805)
- Updated Special Pins, page 9

1.7 Revision 1.0

Revision 1.0 was the first publication of this document.

2 RTG4 FPGA Pin Descriptions

2.1 User I/Os

The RTG4™ field programmable gate array (FPGA) devices have different types of I/O structures that support a range of mixed voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V) through I/O bank selection. The MSIO and MSIOD can be configured as differential I/Os or single-ended I/Os. The DDRIOs do not support true differential outputs. All these I/Os use one pin to implement single-ended standards and two pins for differential standards.

For functional block diagrams of MSIO, MSIOD, and DDRIO, refer to the *UG0574: RTG4 FPGA Fabric User Guide*.

2.2 Bank Location Diagrams

I/Os are grouped based on the I/O voltage standard. The grouped I/Os of each voltage standard form an I/O bank. Each I/O bank has dedicated I/O supply and ground voltages. Therefore, only buffer types with compatible standards can be assigned to the same I/O voltage bank.

The following figure shows the bank locations of RT4G150-CG1657.

Figure 1 • **RT4G150-CG1657 I/O Bank Locations—Bottom View**

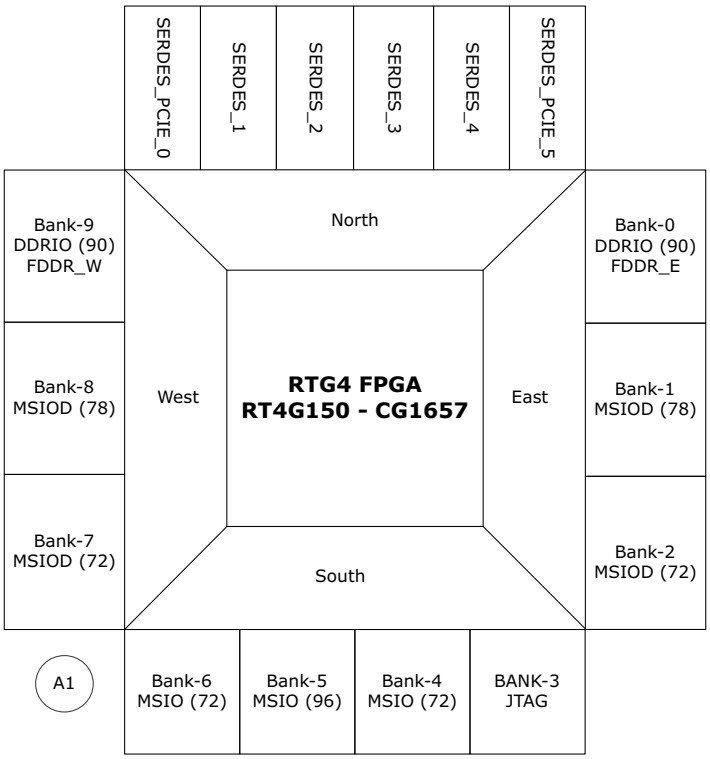
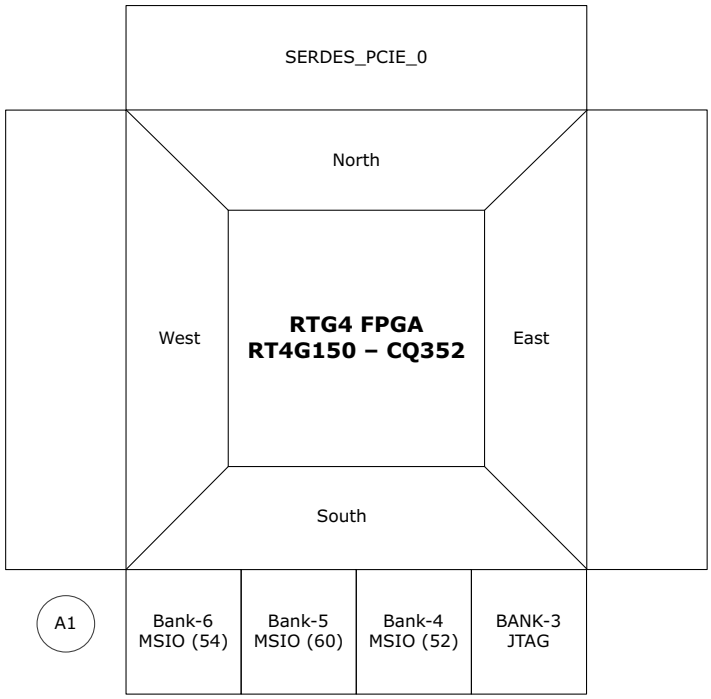


Figure 2 • **RT4G150-CQ352 I/O Bank Locations—Bottom View**



The following table describes the types of multi-standard I/Os.

Table 1 • **Multi-Standard I/O Types**

Name	Type	Description
MSIOxyBz	Input/Output	MSIOs provide programmable drive strength, weak pull-up, and weak-pull-down. In single-ended mode, the I/O pair operates as two separate I/Os named P and N (described in the y field of the naming convention). The RTG4 MSIO include ESD protection. MSIO I/O cells operate at up to 3.3 V and are capable of LVDS operation. MSIOs do not support a user programmable slew rate.
MSIODxyBz	Input/Output	Similar to MSIO, but operates only up to 2.5 V, and adds pre-emphasis, to achieve higher speeds. MSIODs provide programmable drive strength, weak pull-up, and weak pull-down. MSIOD I/Os are capable of high-speed LVDS2V5 operation and include ESD protection. MSIODs do not support a user programmable slew rate and have pre-emphasis on the differential output.
DDRIOxyBz	Input/Output	The double data rate input output (DDRIO) is a multi-standard I/O optimized for LPDDR/DDR2/DDR3 performance. These I/Os also operate up to 2.5 V like MSIOD. They have ESD protection. If the FDDR interface block is utilized, the Libero® System-on-Chip (SoC) software automatically connects the FDDR signals to the DDRIOs. Depending on the memory configuration, Libero uses the required DDRIOs. Unused DDRIOs are available to access the FPGA fabric. DDRIOs support programmable slew control on the non-differential drive outputs.

For information about hot-swap and cold-spare applications, refer to the *UG0574: RTG4 FPGA Fabric User Guide*.

For information about I/O utilization of the RTG4 device corresponding to the supported DDR bus widths, refer to I/O Utilization for RTG4 Devices table of the *UG0573: RTG4 FPGA High Speed DDR Interfaces User Guide*.

2.3 Naming Convention

2.3.1 User I/O Naming Convention

The naming convention used for FPGA user I/O is IOxyBz, where:

- IO: Type of I/O—MSIO, MSIOD, or DDRIO.
- x: I/O pair number in bank z.
- y: P (positive) or N (negative).
  In single-ended mode, the I/O pair operates as two separate I/Os named P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O.
- B: Bank.
- z: Bank number (0-9 for RT4G150-CG1657).

Differential I/O standards are implemented as true differential outputs and complementary single-ended outputs for stub series terminated logic (SSTL) or high speed transceiver logic (HSTL). In single-ended mode, the I/O pair operates as two separate I/Os named P and N. All the configurations and data inputs/outputs are different and use names ending with P and N to differentiate between the two I/Os.

For more information about I/Os, refer to the I/Os chapter of the *UG0574: RTG4 FPGA Fabric User Guide*.

2.3.2 Dedicated Global I/O Naming Convention

Dedicated global I/Os are dual-use I/Os, which can drive the global blocks directly or through clock conditioning circuits (CCC). They can also be used as regular user I/Os. These global I/Os are the primary source to bring external clock inputs into the RTG4 device. Unused global pins are configured as inputs with pull-up resistors by the Libero software.

The RTG4 devices have 36 I/Os which are dedicated for global clocks. Out of these 36 global clocks, 12 are dedicated for SerDes clocks.

Dedicated global I/Os that drive the global blocks (GB) directly are named as **GBx**, where x is 0 to 23.

Dedicated global I/Os that drive GBs through CCCs are named **CCC_xyz_CLKIw**, where:

- **xy**: Individual CCC block located at specific chip corner NE, SE, SW, or NW.
- **z**: CCC number (0 or 1) for the corresponding corner (NE, SE, SW, or NW) of the RTG4 device.
- **I**: Input clock.
- **w**: Four dedicated global inputs (0, 1, 2, or 3) of the associated CCC_xyz_CLKI.

Unused pins (including dual-use globals) have input and output buffers tri-stated, weak pull-up enabled.

For more information on Global I/Os, refer to the Fabric Global Routing Resources chapter of the *UG0586: RTG4 FPGA Clocking Resources User Guide*.

For example, MSIOD168PB8/GB0_11/CCC_NW1_CLKI2/SPWR_NW1_1_RX_STROBE_P pin can be used as any of the functions listed:

- GB global input buffer (driving clocks, very high-fanout data signals, or resets)
- Regular user I/O (driving regular routing to fabric resources)
- CCC CLKI2 input clock (driving CCC reference clocks)
- SpaceWire Strobe input (driving CCC clock recovery circuit)

GRESET generates a global asynchronous reset signal during power-up / programming, and allows the user to apply an asynchronous reset on the fabric flip-flops globally if required. For more information on GREST, refer to the *UG0574: RTG4 FPGA Fabric User Guide*.

2.4 Fabric DDR Interface

The RTG4 devices have two FDDR blocks. The FDDR subsystem is a hardened ASIC block for interfacing the LPDDR, DDR2, and DDR3 memories. It supports 8/16/32-bit data bus width modes. The DDRIO uses fixed impedance calibration for different drive strengths. These values can be programmed using Libero SoC software for the selected I/O standard. The values are fed to the pull-up/pull-down reference network to match the impedance with an external resistor. For more information about

reference resistor values (for different drive modes), refer to the *UG0574: RTG4 FPGA Fabric User Guide*.

2.4.1 FDDR Controller Pins

The following figure shows the FDDR controller pins.

Table 2 • **FDDR Controller Pins**

Pin Name	Type	Reference Resistor (Ω)
FDDR_x_CAS_N	Output	DRAM CASN.
FDDR_x_CKE	Output	DRAM CKE.
FDDR_x_CLK	Output	DRAM single-ended clock for differential pads.
FDDR_x_CLK_N	Output	DRAM single-ended clock for differential pads.
FDDR_x_CS_N	Output	DRAM CSN.
FDDR_x_ODT	Output	DRAM on-die termination (ODT). 0: Termination Off 1: Termination On
FDDR_x_RAS_N	Output	DRAM RASN.
FDDR_x_RESET_N	Output	DRAM reset for DDR3.
FDDR_x_WE_N	Output	DRAM WEN.
FDDR_x_ADDR[15:0]	Output	DRAM address bits.
FDDR_x_BA[2:0]	Output	DRAM bank address.
FDDR_x_DM_RDQS[3:0]	Input/Output	DRAM data mask from bidirectional pads.
FDDR_x_DQS[3:0]	Input/Output	DRAM single-ended data strobe output for bidirectional pads.
FDDR_x_DQS[3:0]_N	Input/Output	DRAM single-ended data strobe output for bidirectional pads.
FDDR_x_DQ[31:0]	Input/Output	DRAM data input or output for bidirectional pads.
FDDR_x_DQ_ECC[3:0]	Input/Output	DRAM data input or output for SECDED.
FDDR_x_DM_RDQS_ECC	Input/Output	DRAM single-ended data strobe output for bidirectional pads.
FDDR_x_DQS_ECC	Input/Output	DRAM single-ended data strobe output for bidirectional pads.
FDDR_x_DQS_ECC_N	Input/Output	DRAM data input or output for bidirectional pads.
FDDR_x_TMATCH_[0/1]_IN	Input	DQS enable input for timing match between DQS and system clock. For simulations, tie to FDDR_x_TMATCH_[0/1]_OUT.
FDDR_x_TMATCH_[0/1]_OUT	Output	DQS enable output for timing match between DQS and system clock. For simulations, tie to FDDR_x_TMATCH_[0/1]_IN.
FDDR_x_TMATCH_ECC_[IN]	Input	DQS enable input for timing match between DQS and system clock. For simulations, tie to FDDR_x_TMATCH_ECC_[OUT].
FDDR_x_TMATCH_ECC_[OUT]	Output	DQS enable output for timing match between DQS and system clock. For simulations, tie to FDDR_x_TMATCH_ECC_[IN].
FDDR_x_IMP_CALIB	Ref	Pull-down with resistor depending on voltage/standard: DDR2 - 150 Ω DDR3 (1.5 V) - 240 Ω LPDDR - 150 Ω Here, x represents East or West.
FDDR_x_RESERVED		For FDDR0, the reserved pin (bank0) is AK35. For FDDR1, the reserved pin (bank9) is AK7.

Table 2 • **FDDR Controller Pins *(continued)***

Pin Name	Type	Reference Resistor (Ω)
FDDR_x_RESERVED_8_16		In 18-bit, 16-bit, 9-bit, 8-bit DDR bus width modes, five additional pins are reserved. For FDDR0 the reserved pins (bank0) are AK35, AJ31, AK32, AK33, AL35. For FDDR1 the reserved pins (bank9) are AK7, J11, AK9, AK10, AL7.

Note: Though calibration is not required, it is recommended to use the corresponding resistor placeholder to connect the FDDR_x_IMP_CALIB to the ground with or without a resistor. x represents East or West.

For more information about FDDR memory configurations, refer to the *UG0573: RTG4 FPGA High Speed DDR Interfaces User Guide*.

If FDDR is not used, the Libero SoC v11.7 software connects the unused FDDR blocks by adding CFG0 instances and nets to user netlist. You cannot use AL2, AE1, AE41, and AL40 pins with **OUT_REG** or **EN_REG** macros.

2.4.2 I/O Standards

The following table shows the supported I/O standards for different DDR memories.

Table 3 • **Supported I/O Standards for Different DDR Memories**

Memory Type	I/O Standard
DDR3	SSTL15I, SSTL15II
DDR2	SSTL18I, SSTL18II
LPDDR	LVCMOS18

2.5 SpaceWire Interface

SpaceWire is a standard for high-speed point-to-point data links with the following characteristics:

- Operation between 2 Mbps and 400 Mbps.
- Capable of full duplex operation.

In the RTG4 device, only the receiving Clock Recovery blocks are implemented in silicon (in the CCC block). The rest of the SpaceWire IP can be acquired from third-party vendors and implemented as soft IP in the FPGA fabric. Each CCC block has two Clock and Data Recovery blocks.

The SpaceWire clocks are generated from external Data and Strobe I/O pins.

The following table describes the SpaceWire pins.

Table 4 • **SpaceWire Pins**

Pin Name	Description
SPWR_xyz_w_RX_STROBE_[P/N]	Differential Input Strobe signal from I/O pad.
SPWR_xyz_w_RX_DATA_[P/N]	Differential Input Data signal from I/O pad.

Note: **xy** represents individual SpaceWire block located at specific chip corner—NE, SE, SW, or NW.

Note: **z** is CCC number of either 0 or 1 for the corresponding corner of the RTG4 chip.

Note: **w** refers to one of the two possible input pins associated with SPWR_xyz_[0,1].

2.6 Supply Pins

The RTG4 device supports MSIOs, MSIODs, DDRIOs, high speed serial interfaces, SpaceWire interface and a debugging JTAG interface. It requires the power supplies listed in the following table.

Table 5 • **Supply Pins**

Name	Operating Voltage	Description
VDD	1.2 V	DC core supply voltage. Must always power this pin.
VPP	3.3 V	Power supply for charge pumps (for normal operation and programming). Must always power this pin.
VDDIx where x is the bank number	1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V	I/O bank supplies for MSIO, MSIOD and DDRIO banks. For MSIO banks: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V For MSIOD banks: 1.2 V, 1.5 V, 1.8 V, 2.5 V For DDRIO banks: 1.2 V, 1.5 V, 1.8 V, 2.5 V For JTAG bank: 1.8 V, 2.5 V, or 3.3 V To power-up the device, all I/O banks must be powered (to exit from power-on-reset state). There is no power-up sequence requirement between VDDI, VPP, and VDD supplies.
VDDPLL	3.3 V	Power for Eight corner PLLs, PLLs in SerDes PCIe/PCS blocks, and FDDR PLL. When in use, the supply must be connected to a common PLL supply (3.3 V) of the corresponding PLL return path (VSS) on-board through an RC filter. When not in use, the supply must be directly connected to 3.3 V (without the filter circuit).
VREF0 VERF9	0.5 * VDDI	Reference voltage for FDDR signals. Reference voltages must be powered with the appropriate bank supplies through voltage divider circuitry. If I/O banks are used as single-ended I/Os (and FDDR functionalities are not used), VREF0, VREF9 can be left floating (DNC).
SERDES_x_Lyz_VDDAIO where, – x refers to 1, 2, 3, 4, PCIE_0 or PCIE_5 – yz refers to lanes 0 and 1, or lanes 2 and 3	1.2 V	TX/RX analog I/O voltage for SerDes lanes. Low voltage power for Lane-y and Lane-z of SERDES_x. All of the nominal 1.2 V power supply pins for the SerDes block such as SERDES_x_Lyz_VDDAIO are driven from the same supply as the FPGA core (VDD) supply. If SerDes is not used, it must be connected to 1.2 V (VDD).
SERDES_x_Lyz_VDDAPLL where, – x refers to 1, 2, 3, 4, PCIE_0 or PCIE_5 – yz refers to lanes 0 and 1, or lanes 2 and 3	2.5 V	Analog power for SerDes lanes. If SerDes is used, all SerDes PLL pins must be connected to the appropriate supply (2.5 V) of the corresponding return path on-board (SERDES_x_Lyz_REFRET) through an RC filter. If SerDes is not used, they must connect directly to 2.5 V or 1.2 V without the RC filter circuit.
SERDES_x_Lyz_REFRET where, – x refers to 1, 2, 3, 4, PCIE_0 or PCIE_5 – yz refers to lanes 0 and 1, or lanes 2 and 3		Local on-chip ground return path for SerDes lanes. If SerDes is not used, it must be grounded (VSS).

Table 5 • **Supply Pins *(continued)***

Name	Operating Voltage	Description
SERDES_x_Lyz_REXT where, – x refers to 1, 2, 3, 4, PCIE_0 or PCIE_5 – yz refers to lanes 0 and 1, or lanes 2 and 3		External reference resistor (1.21 kΩ) connected to calibrate TX/RX termination value. Each SERDES_x consists of two REXT signals—one for Lane0 and Lane1, and another for Lane2 and Lane3. If the SerDes is not used, it must remain floating (DNC).
SERDES_VDDI	1.8 V, 2.5 V, or 3.3 V	Power for SerDes reference clock receiver supply. The supply voltage depends on SerDes reference clock source. Must always power this pin.
SERDES_VREF	0.5 * SERDES_VDDI	External differential receiver reference voltage for SerDes Reference Clocks. Reference voltage must be powered with the SERDES_VDDI supply through voltage divider circuitry. If SerDes reference clock uses an I/O reference standard such as SSTL, HSTL on the board, SERDES_VREF must be connected to SERDES_VDDI through a voltage divider circuit. If SerDes is not used or SerDes reference clock uses a non reference standard such as LVDS, LVCMOS, and LVTTL on the board, SERDES_VREF must be connected to Ground through a 1 k–10 kΩ resistor.
VSS	Ground	Ground pad for core and I/Os. Always connect to ground.

2.7 JTAG Pins

JTAG pins can operate at 1.8 V/2.5 V/3.3 V (nominal).

Table 6 • **JTAG Pin Names and Descriptions**

Name	Type	Description
JTAG_TCK	Input	Test clock. Serial input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/pull-down resistor. For used condition, connect 1 K to GND. For unused condition, connect either VDDI3 or VSS through resistor (200 Ω to 1 KΩ).
JTAG_TDI	Input	Test data in. Serial input for JTAG boundary scan. There is an internal weak pull-up resistor on the TDI pin.
JTAG_TDO	Output	Test data out. Serial output for JTAG boundary scan. The TDO pin does not have an internal pull-up/pull-down resistor.
JTAG_TMS	Input	Test mode select. The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, and TRST). There is an internal weak pull-up resistor on the TMS pin.
JTAG_TRSTB	Input	Test reset. The TRSTB pin is an active low input. It asynchronously initializes (or resets) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRSTB pin. To hold the JTAG in reset mode and prevent it from entering into undesired states in critical applications, connect TRSTB to GND through a 1 kΩ resistor (placed close to the FPGA pin).

2.8 SerDes I/Os

The SerDes I/Os available in the RTG4 device are dedicated for high speed serial communication protocols. The SerDes I/Os support protocols such as PCIe Gen1, XAUI, serial giga-bit media independent interface (SGMII), EPCS, serial rapid I/O (SRIO), and user-defined high speed serial protocol implementations in the fabric. The RTG4 SerDes I/Os include ESD protection.

The following table lists the SerDes I/O pins.

Table 7 • **SerDes I/O Pins**

Port Name	Type	Description
SERDES_x_RXDy_P/N where, – x refers to 1, 2, 3, 4, PCIE_0 or PCIE_5 – y refers to 0, 1, 2 or 3	Input	SerDes differential positive/negative input. Each SerDes interface consists of four receiving differential RXD signals. If SerDes is not used, it must be connected to VSS through a 1 k–10 kΩ resistor. If the board space is a constraint, you can group up to eight RXD pads to an external 10 kΩ pull-down resistor. Due to reliability issues, you must not connect RXD pads to VSS directly.
SERDES_x_TXDy_P/N where, – x refers to 1, 2, 3, 4, PCIE_0 or PCIE_5 – y refers to 0, 1, 2 or 3	Output	SerDes differential positive/negative output. Each SerDes interface consists of four transmitting differential TXD signals. If SerDes is not used, it must be floating (DNC).
SERDES_x_REFCLK_P/N where, x refers to 1, 2, 3, 4, PCIE_0 or PCIE_5	Clock	Reference clock differential positive/negative. If SerDes is not used, it must be connected to SERDES_VDDI through a 10 kΩ resistor.

2.9 Special Pins

The following table lists the special pins name and description.

Table 8 • **Special Pins**

Name	Type	Description
DEVRST_N	Input	Device reset. External active low input only signal. Powered by VPP. Once asserted, DEVRST_n resets the system controller, starts up the device, and drives GRESET. It is an asynchronous signal and Schmitt trigger input with a maximum ramp rate of 1 µs. In unused condition, connect it to VPP through a 10 kΩ pull-up resistor.
TEMP_MONITOR	Input	An internal temperature sensing diode has a dedicated pin Temp_Monitor connected to the anode. The cathode is connected to VSS of the die.
VDD_MONITOR VSS_MONITOR	Input	Internal power supply sense pins—VDD_MONITOR and VSS_MONITOR—are provided for the RTG4-CQ352 device to monitor the device's VDD and VSS planes. These pins are connected directly to the VDD and VSS supply planes on the die. This sensing pair provides the best measurement points for the voltage of the silicon die and the best point to connect to the remote sense pins on DC-DC power converters. Using a power supply with a differential remote sense input is the best practice to ensure proper IR voltage compensation within the device and package. The voltage sensing connections to the power regulator must be routed as tightly coupled differential pair traces. It is critical that the routing traces be kept away from any switching and high current paths that can cause PCB noise. Remote sensing is required for the RTG4-CQ352 device to meet all device performance specifications.

Table 8 • **Special Pins *(continued)***

Name	Type	Description
PROBE_READ_DATA	Output In/Out	Using SmartDebug feature, the PROBE_READ_DATA output pin can be used for a single asynchronous test point of an internal fabric flip-flop output or it can be used in conjunction with the PROBE_CAPTURE input that serves to trigger the output observed on the PROBE_READ_DATA pin. If probing is not used, this pin can be configured as input, output, or bidirectional I/Os. To perform live switching between user I/O and probing, these I/Os must be configured only as outputs. If configured as input for general purpose, and then switched to probe operation, the probe circuitry drives out into these I/Os, and the I/Os may get damaged.
PROBE_CAPTURE	Input In/Out	Using SmartDebug feature, the PROBE_CAPTURE input is used with an external trigger to capture a snap-shot of an internal fabric flip-flop that is monitored by the PROBE_READ_DATA output pin. If probing is not used, this pin can be configured as input, output, or bidirectional I/Os.
DNC		Do not connect. This pin should not be connected to any signals on the PCB.
NC		No connect. This pin is not connected to circuitry within the device. It can be driven to any voltage or left floating with no effect on the operation of the device.

2.10 I/O Programmable Features

The RTG4 device supports different I/O programmable features for MSIO, MSIOD, and DDRIO.

Each I/O pair (P, N) supports the following programmable features:

- Programmable drive strength
- Programmable weak pull-up and pull-down
- Configurable ODT and driver impedance
- Programmable input delay
- Programmable Schmitt input and receiver

For more information about RTG4 I/O programmable features, refer to the RTG4 I/O Features table of the *UG0574: RTG4 FPGA Fabric User Guide*.

2.11 Packaging Information

See *https://www.microsemi.com/product-directory/rad-tolerant-fpgas/3576-rtg4#documents* packaging section for package outline drawings of RTG4 devices.

2.11.1 Pin Tables

See *https://www.microsemi.com/product-directory/rad-tolerant-fpgas/3576-rtg4#documents* packaging section for public pin assignment tables of RTG4 devices.