Total Ionizing Dose Characterization of 65 nm Flash-Based FPGA

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***Abstract*—New 65 nm flash-based field programmable gate array with system-on-chip capability is introduced. We present recent Total Ionizing Dose tests results on Smart Fusion 2 Flash-based FPGAs. TID effects at the device and product level are presented and discussed.**

I. INTRODUCTION

FLASH based Field programmable gate arrays (FPGAs) have become more and more attractive for high level system integration in aerospace and military applications. They have the advantage of being both nonvolatile and re-programmable compared to other technologies such as Antifuse and SRAM. Also, configuration cells are not susceptible to Single event upsets (SEU).

However, flash based FPGAs are sensitive to Total Ionizing Dose (TID) [1-2]. Charge pump circuit is one of the most TID-sensitive blocks because its high voltage operation requires the use of thick oxide MOS devices, which are sensitive to charge trapping. Also, Floating Gate (FG) cells can be affected by TID [3], resulting in threshold voltage shift and consequently bit errors. Even though the discharge of the floating gate is a phenomenon that does not imply any permanent damage, periodic refresh of the floating gate cell information may be required during a space mission to avoid the loss of critical data.

This work covers the TID performance at the device and product level of reprogrammable and non-volatile commercial 65 nm Flash-based FPGAs, the Smart Fusion 2 (M2S050).

II. PRODUCT UNDER TEST (SMART FUSION 2)

The M2S050 product is a family member of a new 65 nm flash-based field programmable gate array (FPGA) manufactured by UMC. It is a true system on chip (SOC) device featuring an inherently reliable flash-based FPGA fabric embedded with a 166 megahertz (MHz) ARM® Cortex™-M3 microprocessor with instruction cache and many other embedded functional components including advanced security processing accelerators, DSP blocks, SRAM, eNVM, and industry-required high-performance communication interfaces. SmartFusion2 is differentiated from other FPGAs by its low power capabilities that enable orders of magnitude lower power operation for low duty cycle applications, as well as high reliability and advanced security that makes it suitable for military, aviation, communication and medical applications. There are 56 K logic elements available in this member of the M2S (Smart Fusion 2) family.

The TID testing of the M2S050 product was conducted at two facilities, the defense microelectronics activity (DMEA) in McClellan, CA and Vanderbilt University in Nashville, TN using gamma ray and X-ray respectively.

III. TID INDUCED-EFFECTS AT THE DEVICE LEVEL

The TID effects in these Flash-FPGAs were shown first as radiation-induced charge loss in the floating gate [1-4] and second as induced leakage currents and shifts in the threshold voltage of the HV/MV/LV CMOS transistors [4-5]. The latter are used for the programming control circuits, the biasing of the FG devices and the FPGA logic gates. The FPGA configuration cell consists of a set of two NMOS transistors. Its gate stack is a typical floating gate structure very close to that in memory products as shown in Fig. 1. Each cell consists of two FG-NMOSFETs sharing the same gate. One transistor is called the sense device which performs the configuration programming and state sensing; the other transistor, called the switch device performs the ON/OFF switch function in the critical path and is tied-off in the non-critical path of the FPGA logic. Fig. 2 shows a simple layout and schematic of a flash configuration cell.

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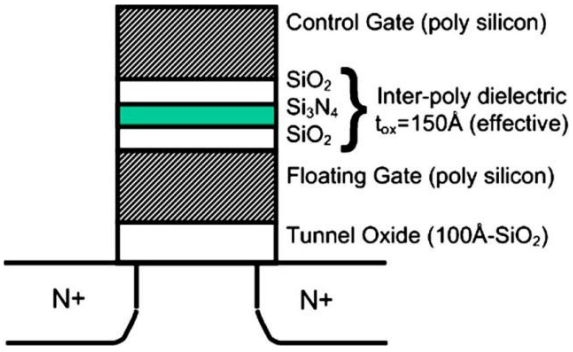
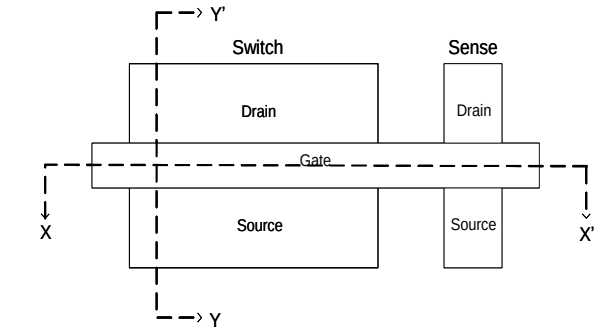
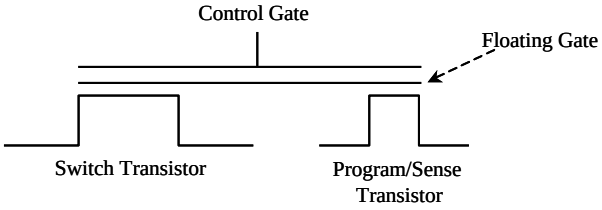


Fig. 1. Floating Gate Transistor in the Flash-Based FPGA



(a)



(b)

Fig. 2. (a) Layout of the flash configuration cell, each cell contains one switch and one sense FG transistor; the control gate and FG are shared by both the switch and sense transistor. (b) Schematic showing the cross-section X-X'.

A. TID effects on the floating gate device

Single flash cell and CMOS devices (high voltage, medium voltage and low voltage devices) were irradiated and tested at room temperature using an ARACOR 10-keV X-ray irradiation source at a dose rate of 18 krad(SiO_2)/min. Floating gate cell, high voltage and medium voltage devices were tested for doses up to 70 krad(SiO_2); low voltage devices were tested for doses up to 100 krad(SiO_2). During irradiation the gate was biased at V_{PP} (3.3 V) and V_{DD} (1.2 V), which are the normal operation condition for the thick oxide devices and thin oxide devices respectively, and the rest of the terminals were grounded. Flash cell, which contains one switch transistor and one sense floating gate transistor, was tested for both switch ON (erased state) and switch OFF (programmed state) states.

Fig. 3 shows the I_dV_g characteristics of the erased flash cell before and after irradiation, where the V_t shifts to the right by approximately 2.78 V at 70 krad. For the programmed state, as shown in Fig. 4, the V_t shifts to the left by approximately 0.83 V. The V_t of the flash cell in the erased (switch ON) and programmed (switch OFF) states versus total dose is summarized in Fig. 5.

Three radiation-induced mechanisms can affect the threshold voltage of the floating gate devices [6]: 1) holes injected into the floating gate, 2) holes trapped into the oxides and 3) electrons emitted over the polysilicon/oxide barriers. Electron-hole pairs initiated from radiation results in the injection of holes into the floating gate and the trapping of holes in the oxides. Hole injection and trapping have a similar effect since they both reduce the threshold voltage in the floating gate device. The third radiation phenomenon: electron-emission occurs mainly when radiation-induced photons possess an energy exceeding the potential barrier. The emitted electrons are then swept to the substrate or control gate by the electric field, which reduces the floating gate threshold voltage.

Fig. 5 also shows the experimental data fitting to the analytical model [1], [6] which predicts the immediate TID effects on the threshold voltage of a floating gate device. The fit curves in Fig. 5 are obtained using the following model with V_{bias} :

$$V_{th}(\gamma) = C_0 + B \bullet V_{bias} + [C_1 - B \bullet V_{bias}] \bullet \exp(-A \bullet \gamma) \quad (1)$$

Where γ is the total ionizing dose, V_{bias} is the control gate bias, and C_0, C_1, B and A are physical constants [1], [6].

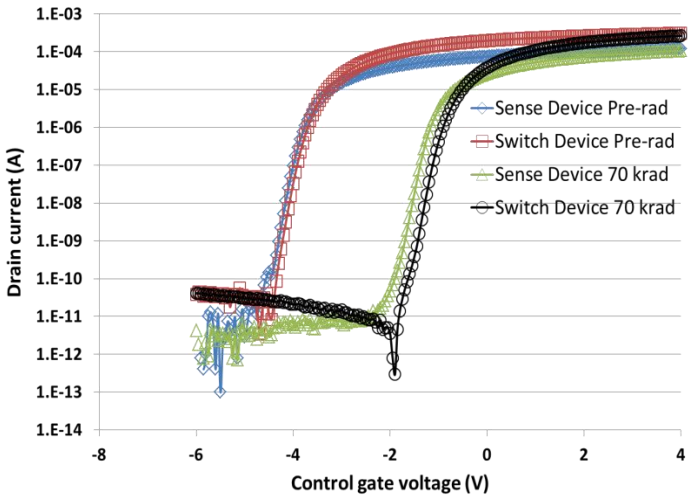


Fig. 3. TID effect on the erased FG cell (switch and sense).

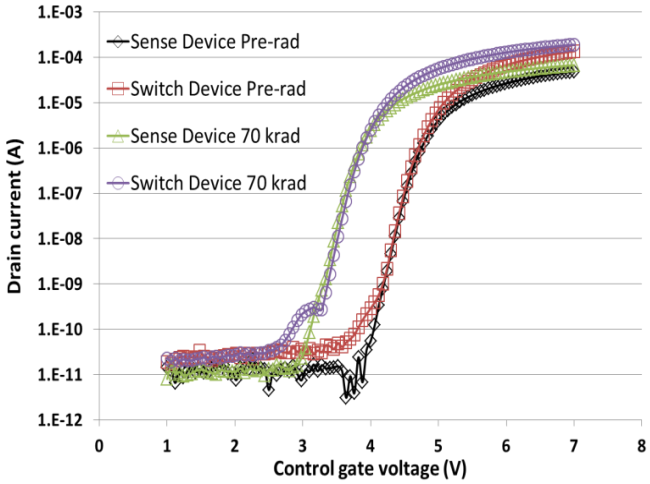


Fig. 4. TID effect on the programmed FG cell (switch and sense).

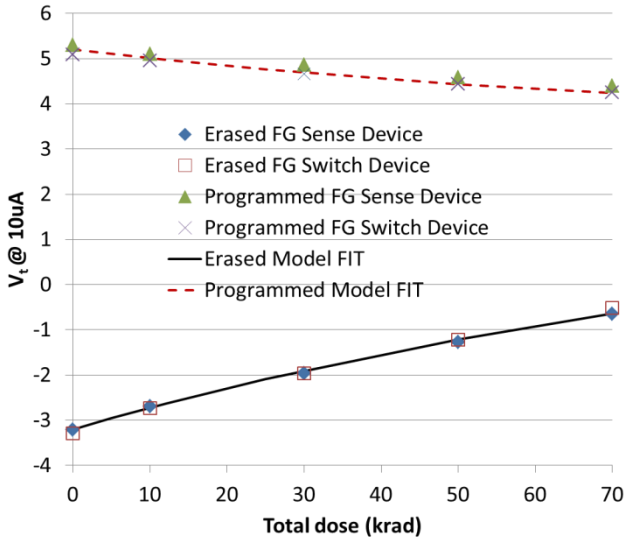


Fig. 5. Model prediction (dashed line) and experimental V_t versus total dose for flash cell in erased (switch ON) and programmed (switch OFF) states.

B. TID effects on the CMOS devices

The radiation-induced trapped charges in the high/medium voltage thick oxide devices cause a left shift in the threshold voltages with TID. For NMOS, this shift consequently induces significant drain-source leakage current. The positive oxide trapped charges at the STI sidewalls of the NMOS device induce further drain-source leakage current. On the other hand PMOS devices suffer from only post radiation V_t shift. Low voltage device with thin oxide, for both NMOS and PMOS, show negligible TID effects.

The I_dV_g characteristics of a high voltage and a medium voltage NMOS device with an effective gate oxide thickness of 290 Å are shown in Fig 6 (a) and (b), respectively. The pre-irradiation off-state leakage current increases by approximately 6 orders of magnitude at Vg = 0V with 70 krad. The I_dV_g characteristics of a high voltage PMOS device are shown in Fig. 7, which mainly suffers from V_t shift.

Finally the I_dV_g characteristics of a low voltage NMOS device with an effective gate oxide thickness of 26 Å show no V_t shift or off-state leakage current with TID as shown in Fig. 8.

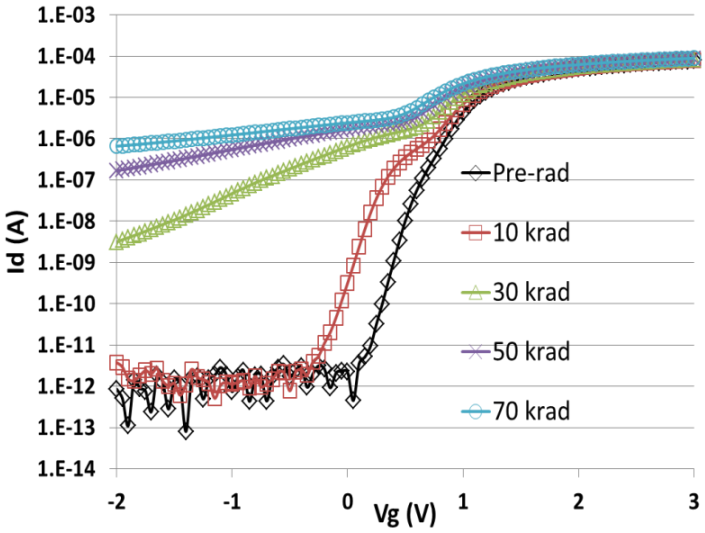


Fig. 6 (a). The pre and post-irradiation I_dV_g characteristics of high voltage NMOS device, with W/L = 10/1, and V_{ds}= 0.1 V.

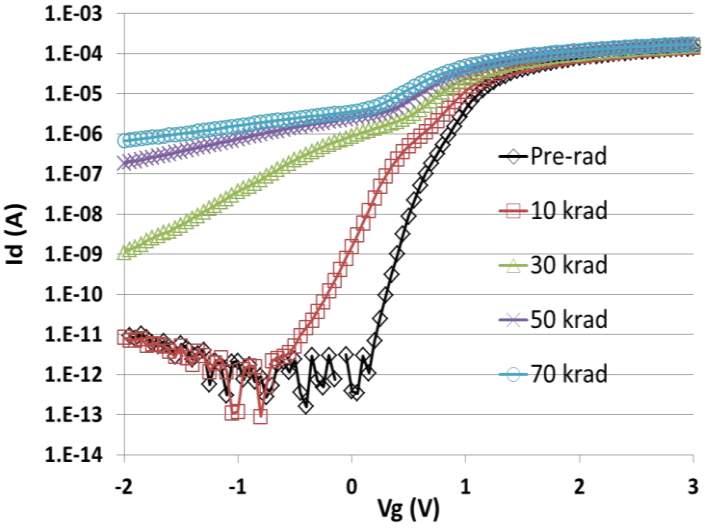


Fig. 6 (b). The pre and post-irradiation I_dV_g characteristics of medium voltage NMOS device, with W/L = 10/0.68, and V_{ds}= 0.1 V.

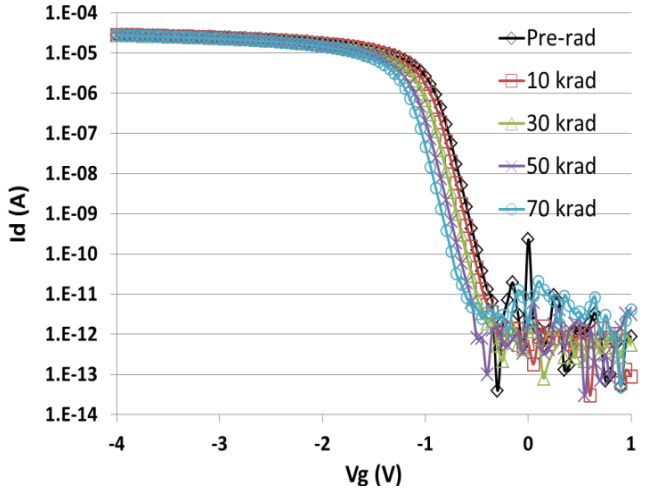


Fig. 7. The pre and post-irradiation I_dV_g characteristics of high voltage PMOS device, with W/L = 10/1, and V_{ds}= 0.1 V.

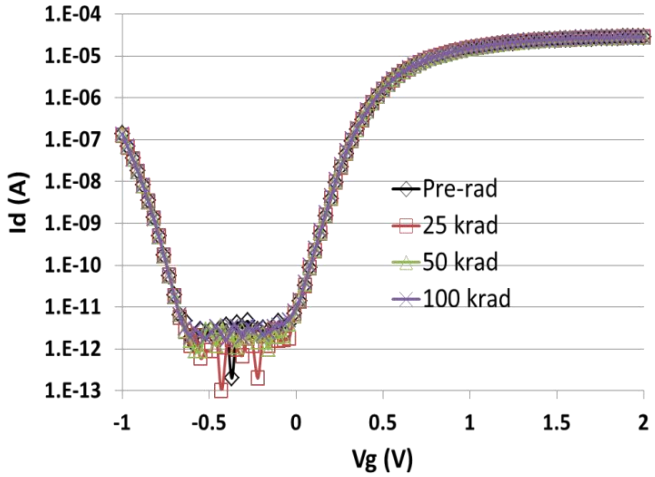


Fig. 8. The pre and post-irradiation I_dV_g characteristics of low voltage NMOS device, with W/L = 1/1, and V_{ds}= 0.1 V.

IV. TID INDUCED-EFFECTS AT THE PRODUCT LEVEL

TID testing on the M2S050 device of the SmartFusion2 SOC FPGA family was performed at DMEA using gamma ray at high dose rate of 10 krad(SiO_2)/min.

The combined TID-induced degradation of the physical parameters of CMOS and floating gate devices causes the parametric degradation measured on test designs implemented on the FPGAs. At the product level, typical key electrical parameters are the propagation delay and the core power supply current ICCA.

The propagation delay is measured on an inverter-string design with 7200 stages programmed into the FPGA. Fig. 9 shows a simplified block diagram of the critical path. The floating gate biasing circuit is mainly composed of high voltage devices. Their TID degradation will directly affect the control gate voltage of the floating gate device. The TID tolerance is illustrated by plotting 1) the degradation in the propagation delay versus the applied total dose, 2) the DUT core power supply current ICCA and 3) the V_t degradation of the flash-based FPGA switches. Each Smart Fusion 2 FPGA was configured with an inverter-string. Before irradiation and at every TID dose-step, the delta between the rising/falling edges of both the input and output signals of the inverter-string were measured. The input signal was supplied from a function generator while the electrical parameters of the input/output signals were observed and recorded on the oscilloscope.

Overall the propagation delay reaches 10% degradation after approximately 24 to 29 krad, and progressively reaches 100 % degradation after approximately 70 krad as shown in Fig. 10. All the parts remain functional after 100 krad.

The ICC power supplies remain within the specification except the core power supply current ICCA. Fig. 11 shows that ICCA increases significantly after reaching approximately 60 krad.

At total dose level up to 10 krad the V_t distribution of the fabric configuration cells (approximately 30 million in the M2S050) can be measured. The operation of measuring V_t of every flash cell is called "margin". The measurement starts to fail after approximately 10 krad on the high V_t side (programmed state) and approximately 15 krad on the low V_t side (erased state). When the measurement starts to fail, "margining" starts to produce unreliable data and finally no parts can be "margined" after 20 krad. The conjecture of the cause of the failure is due to the V_t shift of the thick oxide devices (high voltage and medium voltage transistors) in the peripheral circuitry. Fig. 12 shows the V_t cumulative probability distribution for TID up to 15 krad for a Flash-based FPGA irradiated with gamma ray at 10 krad(SiO_2)/min.

The TID degradation of the high voltage devices, i.e. V_t shift and leakage current shown in Fig. 6 (a) and (b), reduces the voltage of the control gate ($V_{control\ gate}$), and subsequently reduces the biasing of the floating gate device. For example, after irradiation the high voltage NMOS device M1 in Fig. 9 becomes not fully ON and can no longer pass a full V_{DD} to support $V_{control\_gate}$. $V_{control\_gate}$ starts to drop with irradiation, the floating gate device is no longer properly biased and the propagation delay starts to degrade.

In addition, the floating gate itself also suffers from V_t shift after irradiation (as shown in Figs. 5 and 12). Although Fig. 5 shows that V_t at 70 krad is still supporting the operation of the floating gate device, it only shows the results for a typical bit, and the worst bit can be a problem. Fig. 12 clearly shows a tail in the distribution, which may start to affect the operation of the floating gate cell.

Furthermore, if the increase in the propagation delay and ICCA current was only due to the V_t shift of the floating gate cell on its own, we would see a shallower increase in ICCA and propagation delay.

In conclusion, the combined effects of high voltage devices degradation and floating gate cell degradation result in the increase of the propagation delay and core power supply current ICCA. On the other hand, the inverters shown in Fig. 9 are low voltage devices and they have negligible TID effects as shown in Fig. 8 due to their thin gate oxide and should not have any significant impact on the results.

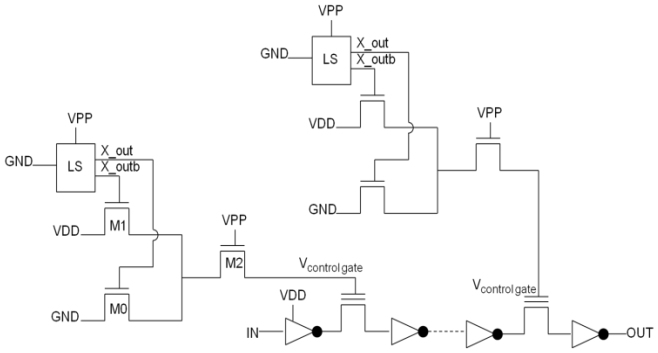


Fig. 9. Simplified block diagram of the DUT design, V_{PP} = 3.3 V, V_{DD}=1.2 V.

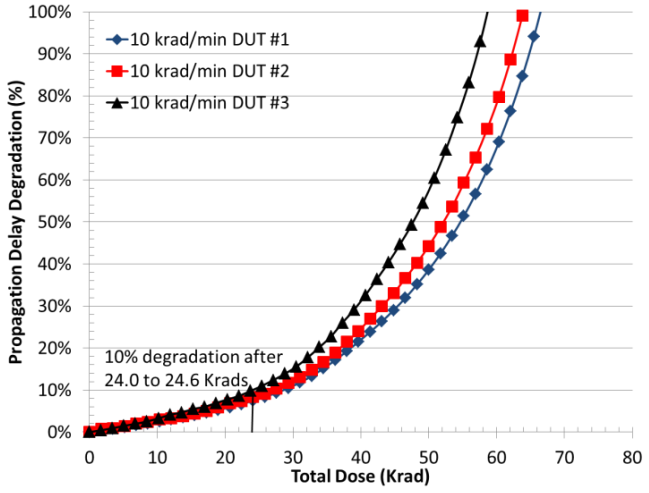


Fig. 10. Percentage of propagation-delay degradation versus TID at 10 krad(SiO_2)/min for multiple DUTs.

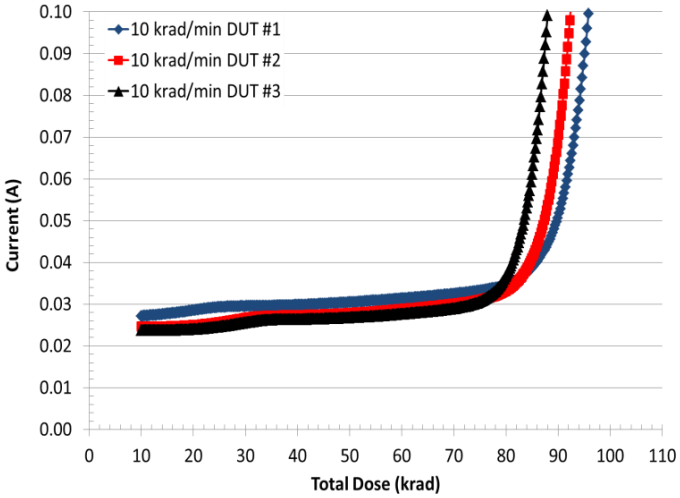


Fig. 11. ICCA versus TID at 10 krad(SiO_2)/min for multiple DUTs.

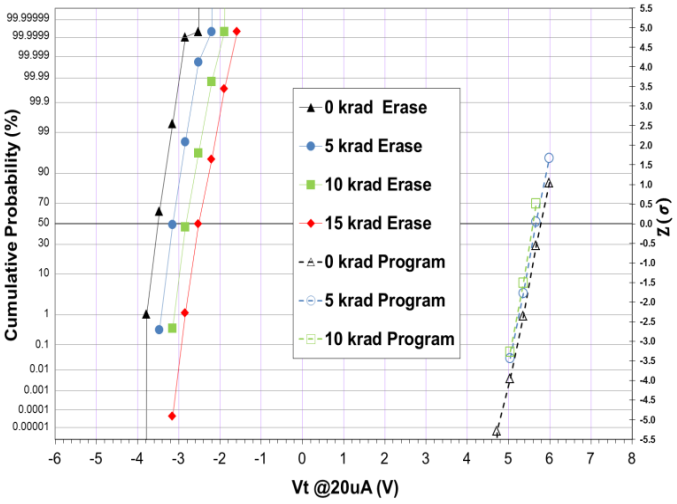


Fig. 12. Log normal distribution of V_t for the programmed state (plots on right) and erased state (plots on left) versus TID for a Flash-based FPGA irradiated with gamma ray at 10 krad(SiO_2)/min.

V. Conclusion

We presented data from recent TID test on Smart fusion 2 flash-based FPGA. Total ionizing dose effects at the device level and product level were presented and discussed. The TID tolerance at the product level was presented using three parameters: the degradation in the propagation delay versus the applied total dose, the DUT core power supply current ICCA, and the V_t degradation of the flash-based FPGA switches. We concluded that the combined degradation of the physical parameters of the thick oxide devices and floating gate devices causes the parametric degradation with TID of the performance of any design implemented on these FPGAs.

VI. References

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