Libero SoC v11.4 SP1 Release Notes

Libero® System-on-Chip (SoC) is the most comprehensive and powerful FPGA design and development software available, providing start-to-finish design flow guidance and support for novice and experienced users alike. Libero SoC combines Microsemi SoC Products Group tools with such EDA powerhouses as Synplify Pro® and Model*Sim*®.

Use Libero SoC v11.4 SP1 for designing with Microsemi's SmartFusion2 and SmartFusion SoC FPGAs, and IGLOO2, IGLOO, ProASIC3 and Fusion FPGA families.

Click the Documents tab on your device page at www.microsemi.com to obtain silicon Datasheets, User's Guides, Tutorials and Application Notes.

Development Kits and Starter Kits are available.

Note: It is recommended that all SmartFusion2 and IGLOO2 designs be updated to Libero SoC v11.4 SP1.

Contents

What's New in Libero SoC v11.4 SP1?

New Package Support

IGLOO2

Die	Package	Free Libero Gold	Libero Platinum
M2GL150	FCS536	No	Yes
M2GL150T	FCS536	No	Yes
M2GL150TS	FCS536	No	Yes

SmartFusion2

Die	Package	Free Libero Gold	Libero Platinum
M2S150	FCS536	No	Yes
M2S150T	FCS536	No	Yes
M2S150TS	FCS536	No	Yes

New Operating Conditions for Security Devices

All SmartFusion2 and IGLOO2 parts are now offered in STD & -1 speed grades, and COM and IND Temperature Ranges.

Software Enhancements

SmartPower uses production (post-silicon) data for M2S050/M2GL050, M2S025/M2GL025 and M2S010/M2GL010 devices.

Mini-LVDS I/O Update.

The drive strength for Mini-LVDS has been updated to meet the datasheet specifications.

Design separation methodology for implementation and verification.

This new design flow provides a methodology to keep individual subsystems separate and independent (in terms of physical layout and programming) to meet design separation requirements.

When the Compile option is enabled, Libero generates a parameter file that details design blocks present in the design and the number of signals entering and leaving a design block.

For more information, refer to the SmartFusion2 and IGLOO2 Microsemi Design Separation Methodology document.

Stand-alone Peripheral Initialization for MDDR/FDDR/SERDESIF Peripherals

In some applications it may not be possible to use the automatically generated peripheral initialization using the System Builder flow. A new stand-alone solution has been provided to allow users to create their own initialization solutions. When enabled in the Project Settings, the System Builder will not build the peripherals initialization logic. For more information, refer to the SmartFusion2 DDR Controller and Serial High Speed Controller Standalone Peripheral Initialization or IGLOO2 DDR Controller and Serial High Speed Controller Standalone Peripheral Initialization document.

New SmartFusion2 and IGLOO2 Programming Features

Libero SPI Slave programming of the SmartFusion2 and IGLOO2 devices supported with FlashPro5.

The programming mode setting can be configured from “Programming Connectivity and Interface” tool within Libero.

Libero Select Target Device option added in the “Programming Connectivity and Interface” tool.

Allows the user to select the target device for programming when there are identical SmartFusion2 or IGLOO2 devices in the JTAG chain.

Libero export single device chain STAPL file for SmartFusion2/IGLOO2 devices.

Exports a STAPL file to program a single device within a JTAG chain. This is added to the “Export Bitstream” tool.

Critical Fixes in Libero SoC v11.4 SP1

Fixes for Fusion and SmartFusion (Microsemi Binary Memory Format)

In Libero SoC v11.4, Flash Memory System Builder cannot generate the RAM with initialization in SmartDesign. This is fixed in 11.4 SP1.

Fixes for SmartFusion2 and IGLOO2

The SmartFusion2 MSS block has no best/worst case de-rating in v11.4.

SmartTime will report optimistic timing for all timing paths to/from the MSS block. Note that the MSS timing was correct in v11.3.

Use 11.4 SP1 for proper timing analysis of designs containing MSS or HPMS.

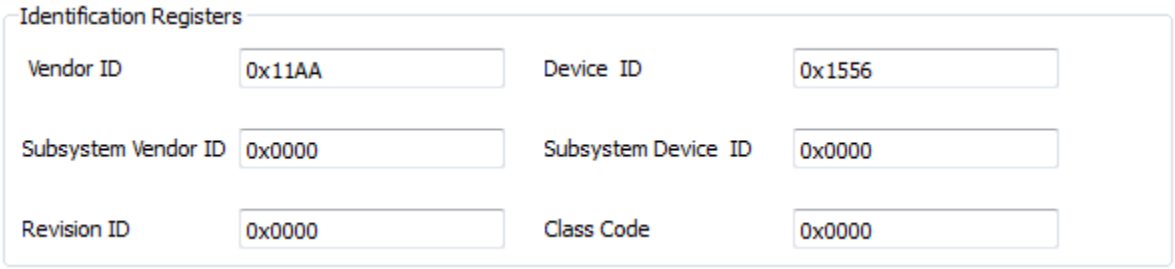
SERDES - PCIe BAR2/3 shifting on silicon

SERDES_IF versions 1.2.102 and earlier have an incorrect BAR2/3 mapping configuration and should not be used.

New SERDES_IF v1.2.103 was released 9/4/2014 with the BAR2/3 configuration fix. Download and update your design.

SERDES – PCIe Core Replace Version

When replacing the SERDES core version with v11.4 the configuration data for the PCIe Identification Registers was incorrectly generated, causing these registers to be incorrect on silicon. This problem has been resolved in 11.4 SP1.



Updating Your SmartFusion2 or IGLOO2 Design to Libero SoC v11.4 SP1

There are several software updates in Libero SoC v11.4 SP1 that require pre-v11.4 SP1 designs to be updated before proceeding with programming. They are listed below:

Designs using MINILVDS I/O are invalidated to the pre-programming state.

The programming of the MINILVDS I/O has been updated. When updating to v11.4 SP1 the following information will be provided to the user.

Info: "Your design contains I/Os using the MINILVDS I/O standard. The drive strength for this standard has been updated to meet the datasheet specifications.

Designs using On Die Termination and fixed calibration code are set to a pre-Compile state.

In SmartFusion2/IGLOO2 only the DDRIO banks support an automatic calibration of the ODT. ODT can be used in other IO banks, but must use a fixed calibration. In releases prior to Libero SoC v11.4 SP1 it was possible for a design to contain ODTs set for calibration in non-DDRIO banks. In this case, Libero SoC v11.4 SP1 will alert the user of this incorrect assignment.

Info: "Your design contains I/Os using On Die Termination (ODT) placed in banks that have fixed calibration codes. This configuration is not supported.

Design containing a Fabric DDR Controller (FDDR) using an LPDDR configuration with LVCMOS18 I/Os and no calibration are set to a pre-generated state.

When using the FDDR with LVCMOS18 I/O calibration is required to be used. If a design contains a FDDR with LVCMOS18 I/O without calibration when updating to v11.4 SP1 the following information will be provided to the user.

Info: "Your design contains a Fabric DDR Controller (FDDR) using an LPDDR configuration with LVCMOS18 I/Os and no calibration. Programming files generated with this configuration are incorrect.

SmartFusion2 designs invalidated to the pre-programming state.

M2S050 designs are not affected.Pre-v11.4 SP1 designs targeting all other SmartFusion2 devices will be invalidated and the following warning message will be displayed.

Warning: Your design contains a Micro Controller Subsystem (MSS) with the cache enabled. Concurrent accesses of the I-Bus and D-Bus on the Cortex-M3 may result in an invalid value returned to the Cortex-M3 when both accesses go through the cache. Concurrent accesses of the I-Bus and D-Bus have been permanently disabled.

Introduced in Libero SoC v11.4

New Package Support

IGLOO2

Die	Package	Free Libero Gold	Libero Platinum
M2GL005	256 VF	Yes	Yes
M2GL005S	256 VF	No	Yes
M2GL010	144 VQ	Yes	Yes
M2GL010	256 VF	Yes	Yes
M2GL010T	256 VF	Yes	Yes
M2GL010TS	256 VF	No	Yes
M2GL025	256 VF	Yes	Yes
M2GL025T	256 VF	Yes	Yes
M2GL025TS	256 VF	No	Yes

SmartFusion2

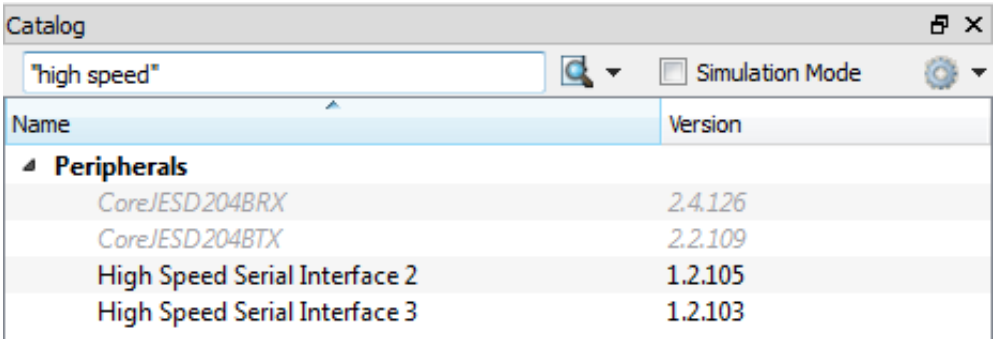
Die	Package	Free Libero Gold	Libero Platinum
M2S005	256 VF	Yes	Yes
M2S005S	256 VF	No	Yes
M2S010	144 VQ	Yes	Yes
M2S010	256 VF	Yes	Yes
M2S010T	256 VF	Yes	Yes
M2S010TS	256 VF	No	Yes
M2S025	256 VF	Yes	Yes
M2S025T	256 VF	Yes	Yes
M2S025TS	256 VF	No	Yes

Software Enhancements

High Speed Serial Interface Configuration GUI Enhancements

M2S/M2GL090T/TS: Two and Three-Protocol Support

Libero 11.4 SP1 supports both two-protocol and three-protocol versions of the High Speed Serial Interface (only for the M2S090T/TS and the M2GL090T/TS). If you want to use the High Speed Serial Interface in two-protocol mode, you must instantiate High Speed Serial Interface 2 version 1.2.105. If you want to use the High Speed Serial Interface in three-protocol mode, you must instantiate High Speed Serial Interface 3 version 1.2.103.



Protocol of EPCS used for SGMII, EPCS_125, and EPCS_250

The protocols of SGMII, EPCS_125, and EPCS_250 are no longer provided in the protocol drop down of the GUI. When migrating projects to v11.4 SP1 these protocol selections will be automatically converted to use an equivalent EPCS mode for the data rate and bus width.

The new EPCS protocol always presents a 20-bit data bus for the EPCS_TX_DATA and EPCS_RX_DATA ports. The IGLOO@ FPGA High Speed Serial Interfaces User Guide provides information on which bits of the 20-bit data bus are used for each of the supported bit widths (4, 5, 8, 10, 16, and 20). Libero SmartDesign supports a function to slice a port into smaller bit widths. This function can be used to modify the port for connections in SmartDesign.

Runtime improvements

This release delivers faster:

- Layout for larger devices.
- High-effort Layout.
- Timing Analysis.
- PLL lock simulation for low frequencies.
- System Builder, SmartDesign, and MSS generation.
- File import.

Libero UI Enhancements

Simulation Flow Enhancements:

- Ability to create a HDL or SmartDesign test bench from any node in the Design Hierarchy.
- Ability to run pre-synthesis simulation on any test bench from the Stimulus Hierarchy.

Enhanced configuration data management for SmartFusion2 MSS, SERDES and FDDR.

Enhanced HDL text editor with:

- Syntax & Block Highlighting
- Comment/uncomment
- Column Editing

Reports can be viewed as soon as they are available when running the Design Flow.

You can now instantiate VHDL files containing these special types in SmartDesign.

- Multidimensional Arrays
- “Record” datatype

Libero SmartFusion2 Firmware Flow Changes

There are major changes to the Firmware development flow in Libero SoC v11.4. Prior to Libero SoC v11.4 portions of the firmware were automatically updated when design changes were made in the System Builder or the High Speed Serial Interfaces or FDDR GUIs. Starting with Libero SoC v11.4 the user is now responsible for exporting the updated firmware after changes have taken place.

In the design flow there is now a new function "Export Firmware". The user can use this tool to export the updated firmware .c and .h files for use in the firmware development. This is now a requirement for the user to push the latest configuration to the Software IDE used by the user

SmartFusion2 CMSIS 2.2.101 must be used with v11.4

The SmartFusion2 CMSIS v2.2.101 includes an updated peripheral initialization for the SERDES and M/FDDR. This CMSIS needs to be used with the netlist generated with the Libero SoC v11.4 and newer System Builder. A mismatch in the SmartFusion2 CMSIS version will results in the INIT_DONE function of the System Builder module to never assert. In Libero SoC v11.4 SP1 there is a check to make sure users are using the correct SmartFusion2 CMSIS version.

To view and configure the firmware driver cores corresponding to the SmartFusion2 CMSIS, MSS peripherals and soft IP peripherals, use the ‘Configure Firmware Cores’ tool in the Design Flow pane which opens the DESIGN_FIRMWARE window.

Note: If you are regenerating your Firmware project or Firmware directory for any reason, you must upgrade your SmartFusion2 CMSIS core to version 2.2.101 or later.

HDL+

Management of parameter changes, port changes and HDL links.

Bus Interface Port Mapping Enhancements.

System Builder

Independent PCIe resets for M2S090/M2GL090.

AHBLite Bypass Mode Option for improved throughput.

AXI direct Master/Slave connection for improved throughput.

Memory map fixes.

SERDES

M2S090/M2GL090 devices

These devices now support independent PCIe resets and two PCIe Endpoints with two independent lanes of EPCS protocol.

PCIe Peripheral Initialization

The PCIe Peripheral Initialization sequence has been re-architected to properly configure the PCIe registers. You must upgrade to the latest SERDES core versions and re-generate your design to use the new initialization sequence. Note that, for SmartFusion2, you must export the firmware with the latest SmartFusion2 CMSIS version (v2.2.101) and re-compile your firmware application.

EPCS Configuration

The SERDES configurator has been enhanced to provide an extended set of EPCS configurations.

- Configurable Reference Clock and data rate per lane.
- Flexible lane assignment.
- The pre-defined SGMII, EPCS-125 and EPCS-250 protocols have been removed. Note that SGMII configuration is equivalent to 125MHz Reference Clock and 1250 bit/s (10-bit interface) data rate configuration.

Timing for M2S025/M2GL025 and M2S010/M2GL010 devices

Production (post-silicon) timing and improved min-delay timing analysis.

MIL Temperature Analysis

Custom temp range selection spanning -55~125 allows for timing and power analysis for all SmartFusion2 and IGLOO2 devices.

Test Bench Generation for SmartDesigns

Creation of HDL/SmartDesign test benches available from any node in the Design Hierarchy.

Pre-synthesis simulation of any stimulus files from the Stimulus Hierarchy.

In previous releases Libero automatically generates a test bench when you generate the corresponding SmartDesign. Starting with Libero SoC v11.4 if you regenerate your SmartDesign your auto-generated test-bench will be deleted. If you want to preserve your pre-v11.4 test bench you must save it to a different location.

TCL Enhancements

New user guide with examples: Batch Flow TCL for SmartFusion2 and IGLOO2

Support for:

- ‘Security Policy Manager (SPM)’
- ‘Flash*Freeze’
- ‘Export Design Summary’

I/O Editor Enhancements

Column-based filtering

Multi-row editing

LPDDR LVCMOS18 support has been added to reduce power

Layout Optimizations

Automatic IO Register Combining to aid in IO timing closure.

System Services Simulation

Export Design Summary (Datasheet) Tool for SmartFusion2 and IGLOO2

Datasheet (.xml) will not be generated when the top level (root) SmartDesign component is generated. However, you can export the snapshot of your design summary (datasheet in .html format) to any desired location on disk by using the option 'Tools → Export → Design Summary'.

Export Firmware Tool for SmartFusion2

The firmware directory and the software IDE project will not be generated when the top level (root) SmartDesign component is generated. You can export the firmware directory and the software IDE project of your choice (SoftConsole/IAR/Keil) to any desired location on disk by using the 'Export_Firmware' tool in the Libero Design Flow pane.

Configure Firmware Cores Tool for SmartFusion2

To view and configure the firmware driver cores corresponding to the SmartFusion2 CMSIS, MSS peripherals and soft IP peripherals, use the 'Configure Firmware Cores' tool in the Design Flow pane which opens the DESIGN_FIRMWARE window.

Programming

Integrated drivers for FlashPro5 hardware for Windows and Linux platforms.

New FlashPro Express programming tool for production programming.

Debug Policy can be enabled within the Security Policy Manager.

Libero programming on Linux with FlashPro5 for SmartFusion2 and IGLOO2.

Programming Recovery and Auto Update in Libero.

Updated Security Policy Manager in Libero.

Libero Export Programming Job tool simplifying job transfers to FlashPro Express.

Updated Export Bitstream tool In Libero allowing users flexibility in customizing the bitstream components and types of security files to be exported.

SmartDebug support for SmartFusion2 and IGLOO2 on Linux with FlashPro5.

Silicon Signature Programming Support.

SmartDebug

When device is secured, SmartDebug is allowed only when Debug Passkey and User Passkey match.

FlashPro Express - New Production Programming Tool

- Windows supports FlashPro Lite, FlashPro3, FlashPro4, FlashPro5
- Linux supports FlashPro5 only

SoftConsole 3.4 SP1 Requirement

SoftConsole v3.4 requires a service pack to be compatible with Libero SoC v11.4

You must use SoftConsole 3.4 SP1, and SmartFusion2 CMSIS version 2.2.101 or later with Libero SoC v11.4

Download SoftConsole 3.4 SP1.

Updating Your Design to Libero SoC v11.4

Libero Project Invalidation

With each new update of the Libero SoC design suite comes new features, new device support and resolved issues. As the Libero SoC design suite is upgraded it is sometimes required to invalidate Libero projects created with previous versions of Libero SoC. Design invalidation means that the current Libero project will not be able to use either a subset or all of the existing data structures of the previous project. This means that the design flow may be reset back to a pre-synthesis state or that portions of the design may need to be regenerated in the case of IP or architectural elements. The decision to invalidate a previous Libero SoC project is not taken lightly and every option to provide a backward compatible solution is always considered. The following sections will document the conditions for project invalidation with Libero SoC v11.4.

SmartFusion2 and IGLOO2 Project Invalidation Conditions

Embedded Features

In Libero Soc v11.4 the data structures associated with the embedded features of the SmartFusion2 and IGLOO2 have been modified. This includes the System Builder, High Speed Serial Interface (SERDESIF), and the DDR Memory Controller (MDDR and FDDR). If using a design from 11.3, it is not necessary to regenerate these modules, Libero SoC v11.4 will work correctly without any modifications to these blocks. However, if one of the blocks is regenerated, then all of them will need to be regenerated to use the new data structures. When a block is regenerated the design flow will be reset back to the pre-synthesis state.

If a project contains a SERDESIF that is prior to Libero v11.3 then the following warning will be issued and the project will be automatically reset back to the pre-compile state.

Warning: Your design has been invalidated because it contains out-of-date SERDES blocks.

Reasons for updating to the latest version of embedded blocks are listed below.

- SERDESIF - New PCIe initialization and reset scheme (required for PCIe designs).
- SERDESIF - New EPCS data rate and lane selection features.
- SERDESIF - New EPCS reference clock addition when using two or more lanes.
- MSS/FDDR – Addition of the LVCMOS18 type for the MDDR and FDDR LPDDR controllers.
- ALL – Any other resolved issues that have been addressed in this release.

To update to the latest version of the blocks you must replace the embedded cores with the latest version available from the repository and regenerate the design. Re-run Compile

Updating designs using SERDES_IF

You must update SmartFusion2 and IGLOO2 designs that use SERDES blocks in the following steps:

1. Open your existing Libero 11.3 project.
2. If you are not using PCIe:
    a. Right-click on each instance of SERDESIF.
    b. Click “Replace Component for Instance” and replace the SERDESIF instance with either High Speed Serial Interface v1.2.103 (for all but the 090T/TS devices) or High Speed Serial Interface 2 v1.2.105 (for the 090T/TS devices).
3. (SmartFusion2 only):
    a. Upgrade your SmartFusion2 Firmware core to 2.2.101 using the ‘Configure Firmware’ tool in the Design Flow.
    b. Regenerate your Firmware project using the new ‘Export Firmware’ tool in the Design Flow and recompile your application with the exported firmware configuration.

SSTL and HSTL IO

In Libero SoC 11.4 referenced buffer types are no longer supported on certain device pins.

SSTL18I, SSTL18II, HSTLI, and HSTLII

These IO standards are no longer supported in MSIO or MSIOD banks. They are still supported in DDRIO banks.

SSTL15I and SSTL15II

These IO standards are no longer supported when not used with the MDDR and FDDR memory controllers.

If your pre-v11.4 design contains I/O standards on unsupported device pins then the software automatically invalidates your Compile state. The user must change the IO type or move the pin to a valid location in the device.

If your design is affected when you open your project you will see the following message:

Warning: Your design has been invalidated to a pre-Compile state because of unsupported I/O standards.

Resolved Issues

Issues Fixed in v11.4 SP1

SAR 59212 - Export Design Summary sometimes results in an empty html file => 0 KB.

SAR 59576 - Libero export_prog_job Tcl command failed when file type is UEK1.

SAR 58949 - Generate bitstream fails during name change in programming connectivity and interface.

SAR 59218 - Export Bitstream, Export Programming Job and Generate Bitstream will fail if DPK is not entered in the Security Policy Manager.

SAR 60230 – When moving a project with SERDES from Libero SoC v11.3 to 11.4, Replace Instance results in an invalid configuration of the design after Generation.

SAR60089 – MSS Timing Data is optimistic in v11.4.

Issues Fixed in v11.4

SAR 48929 - SmartDesign shows incorrect Memory Map for SmartFusion2 FIC_1.

SAR 49025 – System Builder shows incorrect Memory Map for IGLOO2.

SAR 49868 – The Power Report is generated only for the first run when using the Multi-pass Layout option.

SAR 51770 – MSS/HPMS VHDL post-synthesis/post-layout simulation fails for projects created with Libero SoC v11.1 SP3 and earlier.

SAR 52554 – 325 FCSBGA Package and SERDES lane limitations have been addressed.

SAR 53628 - SmartFusion2 and IGLOO2 PCIe registers are not initialized properly in all cases.

SAR 54054 - Secure IP Flow: VHDL compiler directive ‘protect’ treated as illegal syntax.

SAR 54584 - Generic of std_logic in VHDL RTL reports error in Compile for VM flow.

SAR 55035 - PCIe SERDESIF configuration is lost when changing lane width.

SAR 55154 - PCIe SERDESIF reverse x1 mode not linking up.

SAR 55368 - eNVM cannot be accessed from SmartDebug when UPK1 is used to lock eNVM update protection.

SAR 55421 - "Device I/O states During Programming" Option crashing on Linux.

SAR 55517 - Stand-alone Identify Instrumentor error.

Customer Reported SARs fixed in v11.4 SP1

SAR	Case Number	Product	Summary
56192	493642-1605209692, 493642-1659255930	FlashPro	Support two identical SmartFusion2 or IGLOO2 devices in chain.
56859	493642-1619399836	Help	Update Tcl commands in the User Guide.
58552	493642-1638771622	Compile	Update the outdrive bits for the MLVDS and BUSLVDS to be 6.
59137	493642-1659255930	FlashPro	Support exporting chain STAPL for SmartFusion2 and IGLOO2.
59282	493642-1674374510	IBIS	IBIS model for LVCMOS 3.3 was incorrect for IGLOO.
59960	493642-1695967650	SmartGen	Fusion Flash Memory System Builder cannot generate the RAM with initialization in SmartDesign.

Customer Reported SARs fixed in v11.4

Refer to your Technical Support Hotline Case Number to determine if the SAR has been fixed in this release. The case number and SAR are listed below.

SAR	Case Number	Product	Summary
129	1-12375313	Project_Manager	VHDL parser support for VHDL 93 syntax.
6087	1-32101848	Project_Manager	HDL Editor color scheme enhancement.
55110	3642-1576444552	Project_Manager	Failed to create core from design hierarchy.
29635	489394-306510963	Project_Manager	Fixed runtime error while opening SmartDesign Component (VHDL Array Type support).
42440	493642-1078521778	FlashPro Express	FlashPro Linux support.
44158	493642-1131886330	Project_Manager	Support for VHDL user defined data types.
43502	493642-1147728263	SmartDesign	Export datasheet.
43915	493642-1187871652	SmartDesign	SmartDesign incorrectly changes VHDL ports from unsigned to std_logic_vector type.
45965	493642-1252144869	SmartDesign	Add support for VHDL Record in SmartDesign.
47210	493642-1276143212	Project_Manager	Enhancement in stimulus hierarchy.
47422	493642-1316926771 493642-1517479118	Project_Manager	Libero support for referring internal signals in VHDL test bench.
48004	493642-1320859644	FAB_CCC	Output Delay value in CCC with PLL configuration.
48813	493642-1356097722	Project_Manager	ULPI XCLK should not be shown as InOut. It is only Input.
50153	493642-1427026061	Project_Manager	HDL uncomment function not working as expected.
51176	493642-1427891495	Help	Missing ERRORCODE/AUTHERRCODE information in FlashPro online help.
50399	493642-1433992578	SmartDesign	Mismatch in the memory map of FIC0.
49750	493642-1456089123	CAE	Need burst mode for PCIe BFM model with AXI interface.
52243	493642-1495894889	Project_Manager	Libero does not allow direct instantiation method in VHDL.
53203	493642-1526597854	Project_Manager	Constraint Flow is not working.
53683	493642-1529692090	Designer	Synthesis and Compile reports show different resource utilization.
53410	493642-1533321021	SmartGen	Selecting and deselecting outputs in CCC configurator is not behaving correctly in Smartfusion2 device.
53895	493642-1535816992	Microcontroller	Add a new BFM command to fill an array from a text file.
54117	493642-1542294911	Firmware Catalog	IAR Profile needed to generate IAR Firmware from Libero for SmartFusion2.
53899	493642-1552954576 493642-1617555861	Designer	Resource Usage Report Enhancement.
53995	493642-1555950679	Project_Manager	VHDL Array support.
54845	493642-1561745092	FAB_CCC	Describe how we can achieve frequencies lower than 768 kHz.
55152	493642-1564774511	Designer	Update SC_SPI pins for SmartFusion2 and IGLOO2.
54619	493642-1566753874	Synopsys	Synthesis failed because of Internal Error in m_proasic.exe.
54522	493642-1567956542	Project_Manager	Design should not compile after introduction of a syntax error in VHDL.
54495	493642-1568401322	SmartDesign	SmartFusion2 eNVM Data Clients do not show up in memory map.
54846	493642-1571079832	Designer	Unable to constrain JTAG bank to a voltage other than 3.3V.
54899	493642-1574237892	SmartGen	Issue with hex file format for RAM initialization.
54836	493642-1574723646	SmartDesign	MSS_eSRAM0 address range is wrong in memory map table.
55185	493642-1583238591	Project_Manager	Issue while exporting IBIS file for FCS325 package.
55464	493642-1584713909	Micro_Controller	Wind/U X-toolkit Error.
55640	493642-1595355553	Designer	Assertion in "Export BSDL file".
56048	493642-1598905151	Timing	LPDDR power solution for M2S010-VF400.
56351	493642-1598905151	MVN	Update the LPDDR standards based on the production characterization data.
56300	493642-1602265092	Micro_Controller	PCIe AXI/AHB BFM simulation to replicate silicon behavior.
56297	493642-1608705238	Project_Manager	Error while importing Tcl.

56326	493642-1609904452	Micro_Controller	MDDR clock is not working.
57206	493642-1609904452	SmartGen	Allow option to turn off calibration for DDR.
57188	493642-1616425522	Designer	Designer crash while setting IO attributes through TCL.
57025	493642-1618564625	Project_Manager	Remove External 32KHz xtl osc as source for HPMS/MSS in F*F Hardware Setting GUI.
56809	493642-1622185041	Error_Msg	Generating SERDES in VHDL project gives warning about top_test_SERDES_IF_0_SERDES_IF_pre.vhd.
56941	493642-1624413570	Micro_Controller	AXI WSTRB and WRDATA are not in sync.
57096	493642-1626949610	Project_Manager	Problem creating a core from HDL.
57290	493642-1628501395	Project_Manager	Tool ignores back annotated file HDL selection.
57093	493642-1629224981	Mentor	ModelSim ME fails for a specific project.
53168	493642-1641483259	Designer	NCSim elaboration errors.
58330	493642-1644113861	SmartGen	RAM content manager incorrectly populates with zeros.
58344	493642-1655850735	Project_Manager	Optimization flag error in SoftConsole files used by SmartDesign.
59020	493642-1667451401	Designer	RC Osc clock signal must be on a global network when it drives the Fabric logic directly.
8878	493642-33916303	Project_Manager	Fixed issues related to connecting ports of array types for VHDL Record when using SmartDesign.
31614	493642-38237973	SmartDesign	Conflicts between signal name and macro name causes post-synthesis simulation to fail.
35631	493642-515129313	Project_Manager	Support for defining multiple entities in single VHDL file.
36604	493642-616782013	FlashPro Express	Linux programming support.
38461	493642-814259074	Project_Manager	HDL cannot delete from disk.
21655	493642-882588725 493642-51581943 493642-1252144869	SmartDesign	Add support for VHDL 'record' structure in SmartDesign.
39944	493642-930895145	Project_Manager	Remove “Open datasheet for details" error message for IP Components.
51401	93642-1470559328	Project_Manager	MSS Datasheet generated by Libero is not updated after user makes changes to the MSS.

Known Limitations, Issues and Workarounds

Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines the InstallShield Wizard displays a message stating:

The installation of Microsoft Visual C++ 2005 SP1 Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Select **Yes** and the installation will complete successfully.

SmartFusion2 and IGLOO2

SAR60102 – PCIe BAR2 and BAR3 settings incorrect with SERDESIF version 1.2.102

Version 1.2.102 of SERDES_IF does not correctly configure the PCIe BAR2 and BAR3 windows. You must use SERDES_IF version 1.2.103 with Libero 11.4

SERDES - PCIe - Options BAR size is not preserved if it is set to 4K

Incorrect – blank – size setting when re-opening configurator for BARs 1 to 5. This will be fixed in a subsequent release.

Workaround: Select any other configuration first and then select 4KB. It will then be registered correctly.

SERDES – EPCS - Issue when switching project settings (speed grade)

The EPCS data configuration changes when you change the speed grade settings (STD <-> -1) in Libero and re-open the SERDES configurator after the speed grade change. You may not realize the configuration has changed and proceed with an incorrect configuration. The silicon will not be functional.

Workaround: Always re-open the SERDES configurator and reconfigure the data rate after changing the speed grade.

SAR 46571 - M2S050 has only one Oscillator

When you instantiate the Oscillator in your design and also use MSS RTC, the Clock Source of the RTC must match the clock source used in the Oscillator. For example, configuring the RTC with Clock Source set to 32 KHz RTC Crystal Oscillator while the Oscillator block is configured with the External Main Crystal Oscillator set to 5 MHz is invalid. The frequencies must match.

MIL Temp Removed from 400 VF, 676 FBGA & 896 FBGA packages

Military Temperature for all SmartFusion2 and IGLOO2 packages was introduced in V11.2. Subsequently, we decided to offer MIL Temp only for 484 FBGA and 1152 FC packages.

If you started a design using Libero SoC v11.2 and selected MIL Temp for any 400 VF, 676 FBGA or 896 FBGA packages, when you open the project in Libero SoC v11.3 the software will crash. Please contact soc_tech@microsemi.com for instructions on how to modify your project so that it can be opened in the current release.

For IGLOO2 projects use System Builder for the following cores; do not use these cores from the Catalog directly.

- DDR Memory Controller
- CoreConfigP
- CoreResetP
- CoreConfigMaster

SAR 58852 – Back-annotated netlist created using a previous release will be invalidated when the project is opened in Libero SoC v11.4.

MSS and SERDES timing has been updated in the simulation models necessitating invalidation of the back-annotated netlist.

Using SmartDebug functions causes the SmartFusion2 MSS and IGLOO2 HPMS to reset in Libero v11.4

When using the SmartDebug functions, for example Memory Blocks Read or SERDES Debug, etc., within Libero SoC v11.4 or standalone FlashPro v11.4 the SmartFusion2 MSS and the IGLOO2 HPMS are reset during the debug process. One of the consequences of this issue is that when using the SERDES debug utility this behavior will prevent proper access to the SmartDebug SERDES control and status registers.

The reset behavior will occur on M2S/M2GL005, 010, 025, and 050 devices. When targeting the M2S/M2GL090 or 150 devices, using SmartDebug does not reset the MSS or HPMS

Workaround: For the affected devices, to prevent the MSS and HPMS from resetting during SmartDebug operation, you must set the def variable **“SMART_DEBUG_DISABLE_JTAG_RESET”** to **“1”** in order to correct the JTAG reset control within the SmartDebug

Note: If you power-cycle, reset the device, or access the JTAG port from any other tool, this will invalidate the SmartDebug session if the SmartDebug GUI is already open. You must close and reopen the SmartDebug tool first before continuing the debugging operations.

Please refer to KI8956 for further information.

Libero

When a Pre-Libero SoC v11.3 project using EDIF netlist flow is changed to Verilog netlist flow, the project will be invalidated post-synthesis.

SAR 58638 – CoreAXI v3.0.112 is dropping the bif connection.

"Using the "Replace Instance Version..." feature with the latest release of CoreAXI results in error messages in the log window. CoreAXI v3.0.112 has new features and the port and parameter lists are not identical to the older versions. This results in errors during the "Replace..." command.

Workaround: Manually open the newly replaced CoreAXI configurator and double check that your settings are as you expect.

SAR 54877 – Block design cannot be used with Verilog flow.

Synplify Pro ME does not write the definition of the blocks in the .vm file. You have to pass them manually to the compile tool.

You can do that from “Organize Input Files -> Organize Source Files” from the right click menu on the tool.

The file you need to pass is the _syn.v files from the blocks (under <project>/designer/<blkname>_blk/

SAR 51880 – Project Archiving tool states are not retained when a Libero Project is uploaded on SVN.

Workaround: Zip the project and upload to SVN in order to retain the tool states.

SAR 50267 – Selecting SMEV RAM available in Fusion’s Advanced Analog System Options dialog degrades the Resolution performance.

In the datasheet we state a resolution of 1/0.25 Deg while using ADC in 10/12 bit mode. When using SMEV RAM we have observed a resolution of 3-4 Deg. in some cases.

SAR 49569 – Libero does not support importing an FDC file. To add constraints for Compile Point, you must open Synplify Pro to add them.

SAR 47957 - SmartFusion2/IGLOO2 RAM Initialization Configurator – Importing Simple-Hex and Motorola-Hex files is not working.

When you try to import Simple-Hex or Motorola-Hex files for initialization for simulation, Libero may crash or the import may fail (content initialized to all zeroes).

Workaround: There is a workaround available that utilizes a *.shx file generated for Fusion. Contact Microsemi Technical Support at soc_tech@microsemi.com for details. Ask for the workaround for SAR 47957.

SAR 46161 - The post-synthesis EDN file will not appear in the design hierarchy until the project is closed and reopened.

SAR 43772 - Linux: The SmartFusion2 configurators for DDR and FICs are missing the diagram describing the details of the block.

This issue will be fixed in a future release.

SAR 42170 - MVN Cross probing is not supported for Path List and Expanded Path View of the Min and Max Analysis windows.

This issue will be fixed in a future release.

SAR 41619 - IGLOO+ hot-swappable option is not displayed correctly in the GUI.

Hot-swappable is always ON for IGLOO+ and cannot be changed. The GUI allows you to check/uncheck this feature, but it is ignored by the tools. These I/Os are always hot swappable.

System Builder

SAR 59407 - VHDL synthesis and simulation issues when multiple Fabric AMBA AXI slaves are added to a FIC subsystem.

If your design is using VHDL flow and if you added more than 2 Fabric AMBA slaves configured as AXI to any of the FIC_0/1 MSS Master Subsystem or FIC_0/1 Fabric Master Subsystem in the System Builder Peripherals page, then you might see errors while running simulation or synthesis for this design.

Workaround: Open the System Builder design as SmartDesign. In the open System Builder component, delete the top level AXI slave BIFs. Promote the CoreAXI slave BIF AXImslave'n' (n>=1) to the top and save. Update the top level SmartDesign containing the System Builder block, save, regenerate, and run synthesis or simulation.

SmartTime

SAR 57220 - 'Restore Defaults' button unchecks inter-clock and recovery, removal checks.

The "Restore Defaults" button is present in the SmartTime Options dialog. Pressing this button unchecks the inter-clock domain and recovery/removal checks options. This is incorrect. The default state is for these two options to be enabled.

Workaround: Set the correct options manually.

SAR 57161 - Automatic hold violation fixing is currently not supported for SmartFusion2 and IGLOO2.

SAR 34365 - Asynchronous Register paths are not displayed in Timing Analysis view.

This issue will be fixed in a future release.

SAR 43767 – Maximize Window button is missing from the title bar for Constraints Editor, Max Analysis and Min Analysis.

Workaround: Double-click the title bar to maximize the window.

SAR 43726 - The exported Tcl file does not include commands to organize SDC files.

Workaround: Requires editing the exported TCL file carefully. This issue will be fixed in a future release.

Libero Firmware Flow

Generated projects for Keil do not compile

Libero-generated Keil projects do not compile. Changes made to the SmartFusion2 CMSIS v2.2.101 are not compatible with the generated projects created by Libero. This will be fixed in a future release.

Workaround: Manually fix the projects.

SoftConsole project generation fails if Java is not installed.

Workaround: Install Java.

Some DirectCore drivers are not added to generated projects

A generated project may not compile due to missing drivers. Some AMBA subsystem topologies are not producing a complete list of required drivers.

Workaround: Manually add the drivers to the project.

SmartFusion2 CMSIS 2.2.101 default UART baud rate change

A change in SmartFusion2 CMSIS default baud rate for the printf function may result in garbage printed to the terminal.

Workaround: Fix the baud rate on the terminal side.

SmartFusion2 CMSIS 2.2.101 includes new linker scripts requiring an update to all existing projects

Existing projects or generated projects using older SmartFusion2 CMSIS versions will fail to link. SmartFusion2 CMSIS 2.2.101 provides more powerful linker script capabilities. However, the previous names are not preserved and replaced.

Solution: Use new linker file names.

Programming

SAR 57456 - Optional procedures are not saved in .pro file.

Running ping on FlashPro5 will report that the programmer is not found.

This error message is incorrect and can be ignored. Message in log:

programmer '00XTYYFF' : Pinging Programmer...

Error: programmer '00XTYYFF' : FP5 delay failed.

Error: programmer '00XTYYFF' : Ping FAILED.

SAR 58993 - Generate Bitstream fails if device name is changed in "Programming Connectivity and Interface" tool.

You will see the bitstream generation error s below in the log window when the Libero design device name is changed in "Programming Connectivity and Interface" tool and then "Generate Bitstream" or "Export Bitstream" tool is run.

: The command 'load_programming_data' failed.

Error: Failure when executing Tcl script. [Line 3]

Error: The Execute Script command failed.

SAR 58063 - For SmartFusion2 and IGLOO2, optional procedures for a programming action configured in Libero are not exported in the Programming Job.

Workaround: Open the programming job project in FlashPro to configure and save this setting.

FlashPro5 is not supported for RHEL 5 and CentOS 5.

Programming Connectivity and Interface TCL support will be added in a future release.

Programming Settings TCL support will be added in a future release.

SVF for SmartFusion2 and IGLOO2 will be available in a future release.

SAR 51767 - Error: The command 'load_programming_data' failed.

During programming file generation if the serialization content files cannot be found, then you will see the following error: "Error: The command 'load_programming_data' failed."

Workaround: Open **Update eNVM Memory Content** and specify a valid path for each serialization content file.

SAR 45867 - STAPL player for SmartFusion2 or IGLOO2 will be available in a future release.

SAR 41069 - Add PDB loading from DDF for Libero environment

You may get an exit 6 idcode failure when chain programming within Libero using a PDB file.

Workaround: Use a STAPL file or use the standalone FlashPro tool for chain programming

SAR 47452 - FlashPro verify and erase errors are reported as programming failures.

If you run programming ACTION VERIFY/ERASE and there is a failure, then the error code will indicate it is a programming failure even though you were running action VERIFY/ERASE.

SmartDebug

SAR 59184 Using SmartDebug functions causes the SmartFusion2 MSS and IGLOO2 HPMS to reset in Libero v11.4 And v11.4SP1

When using the SmartDebug functions, for example Memory Blocks Read or SERDES Debug, etc.., within Libero SoC v11.4 and 11.4SP1 or standalone FlashPro v11.4 and 11.4SP1 the SmartFusion2 MSS and the IGLOO2 HPMS are reset during the debug process. One of the consequences of this issue is that when using the SERDES debug utility this behavior will prevent proper access to the SmartDebug SERDES control and status registers.

The reset behavior will occur on M2S/M2GL005, 010, 025, and 050 devices. When targeting the M2S/M2GL090 or 150 devices, SmartDebug does not reset the MSS or HPMS .

Workaround: For the affected devices, to prevent the MSS and HPMS from resetting during SmartDebug operation, you must set the def variable **“SMART_DEBUG_DISABLE_JTAG_RESET”** to **“1”** in order to correct the JTAG reset control within the SmartDebug .

Note: If you power-cycle, reset the device, or access the JTAG port from any other tool, this will invalidate the SmartDebug session if the SmartDebug GUI is already open. You must close and reopen the SmartDebug tool first before continuing the debugging operations.

Please refer to KI8956 for further information.

SAR 60565 – No support for eNVM debug for M2S/M2GL090 & M2S/M2GL150 devices.

eNVM debug is not supported for M2S/M2GL090 & M2S/M2GL150. An attempt to access Flash Memory debug feature will result in the following error message for these devices:

Error: Unable to access embedded Flash Memory for your selected device: Security settings prevent MSSWR operation: UPWL lock is active, no data is transferred.

SmartDebug will support Flash Memory debug in a future release.

SAR 46847 - eNVM Debug in SmartFusion2 and IGLOO2 disabled due to access restriction to ENVMAHB block by MSSRD/WR command.

Reading Flash Memory page information is limited in SmartFusion2 & IGLOO2 050 and smaller devices due to ENVMAHB access restrictions.

This disables certain Flash Memory page diagnostics. Full support of Flash Memory diagnostics will be added to M2S/M2GL060 and larger devices in a future release.

SAR 54004 - Search in Debug FPGA GUI does not support wild card. This will be supported in a future release.

SmartFusion2 devices will read invalid memory content if the MSS is held in the reset state or M3 is executing invalid microcode programmed into the Flash Memory.

Workaround: Program a valid design. Confirm that the MSS is not in the reset state.

SmartDebug SERDES is not supported for M2S050PP and ES parts.

Synopsys Synplify Pro

SAR 55447 - Compiler Error <btextio.c:1228 NIL file pointer: Cannot write to file. Please check write permissions>.

This issue is under investigation.

Workaround: Remove the synplifypro_ini file from AppData/Roaming and re-run synthesis.

SAR 55543 - The *.so has *.edf option for synthesis_1/2 implementation through Libero.

You can create synthesis_<1/2> implementation by invoking Synplify Pro interactively through Libero. Run synthesis and Libero gets updated accordingly. However, after creating the synthesis_<1/2> implementation if you go back to Libero and change to any different die and run synthesis for synthesis_<1/2> implementation, the synthesis_<1/2> implementation will not be updated correctly. Libero will report the following error:

Unable to find the file 'P:\Test_edif_multiple\synthesis\synthesis_1\dotp_accsub_unsign_asrstn_en.edf', cannot add it to Libero project.

Error: Synthesis failed.

Workaround: After changing to a different die in Libero, invoke Synplify Pro interactively and copy the synthesis implementation to a new name, run synthesis for this new implementation and Libero will be updated correctly.

SAR 46982 - Synplify Pro treats the PLL as a black box

SDC constraints applied to the PLL input do not propagate forward. To actively constrain it; you must constrain both the input and the output of the PLL using the create_clock and create_generated_clock constraints. More information can be found in KI70291.

SAR 46983 - False Path, Multicycle Path and Max delay constraints are not propagated to the SDC file used by Synplify Pro

For more information about constraints consult Chapter 4, Specifying Constraints, in the Synplify Pro User Guide.

Synplify Pro Warning: Unrecognized technology/part/package in Synplify Pro

When executing synthesis using the Libero integrated flow a warning appears if the silicon family, die or package is not present in Synplify Pro. In most cases the design will automatically be mapped to an existing device and continue. If no mapping exists the flow will halt.

Missing Die

```
Unrecognized part [die] specified for device [silicon_family] in
[design_name]:synthesis
```

Design will be mapped to a pre-programmed default and synthesis will proceed.

Missing Package

```
Unrecognized package [package_name] specified for part [die] in
[design_name]:synthesis
```

Design will be mapped to a pre-programmed default and synthesis will proceed.

Missing Silicon Family

```
Warning: Unrecognized technology: [silicon_family]
Unrecognized technology: [silicon_family] in [design_name]:synthesis
```

Synplify Pro halts.

System Requirements

Refer to System Requirements on the web for more information regarding operating systems support and minimum system requirements. 64-bit OS is required for designing SmartFusion2 and IGLOO2 devices.

Setup Instructions for Linux OS can be found on the Libero SoC Documents webpage.

Changes in OS support

Supported

Windows 7, Windows 8.1 *(new)*

RHEL 5* and RHEL 6, CentOS 5* and CentOS 6 *(new)*

** RHEL 5 and CentOS 5 do not support programming using FlashPro5*

Discontinued

32-bit operating systems are no longer supported.

Windows XP is no longer supported.

Synopsys and Mentor Graphics Tools

These tools are included with the Libero SoC v11.4 installation.

Synplify Pro ME 2013.09M SP1-1 Release Notes

ModelSim ME 10.3a

Identify ME 2013.09M SP1-2 Release Notes

Synphony Model Compiler 2014.03M Release Notes

Prerequisite Software: In order to run Synphony Model Compiler ME, you must have MATLAB/Simulink by MathWorks installed with a current license. You cannot run Synphony Model Compiler ME without MATLAB/Simulink.

Download Libero SoC v11.4 SP1

Installation requires Admin privileges.

Windows

Linux

Libero SoC v11.4 SP1 is an incremental service pack and must be installed over Libero SoC v11.4

Download SoftConsole 3.4 SP1

SoftConsole v3.4 requires a service pack to be compatible with Libero SoC 11.4.

Install SoftConsole v3.4 SP1 over SoftConsole v3.4.

Download SoftConsole 3.4 SP1.

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