Libero SoC v11.4 Release Notes

Libero® System-on-Chip (SoC) is the most comprehensive and powerful FPGA design and development software available, providing start-to-finish design flow guidance and support for novice and experienced users alike. Libero SoC combines Microsemi SoC Products Group tools with such EDA powerhouses as Synplify Pro® and Model*Sim*®.

Use Libero SoC v11.4 for designing with Microsemi's SmartFusion2 and SmartFusion SoC FPGAs, and IGLOO2, IGLOO, ProASIC3, and Fusion FPGA families.

Visit the Documents tab on your device page at www.microsemi.com to obtain silicon Datasheets, Silicon User's Guides, Tutorials and Application Notes.

Development Kits and Starter Kits are available.

Note: There are some issues in SERDES blocks and MSS/HPMS Timing Data. These issues are fixed in Libero SoC v11.4 SP1, scheduled for release on September 15, 2014. To find out if you are affected by these issues, and to learn about possible workarounds, refer to the Known Limitations, Issues and Workarounds on page 9.

Contents

What's New in Libero SoC v11.4?

New Device Support

IGLOO2

Die	Package	Speed Grade	Temp Ranges	Free Libero Gold
M2GL005	256 VF	STD, -1	COM, IND	Yes
M2GL005S	256 VF	-1	IND	No
M2GL010	144 VQ	STD, -1	COM, IND	Yes
M2GL010S	144 VQ	-1	IND	No
M2GL010	256 VF	STD, -1	COM, IND	Yes
M2GL010S	256 VF	-1	IND	No
M2GL010T	256 VF	STD, -1	COM, IND	Yes
M2GL010TS	256 VF	-1	IND	No
M2GL025	256 VF	STD, -1	COM, IND	Yes
M2GL025S	256 VF	-1	IND	No
M2GL025T	256 VF	STD, -1	COM, IND	Yes
M2GL025TS	256 VF	-1	IND	No

SmartFusion2

Die	Package	Speed Grade	Temp Ranges	Free Libero Gold
M2S005	256 VF	STD, -1	COM, IND	Yes
M2S005S	256 VF	-1	IND	No
M2S010	144 VQ	STD, -1	COM, IND	Yes
M2S010S	144 VQ	-1	IND	No
M2S010	256 VF	STD, -1	COM, IND	Yes
M2S010S	256 VF	-1	IND	No
M2S010T	256 VF	STD, -1	COM, IND	Yes
M2S010TS	256 VF	-1	IND	No
M2S025	256 VF	STD, -1	COM, IND	Yes
M2S025S	256 VF	-1	IND	No
M2S025T	256 VF	STD, -1	COM, IND	Yes
M2S025TS	256 VF	-1	IND	No

Software Enhancements

Runtime improvements

This release delivers faster:

- Layout for larger devices.
- High-effort Layout.
- Timing Analysis.
- PLL lock simulation for low frequencies.
- System Builder, SmartDesign, and MSS generation.
- File import.

Libero UI Enhancements

Simulation Flow Enhancements:

- Ability to create a HDL or SmartDesign test bench from any node in the Design Hierarchy.
- Ability to run pre-synthesis simulation on any test bench from the Stimulus Hierarchy.

Enhanced configuration data management for MSS, SERDES and FDDR.

Enhanced HDL text editor with:

- Syntax & Block Highlighting
- Comment/uncomment
- Column Editing

Reports can be viewed as soon as they are available when running the Design Flow.

You can now instantiate VHDL files containing these special types in SmartDesign.

- Multidimensional Arrays
- “Record” datatype

HDL+

Management of parameter changes, port changes and HDL links.

Bus Interface Port Mapping Enhancements.

System Builder

- Independent PCIe resets for M2S090/M2GL090. AHBLite Bypass Mode Option for improved throughput.
- AXI direct Master/Slave connection for improved throughput. Memory map fixes.

SERDES

M2S090/M2GL090 devices

- These devices now support independent PCIe resets and also support two PCIe Endpoints with two independent lanes for EPCS protocol.

PCIe Peripheral Initialization

The PCIe Peripheral Initialization sequence has been re-architected to properly configure the PCIe registers. You must upgrade to the latest SERDES core versions and re-generate your design to use the new initialization sequence. For SmartFusion2, you must export the firmware with the latest CMSIS version (v2.2.101) and re-compile your firmware application.

EPCS Configuration

The SERDES configurator has been enhanced to provide an extended set of EPCS configurations.

- Configurable Reference Clock and data rate per lane.
- Flexible lane assignment.
- The pre-defined SGMII, EPCS-125 and EPCS-250 protocols have been removed. SGMII configuration is equivalent to 125MHz Reference Clock and 1250 bit/s (10-bit interface) data rate configuration.

Note: With the new EPCS configurator, the TX and RX bus data widths are always set to 20 bits. If your effective EPCS data width is less than 20 bits, you must slice the TX and RX ports and connect them to the rest of your design. The correct slices are: RX[19:19-width + 1] and TX[width -1:0].

Timing for M2S025/M2GL025 and M2S010/M2GL010 devices

Production (post-silicon) timing and improved min-delay timing analysis.

MIL Temperature Analysis

Custom temp range selection spanning -55~125 allows for timing & power analysis for all SmartFusion2 and IGLOO2 devices.

Test Bench Generation for SmartDesigns

Creation of HDL/SmartDesign test benches available from any node in the Design Hierarchy.

Pre-synthesis simulation of any stimulus files from the Stimulus Hierarchy.

In previous releases Libero automatically generates a test bench when you generate the corresponding SmartDesign. Starting with Libero SoC v11.4 if you regenerate your SmartDesign your auto-generated test-bench will be deleted. If you want to preserve your pre-v11.4 test bench you must save it to a different location.

TCL Enhancements

New user guide with examples: Batch Flow Scripting for SmartFusion2 and IGLOO2

Support for:

- 'Security Policy Manager (SPM)'
- 'Flash*Freeze'
- 'Export Design Summary'

I/O Editor Enhancements

Column-based filtering

Multi-row editing

LPDDR LVCMOS18 support has been added to reduce power

Layout Optimizations

Automatic IO Register Combining to aid in IO timing closure.

Globals (output CCC pin swapping) for increased routing flexibility.

Export Design Summary (Datasheet) Tool for SmartFusion2 and IGLOO2

Datasheet (.xml) will not be generated when the top level (root) SmartDesign component is generated. However, you can export the snapshot of your design summary (datasheet in .html format) to any desired location on disk by using the option 'Tools → Export → Design Summary'.

Export Firmware Tool for SmartFusion2

The firmware directory and the SW IDE project will not be generated when the top level (root) SmartDesign component is generated. You can export the firmware directory and the SW IDE project of your choice (SoftConsole/IAR/Keil) to any desired location on disk by using the 'Export_Firmware' tool in the Libero Design Flow pane.

You must re-export the firmware and recompile it with your application every time you make changes to your MDDR, FDDR, SERDES or MSS configuration. This is required because the initialization of these blocks is performed by the CMSIS SystemInit() function compile with your application. The SystemInit() function uses the data generated by the MDDR, FDDR, SERDES and MSS blocks.

Configure Firmware Cores Tool for SmartFusion2

To view and configure the firmware driver cores corresponding to the CMSIS, MSS peripherals and soft IP peripherals, use the 'Configure Firmware Cores' tool in the Design Flow pane which opens the DESIGN_FIRMWARE window.

Note: If you are regenerating your Firmware project or Firmware directory for any reason, you must upgrade your CMSIS core to version 2.2.101 or later

Programming

Integrated drivers for FlashPro5 hardware for Windows and Linux platforms.

New FlashPro Express programming tool for production programming.

Debug Policy can be enabled within the Security Policy Manager.

Libero programming on Linux with FlashPro5 for SmartFusion2 and IGLOO2.

Programming Recovery and Auto Update in Libero.

Updated Security Policy Manager in Libero.

Libero Export Programming Job tool simplifying job transfers to FlashPro Express.

Updated Export Bitstream tool In Libero allowing users flexibility in customizing the bitstream components and types of security files to be exported.

SmartDebug support for SmartFusion2 and IGLOO2 on Linux with FlashPro5.

Silicon Signature Programming Support.

When device is secured, SmartDebug is allowed when Debug Passkey and User Passkey match.

FlashPro Express - New Production Programming Tool

- Windows supports FlashPro Lite, FlashPro3, FlashPro4, FlashPro5
- Linux supports FlashPro5 only

SoftConsole 3.4 SP1

SoftConsole v3.4 requires a service pack to be compatible with Libero SoC v11.4.

You must use SoftConsole 3.4 SP1, and CMSIS version 2.2.101 or later with Libero SoC v11.4.

Download SoftConsole 3.4 SP1.

Updating Your Design to Libero SoC v11.4

Libero Project Invalidation

With each new update of the Libero SoC design suite come new features, new device support and resolved issues. As the Libero SoC design suite is upgraded it is sometimes required to invalidate Libero projects created with previous versions of Libero SoC. Design invalidation means that the design flow may be reset back to a previous state in the Design Flow or that portions of the design may need to be regenerated. The decision to invalidate a previous Libero SoC project is not taken lightly and every option to provide a backward compatible solution is always considered. The following sections provide information on the conditions for project invalidation with Libero SoC v11.4.

SmartFusion2 and IGLOO2 Project Invalidation Conditions

Embedded Features

In Libero Soc v11.4 the data structures associated with the embedded features of the SmartFusion2 and IGLOO2 have been modified. This includes the System Builder, High Speed Serial Interface (SERDESIF), and the DDR Memory Controller (MDDR and FDDR). If using a design from 11.3, it is not necessary to regenerate these modules, Libero SoC v11.4 will work correctly without any modifications to these blocks. However, if one of the blocks is regenerated, then all of them will need to be regenerated to use the new data structures. When a block is regenerated the design flow will be reset back to the pre-synthesis state.

If a project contains a SERDESIF that is prior to Libero v11.3 then the following warning will be issued and the project will be automatically reset back to the pre-compile state.

Warning: Your design has been invalidated because it contains out-of-date SERDES blocks.

Reasons for updating to the latest version of embedded blocks are listed below.

- SERDESIF - New PCIe initialization and reset scheme (required for PCIe designs).
- SERDESIF - New EPCS data rate and lane selection features.
- SERDESIF - New EPCS reference clock addition when using two or more lanes.
- MSS/FDDR – Addition of the LVCMOS18 type for the MDDR and FDDR LPDDR controllers.
- ALL – Any other resolved issues that have been addressed in this release.

To update to the latest version of the blocks you must replace the embedded cores with the latest version available from the repository and regenerate the design. Re-run Compile.

Updating designs using SERDES_IF

You must update SmartFusion2 and IGLOO2 designs that use SERDES blocks as

described in the following steps:

1. Open your existing Libero 11.3 project
2. If you are using PCIe
    a. Delete each instance of SERDESIF (Note the configuration settings before deleting)
    b. Instantiate SERDESIF versions (High Speed Serial Interface v1.2.103 (for all but the 090T/TS devices)) or (High Speed Serial Interface 2 v1.2.105 (for the 090T/TS devices)) from the IP Catalog
    c. Configure the SERDESIF instances to match your old SERDES configuration settings or equivalent if your previous configuration used one of the pre-defined configurations that have been removed from the SERDES configurator.
    d. Reconnect these new SERDESIF instances to the rest of your design
3. If you are not using PCIe
    a. Right-click on each instance of SERDESIF
    b. Click “Replace Component for Instance” and replace the SERDESIF instance with either High Speed Serial Interface v1.2.103 (for all but the 090T/TS devices) or High Speed Serial Interface 2 v1.2.105 (for the 090T/TS devices)
4. (SmartFusion2 only):
    a. Upgrade your CMSIS Firmware core to 2.2.101using the ‘Configure Firmware’ tool in the Design Flow
    b. Regenerate your Firmware project using the new ‘Export Firmware’ tool in the Design Flow and recompile your application with the exported firmware configuration.

SSTL and HSTL IO

In Libero SoC 11.4 referenced buffer types are no longer supported on certain device pins.

SSTL18I, SSTL18II, HSTLI, and HSTLII

These IO standards are no longer supported in MSIO or MSIOD banks. They are still supported in DDRIO banks.

SSTL15I and SSTL15II

These IO standards are no longer supported when not used with the MDDR and FDDR memory controllers.

If your pre-v11.4 design contains I/O standards on unsupported device pins then the software automatically invalidates your Compile state. The user must change the IO type or move the pin to a valid location in the device.

If your design is affected when you open your project you will see the following message:

Warning: Your design has been invalidated to a pre-Compile state because of unsupported I/O standards.

Resolved Issues

Issues Fixed in v11.4

SAR 48929 - SmartDesign shows incorrect Memory Map for SmartFusion2 FIC_1.

SAR 49025 – System Builder shows incorrect Memory Map for IGLOO2.

SAR 49868 – The Power Report is generated only for the first run when using the Multi-pass Layout option.

SAR 51770 – MSS/HPMS VHDL post-synthesis/post-layout simulation fails for projects created with Libero SoC v11.1 SP3 and earlier.

SAR 52554 – 325 FCSBGA Package and SERDES lane limitations have been addressed.

SAR 53628 - SmartFusion2 and IGLOO2 PCIe registers are not initialized properly in all cases.

SAR 54054 - Secure IP Flow: VHDL compiler directive ‘protect’ treated as illegal syntax.

SAR 54584 - Generic of std_logic in VHDL RTL reports error in Compile for VM flow.

SAR 55035 - PCIe SERDESIF configuration is lost when changing lane width.

SAR 55154 - PCIe SERDESIF reverse x1 mode not linking up.

SAR 55368 - eNVM cannot be accessed from SmartDebug when UPK1 is used to lock eNVM update protection.

SAR 55421 - "Device I/O states During Programming" Option crashing on Linux.

SAR 55517 - Stand-alone Identify Instrumentor error.

Customer Reported SARs fixed in v11.4

Refer to your Technical Support Hotline Case Number to determine if the SAR has been fixed in this release. The case number and SAR are listed below.

SAR	Case Number	Product	Summary
129	1-12375313	Project_Manager	VHDL parser support for VHDL 93 syntax.
6087	1-32101848	Project_Manager	HDL Editor color scheme enhancement.
55110	3642-1576444552	Project_Manager	Failed to create core from design hierarchy.
29635	489394-306510963	Project_Manager	Fixed runtime error while opening SmartDesign Component (VHDL Array Type support).
42440	493642-1078521778	FlashPro Express	FlashPro Linux support.
44158	493642-1131886330	Project_Manager	Support for VHDL user defined data types.
43502	493642-1147728263	SmartDesign	Export datasheet.
43915	493642-1187871652	SmartDesign	SmartDesign incorrectly changes VHDL ports from unsigned to std_logic_vector type.
45965	493642-1252144869	SmartDesign	Add support for VHDL Record in SmartDesign.
47210	493642-1276143212	Project_Manager	Enhancement in stimulus hierarchy.
47422	493642-1316926771 493642-1517479118	Project_Manager	Libero support for referring internal signals in VHDL test bench.
48004	493642-1320859644	FAB_CCC	Output Delay value in CCC with PLL configuration.
48813	493642-1356097722	Project_Manager	ULPI XCLK should not be shown as InOut. It is only Input.
50153	493642-1427026061	Project_Manager	HDL uncomment function not working as expected.
51176	493642-1427891495	Help	Missing ERRORCODE/AUTHERRCODE information in FlashPro online help.
50399	493642-1433992578	SmartDesign	Mismatch in the memory map of FIC0.
49750	493642-1456089123	CAE	Need burst mode for PCIe BFM model with AXI interface.
52243	493642-1495894889	Project_Manager	Libero does not allow direct instantiation method in VHDL.
53203	493642-1526597854	Project_Manager	Constraint Flow is not working.
53683	493642-1529692090	Designer	Synthesis and Compile reports show different resource utilization.
53410	493642-1533321021	SmartGen	Selecting and deselecting outputs in CCC configurator is not behaving correctly in Smartfusion2 device.
53895	493642-1535816992	Microcontroller	Add a new BFM command to fill an array from a text file.
54117	493642-1542294911	Firmware Catalog	IAR Profile needed to generate IAR Firmware from Libero for SmartFusion2.
53899	493642-1552954576 493642-1617555861	Designer	Resource Usage Report Enhancement.
53995	493642-1555950679	Project_Manager	VHDL Array support.
54845	493642-1561745092	FAB_CCC	Describe how we can achieve frequencies lower than 768 kHz.
55152	493642-1564774511	Designer	Update SC_SPI pins for SmartFusion2 and IGLOO2.
54619	493642-1566753874	Synopsys	Synthesis failed because of Internal Error in m_proasic.exe.
54522	493642-1567956542	Project_Manager	Design should not compile after introduction of a syntax error in VHDL.
54495	493642-1568401322	SmartDesign	SmartFusion2 eNVM Data Clients do not show up in memory map.
54846	493642-1571079832	Designer	Unable to constrain JTAG bank to a voltage other than 3.3V.
54899	493642-1574237892	SmartGen	Issue with hex file format for RAM initialization.
54836	493642-1574723646	SmartDesign	MSS_eSRAM0 address range is wrong in memory map table.
55185	493642-1583238591	Project_Manager	Issue while exporting IBIS file for FCS325 package.
55464	493642-1584713909	Micro_Controller	Wind/U X-toolkit Error.
55640	493642-1595355553	Designer	Assertion in "Export BSDL file".
56048	493642-1598905151	Timing	LPDDR power solution for M2S010-VF400.
56351	493642-1598905151	MVN	Update the LPDDR standards based on the production characterization data.
56300	493642-1602265092	Micro_Controller	PCIe AXI/AHB BFM simulation to replicate silicon behavior.

SAR	Case Number	Product	Summary
56297	493642-1608705238	Project_Manager	Error while importing Tcl.
56326	493642-1609904452	Micro_Controller	MDDR clock is not working.
57206	493642-1609904452	SmartGen	Allow option to turn off calibration for DDR.
57188	493642-1616425522	Designer	Designer crash while setting IO attributes through TCL.
57025	493642-1618564625	Project_Manager	Remove External 32KHz xtl osc as source for HPMS/MSS in F*F Hardware Setting GUI.
56809	493642-1622185041	Error_Msg	Generating SERDES in VHDL project gives warning about top_test_SERDES_IF_0_SERDES_IF_pre.vhd.
56941	493642-1624413570	Micro_Controller	AXI WSTRB and WRDATA are not in sync.
57096	493642-1626949610	Project_Manager	Problem creating a core from HDL.
57290	493642-1628501395	Project_Manager	Tool ignores back annotated file HDL selection.
57093	493642-1629224981	Mentor	ModelSim ME fails for a specific project.
53168	493642-1641483259	Designer	NCSim elaboration errors.
58330	493642-1644113861	SmartGen	RAM content manager incorrectly populates with zeros.
58344	493642-1655850735	Project_Manager	Optimization flag error in SoftConsole files used by SmartDesign.
59020	493642-1667451401	Designer	RC Osc clock signal must be on a global network when it drives the Fabric logic directly.
8878	493642-33916303	Project_Manager	Fixed issues related to connecting ports of array types for VHDL Record when using SmartDesign.
31614	493642-38237973	SmartDesign	Conflicts between signal name and macro name causes post-synthesis simulation to fail.
35631	493642-515129313	Project_Manager	Support for defining multiple entities in single VHDL file.
36604	493642-616782013	FlashPro Express	Linux programming support.
38461	493642-814259074	Project_Manager	HDL cannot delete from disk.
21655	493642-882588725 493642-51581943 493642-1252144869	SmartDesign	Add support for VHDL 'record' structure in SmartDesign.
39944	493642-930895145	Project_Manager	Remove “Open datasheet for details" error message for IP Components.
51401	93642-1470559328	Project_Manager	MSS Datasheet generated by Libero is not updated after user makes changes to the MSS.

Known Limitations, Issues and Workarounds

Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines the InstallShield Wizard displays a message stating:

The installation of Microsoft Visual C++ 2005 SP1 Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Select **Yes** and the installation will complete successfully.

SmartFusion2 and IGLOO2

SAR 60230 – When moving a project from Libero SoC v11.3 to 11.4 with SERDES, Replace Instance results in an invalid configuration of the design after Generation

The replace instance feature does not work correctly when upgrading a project from Libero SoC v11.3 to 11.4. You must delete the existing SERDES instance and instantiate a new one as described in the section, Updating Your Design to Libero SoC v11.4 on page 1.

SAR60102 – PCIe BAR2 and BAR3 settings incorrect with SERDESIF version 1.2.102

Version 1.2.102 of SERDES_IF does not correctly configure the PCIe BAR2 and BAR3 windows. You must use SERDES_IF version 1.2.103 with Libero 11.4

SAR60089 – MSS Timing Data is optimistic

Timing data for the SmartFusion2 MSS and IGLOO2 HPMS is optimistic; SmartTime may report that a design has no violation but the design may not be functional on silicon. This issue is fixed in Libero 11.4 SP1 which is planned for release on September 15, 2014. You must use 11.4 SP1 to have correct timing analysis for path to/from the MSS/HPMS block.

SAR 46571 - M2S050 has only one Oscillator

When you instantiate the Oscillator in your design and also use MSS RTC, the Clock Source of the RTC must match the clock source used in the Oscillator. For example, configuring the RTC with Clock Source set to 32 KHz RTC Crystal Oscillator while the Oscillator block is configured with the External Main Crystal Oscillator set to 5 MHz is invalid. The frequencies must match.

MIL Temp Removed from 400 VF, 676 FBGA & 896 FBGA packages

Military Temperature for all SmartFusion2 and IGLOO2 packages was introduced in V11.2. Subsequently, we decided to offer MIL Temp only for 484 FBGA and 1152 FC packages.

If you started a design using Libero SoC v11.2 and selected MIL Temp for any 400 VF, 676 FBGA or 896 FBGA packages, when you open the project in Libero SoC v11.3 the software will crash. Please contact soc_tech@microsemi.com for instructions on how to modify your project so that it can be opened in the current release.

For IGLOO2 projects use System Builder for the following cores; do not use these cores from the Catalog directly.

- DDR Memory Controller
- CoreConfigP
- CoreResetP
- CoreConfigMaster

SAR 58852 – Back-annotated netlist created using a previous release will be invalidated when the project is opened in Libero SoC v11.4.

MSS and SERDES timing has been updated in the simulation models necessitating invalidation of the back-annotated netlist.

SmartFusion2/IGLOO2: Using SmartDebug functions causes the MSS and HPMS to reset in Libero v11.4

When using the SmartDebug functions, for example Memory Blocks Read or SERDES Debug, etc.., within Libero SoC v11.4 or standalone FlashPro v11.4 the MSS (in SmartFusion2) and the HPMS (in IGLOO2) are reset during the debug process. One of the consequences of this issue is that when using the SERDES debug utility this behavior will prevent proper access to the SmartDebug SERDES control and status registers.

The reset behavior will occur on M2S/M2GL 005, 010, 025, and 050 devices. When targeting the M2S/M2GL 090, 100 or 150 devices, using SmartDebug does not reset the MSS or HPMS

Workaround: For the affected devices, to prevent the MSS and HPMS from resetting during SmartDebug operation, you must set the def variable **"SMART_DEBUG_DISABLE_JTAG_RESET"** to **"1"** in order to correct the JTAG reset control within the SmartDebug

Note: If you power-cycle, reset the device, or access the JTAG port from any other tool, this will invalidate the SmartDebug session if the SmartDebug GUI is already open. You must close and reopen the SmartDebug tool first before continuing the debugging operations.

Please refer KI8956 for any further information

Libero

When a Pre-Libero SoC v11.3 project using EDIF netlist flow is changed to Verilog netlist flow, the project will be invalidated post-synthesis.

SAR 59212 - Export Design Summary sometimes results in an empty html file => 0 KB

You may observe that the html datasheet that is exported using Tools → Export → Design Summary is empty.

Workaround: There's no workaround. This will be fixed in the next release.

SAR 58638 – CoreAXI v3.0.112 is dropping the bif connection

"Using the "Replace Instance Version..." feature with the latest release of CoreAXI results in error messages in the log window. CoreAXI v3.0.112 has new features and the port and parameter lists are not identical to the older versions. This results in errors during the "Replace..." command.

Workaround: Manually open the newly replaced CoreAXI configurator and double check that your settings are as you expect.

SAR 54877 – Block design cannot be used with Verilog flow.

Synplify Pro ME does not write the definition of the blocks in the .vm file. You have to pass them manually to the compile tool.

You can do that from "Organize Input Files -> Organize Source Files" from the right click menu on the tool.

The file you need to pass is the *_syn.v files from the blocks (under <project>/designer/<blkname>*_blk/

SAR 51880 – Project Archiving tool states are not retained when a Libero Project is uploaded on SVN

Workaround: Zip the project and upload to SVN in order to retain the tool states.

SAR 50267 – Selecting SMEV RAM available in Fusion's Advanced Analog System Options dialog degrades the Resolution performance

In the datasheet we state a resolution of 1/0.25 Deg while using ADC in 10/12 bit mode. When using SMEV RAM we have observed a resolution of 3-4 Deg. in some cases.

SAR 49569 – Libero does not support importing an FDC file. To add constraints for Compile Point, you must open Synplify Pro to add them.

SAR 47957 - SmartFusion2/IGLOO2 RAM Initialization Configurator – Importing Simple-Hex and Motorola-Hex files is not working

When you try to import Simple-Hex or Motorola-Hex files for initialization for simulation, Libero may crash or the import may fail (content initialized to all zeroes).

Workaround: There is a workaround available that utilizes a *.shx file generated for Fusion. Contact Microsemi Technical Support at soc_tech@microsemi.com for details. Ask for the workaround for SAR 47957.

SAR 46161 - The post-synthesis EDN file will not appear in the design hierarchy until the project is closed and reopened.

SAR 43772 - Linux: The SmartFusion2 configurators for DDR and FICs are missing the diagram describing the details of the block

This issue will be fixed in a future release.

SAR 42170 - MVN Cross probing is not supported for Path List and Expanded Path View of the Min and Max Analysis windows

This issue will be fixed in a future release.

SAR 41619 - IGLOO+ hot-swappable option is not displayed correctly in the GUI

Hot-swappable is always ON for IGLOO+ and cannot be changed. The GUI allows you to check/uncheck this feature, but it is ignored by the tools. These I/Os are always hot swappable.

System Builder

SAR 59407 - VHDL synthesis and simulation issues when multiple Fabric AMBA AXI slaves are added to a FIC subsystem.

If your design is using VHDL flow and if you added more than 2 Fabric AMBA slaves configured as AXI to any of the FIC_0/1 MSS Master Subsystem or FIC_0/1 Fabric Master Subsystem in the System Builder Peripherals page, then you might see errors while running simulation or synthesis for this design.

Workaround: Open the System Builder design as SmartDesign. In the open System Builder component, delete the top level AXI slave BIFs. Promote the CoreAXI slave BIF AXImslave'n' (n>=1) to the top and save. Update the top level SmartDesign containing the System Builder block, save, regenerate, and run synthesis or simulation.

SmartTime

SAR 57161 - Automatic hold violation fixing is currently not supported for SmartFusion2 and IGLOO2.

SAR 34365 - Asynchronous Register paths are not displayed in Timing Analysis view

This issue will be fixed in a future release.

SAR 43767 – Maximize Window button is missing from the title bar for Constraints Editor, Max Analysis and Min Analysis

Workaround: Double-click the title bar to maximize the window.

SAR 43726 - The exported Tcl file does not include commands to organize SDC files.

Workaround: Requires editing the exported TCL file carefully. This issue will be fixed in a future release.

Programming

SAR 59220 - Export Bitstream, Export Programming Job and Generate Bitstream will fail if DPK is not entered in the Security Policy Manager

In the Security Policy Manager, if you only select the "Restrict external Fabric/eNVM digest check request via JTAG and SPI" option in Debug Policy without entering the DPK, then Export Bitstream, Export Programming Job and Generate Bitstream will fail.

Workaround: Always enter DPK if Debug Policy is used.

SAR 58993 - Generate Bitstream fails if device name is changed in "Programming Connectivity and Interface" tool

You will see the bitstream generation error s below in the log window when the Libero design device name is changed in "Programming Connectivity and Interface" tool and then "Generate Bitstream" or "Export Bitstream" tool is run.

Error: The command 'load_programming_data' failed.

Error: Failure when executing Tcl script. [Line 3]

Error: The Execute Script command failed.

SAR 58063 - For SmartFusion2 and IGLOO2, optional procedures for a programming action configured in Libero are not exported in the Programming Job.

Workaround: Open the programming job project in FlashPro to configure and save this setting.

FlashPro5 is not supported for RHEL 5 and CentOS 5.

Programming Connectivity and Interface TCL support will be added in a future release.

Programming Settings TCL support will be added in a future release.

SVF for SmartFusion2 and IGLOO2 will be available in a future release.

SAR 51767 - Error: The command 'load_programming_data' failed.

During programming file generation if the serialization content files cannot be found, then you will see the following error: "Error: The command 'load_programming_data' failed."

Workaround: Open **Update eNVM Memory Content** and specify a valid path for each serialization content file.

SAR 45867 - STAPL player for SmartFusion2 or IGLOO2 will be available in a future release.

SAR 41069 - Add PDB loading from DDF for Libero environment

You may get an exit 6 idcode failure when chain programming within Libero using a PDB file.

Workaround: Use a STAPL file or use the standalone FlashPro tool for chain programming

SAR 47452 - FlashPro verify and erase errors are reported as programming failures.

If you run programming ACTION VERIFY/ERASE and there is a failure, then the error code will indicate it is a programming failure even though you were running action VERIFY/ERASE.

SmartDebug

SAR 59184 - Workaround for SmartFusion2 to prevent MSS resets when SmartDebug is opened.

The following devices will have MSS reset upon any interaction of SmartDebug with the device:

M2S/M2GL 005 Step Mark 0

M2S/M2GL 010 Step Mark 0

M2S/M2GL 025 Step Mark 0

M2S/M2GL 050 Step Mark 0

This behaviour is exhibited by the silicon issue causing MSS reset upon JTAG reset operation.

JTAG reset can be disabled inside the SmartDebug GUI session by setting SMART_DEBUG_DISABLE_JTAG_RESET DEF variable to “1”.

Try to setup and start debug session after opening SmartDebug GUI. Note that setting the DEF variable does not disable JTAG reset upon opening and closing SmartDebug GUI session. Power-cycling, resetting device or accessing JTAG port from any other tool will invalidate SmartDebug GUI session.

SAR 54004 - Search in Debug FPGA GUI does not support wild card. This will be supported in a future release.

SmartFusion2 devices will read invalid memory content if the MSS is held in the reset state or M3 is executing invalid microcode programmed into the Flash Memory.

Workaround: Program a valid design. Confirm that the MSS is not in the reset state.

SmartDebug SERDES is not supported for M2S050PP and ES parts.

Synopsys Synplify Pro

SAR 55447 - Compiler Error <btextio.c:1228 NIL file pointer: Cannot write to file. Please check write permissions>

This issue is under investigation.

Workaround: Remove the synplifypro_ini file from AppData/Roaming and re-run synthesis.

SAR 55543 - The *.so has *.edf option for synthesis_1/2 implementation through Libero

You can create synthesis_<1/2> implementation by invoking Synplify Pro interactively through Libero. Run synthesis and Libero gets updated accordingly. However, after creating the synthesis_<1/2> implementation if you go back to Libero and change to any different die and run synthesis for synthesis_<1/2> implementation, the synthesis_<1/2> implementation will not be updated correctly. Libero will report the following error:

Unable to find the file 'P:\Test_edif_multiple\synthesis\synthesis_1\dotp_accsub_unsign_asrstn_en.edf', cannot add it to Libero project.

Error: Synthesis failed.

Workaround: After changing to a different die in Libero, invoke Synplify Pro interactively and copy the synthesis implementation to a new name, run synthesis for this new implementation and Libero will be updated correctly.

SAR 46982 - Synplify Pro treats the PLL as a black box

SDC constraints applied to the PLL input do not propagate forward. To actively constrain it; you must constrain both the input and the output of the PLL using the create_clock and create_generated_clock constraints. More information can be found in KI70291.

SAR 46983 - False Path, Multicycle Path and Max delay constraints are not propagated to the SDC file used by Synplify Pro

For more information about constraints consult Chapter 4, Specifying Constraints, in the Synplify Pro User Guide.

Synplify Pro Warning: Unrecognized technology/part/package in Synplify Pro

When executing synthesis using the Libero integrated flow a warning appears if the silicon family, die or package is not present in Synplify Pro. In most cases the design will automatically be mapped to an existing device and continue. If no mapping exists the flow will halt.

Missing Die

```
Unrecognized part [die] specified for device [silicon_family] in
[design_name]:synthesis
```

Design will be mapped to a pre-programmed default and synthesis will proceed.

Missing Package

```
Unrecognized package [package_name] specified for part [die] in
[design_name]:synthesis
```

Design will be mapped to a pre-programmed default and synthesis will proceed.

Missing Silicon Family

```
Warning: Unrecognized technology: [silicon_family]
Unrecognized technology: [silicon_family] in [design_name]:synthesis
```

Synplify Pro halts.

System Requirements

Refer to System Requirements on the web for more information regarding operating systems support and minimum system requirements. 64-bit OS is required for designing SmartFusion2 and IGLOO2 devices.

Setup Instructions for Linux OS can be found on the Libero SoC Documents webpage.

Changes in OS support

Supported

Windows 7, Windows 8.1 *(new)*

RHEL 5* and RHEL 6, CentOS 5* and CentOS 6 *(new)*

** RHEL 5 and CentOS 5 do not support programming using FlashPro5*

Discontinued

32-bit operating systems are no longer supported.

Windows XP is no longer supported.

Synopsys and Mentor Graphics Tools

These tools are included with the Libero SoC v11.4 installation.

Synplify Pro ME 2013.09M SP1-1 Release Notes

ModelSim ME 10.3a

Identify ME 2013.09M SP1-2 Release Notes

Synphony Model Compiler 2014.03M Release Notes

Prerequisite Software: In order to run Synphony Model Compiler ME, you must have MATLAB/Simulink by MathWorks installed with a current license. You cannot run Synphony Model Compiler ME without MATLAB/Simulink.

Download Libero SoC v11.4

Installation requires Admin privileges.

Windows

Linux

SoftConsole v3.4 SP1 should be installed over SoftConsole v3.4 for use with Libero SoC v11.4

SoftConsole 3.4 SP1

SoftConsole v3.4 requires a service pack to be compatible with Libero SoC 11.4

Download SoftConsole 3.4 SP1

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