
Accessing External SDRAM through Fabric

Libero SoC Flow Tutorial for the SmartFusion2 SoC FPGA

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Abbreviation Used

- cSoC – Customizable system-on-chip
- MSS – Microcontroller subsystem
- SDR SDRAM – Single data rate synchronous dynamic Random Access Memory
- SMC_FIC – Soft Memory Controller – Fabric Interface Controller
- CCC – Clock conditioning circuits
- MSS CCC – CCC block inside the MSS component
- Fabric CCC – CCC block instantiated inside the FPGA fabric
- DDR – Double data rate memory controller
- MDDR – DDR controller inside the MSS component.
- BFM – Bus functional model

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Accessing External SDRAM through Fabric

Introduction

This tutorial shows how to create a hardware design for accessing an external SDR SDRAM and functionally verify the design using simulation. A CoreSDR_AXI IP is used in SmartFusion[®]2 system-on-chip (SoC) field programmable gate array (FPGA) devices for interfacing the external SDR SDRAM memory with the ARM[®] Cortex[™]-M3 processor, which is the master for this design. The CoreSDR_AXI IP has a 64-bit AXI bus interface for communicating to the Cortex-M3 processor. The CoreSDR_AXI IP generates the inputs for the SDR SDRAM memory and handles the timing parameters for the input signals of the SDR SDRAM memory.

Upon completion of tutorial, you will be familiar with the following:

- Creating a Libero[®] System-on-Chip (SoC) v11.3 project using a SmartFusion2 SoC FPGA
- Updating the IP catalog by downloading the latest versions of the IP cores
- Configuring the various hardware blocks using SmartDesign
- Configuring the MDDR and CCC blocks of the microcontroller subsystem (MSS) component
- Generating the microcontroller subsystem (MSS) component
- Integrating the various hardware blocks in SmartDesign and generating the final top-level component
- Performing functional level verification of the design using AMBA AXI bus functional model (BFM) simulation in Mentor Graphics ModelSim[®] simulator.
- Using the ModelSim GUI to see the various design signals in the Waveform window of ModelSim.

Tutorial Requirements

Requirements and Details

Table 1 • Reference Design Requirements and Details

Reference Design Requirements and Details	Description
Hardware Requirements	
Host PC or Laptop	Any 64-bit Windows Operating System
Software Requirements	
Libero SoC	11.3

Project Files

The project files associated with this tutorial can be downloaded from Microsemi website: http://www.microsemi.com/soc/download/rsc/?f=SmartFusion2_SDRAM_Tutorial_DF. The project files associated with this tutorial include the following:

- Source
- Solution
- A readme file

Refer to the readme file for the complete directory structure.

Design Overview

The design demonstrates read/write access to an external slave SDR SDRAM memory using the SmartFusion2 SoC FPGA. Inside the SmartFusion2 SoC FPGA, the Cortex-M3 processor acts as the master and performs the read/write transactions on the external slave memory. A soft SDRAM controller, CoreSDR_AXI, is implemented inside the FPGA fabric of the SmartFusion2 SoC FPGA and provides the interface between the Cortex-M3 processor master and the slave SDRAM memory. The CoreSDR_AXI IP has a 64-bit AMBA AXI interface on one side, which communicates with the Cortex-M3 processor through the AXI interface. On the other side of the CoreSDR_AXI are the SDRAM memory interface signals, which go as an input to the external SDRAM memory through the FPGA I/Os of the SmartFusion2 SoC FPGA. The CoreSDR_AXI IP takes care of converting the AXI transactions into the SDRAM memory read/write transactions with appropriate timing generation. It also handles the appropriate command generation for write/read/refresh/precharge operations required for SDRAM memory.

The Cortex-M3 processor resides in the microcontroller subsystem (MSS) block of the SmartFusion2 SoC FPGA. The MSS contains another block called the DDR Bridge. This block is responsible for managing the read/write requests from the various masters to the DDR controller in the MSS, called the MDDR block, or interfacing with external bulk memories such as SDR SDRAM via fabric. This fabric interface for the external bulk memories is called the SMC_FIC.

Either the MDDR controller or the SMC_FIC can be enabled at a given time. The MDDR controller is disabled when the SMC_FIC path is active. The fabric side of the SMC_FIC can be configured for either one or two 32-bit AHB-Lite interfaces or an AXI64 interface. The enabling of the SMC_FIC path as well as its interface towards the fabric side of the SMC_FIC can be configured through MSS configurator, as discussed in the tutorial.

In this design, you configure the MDDR block to bring out the 64-bit AXI interface to the fabric through the SMC_FIC.

In the SmartFusion2 SoC FPGA device, there are six clock conditioning circuits (CCCs) inside the Fabric and one CCC block inside the MSS. Each of the CCC blocks has an associated PLL. These CCC blocks and their PLLs provide many clock conditioning capabilities such as clock frequency multiplication, clock division, phase shifting, and clock-to-output or clock-to-input delay canceling. The CCC blocks inside the fabric can directly drive the global routing buffers inside the fabric, which provides a very low skew clock routing network all throughout the FPGA fabric. In this design, you will configure both the MSS CCC and the fabric CCC blocks to generate the clocks for the various elements inside the MSS and the fabric.

In the SmartFusion2 SoC FPGA device there are three oscillator sources – one on-chip 25 MHz–50 MHz RC oscillator, on-chip 1 MHz RC oscillator, and an external main crystal oscillator. In this design, you will configure the 25 MHz–50 MHz on-chip oscillator to provide the clock input for the fabric CCC block, which in turn will drive the clocks to all the design blocks, including the MSS block.

Figure 1 shows the top-level block diagram of the design.

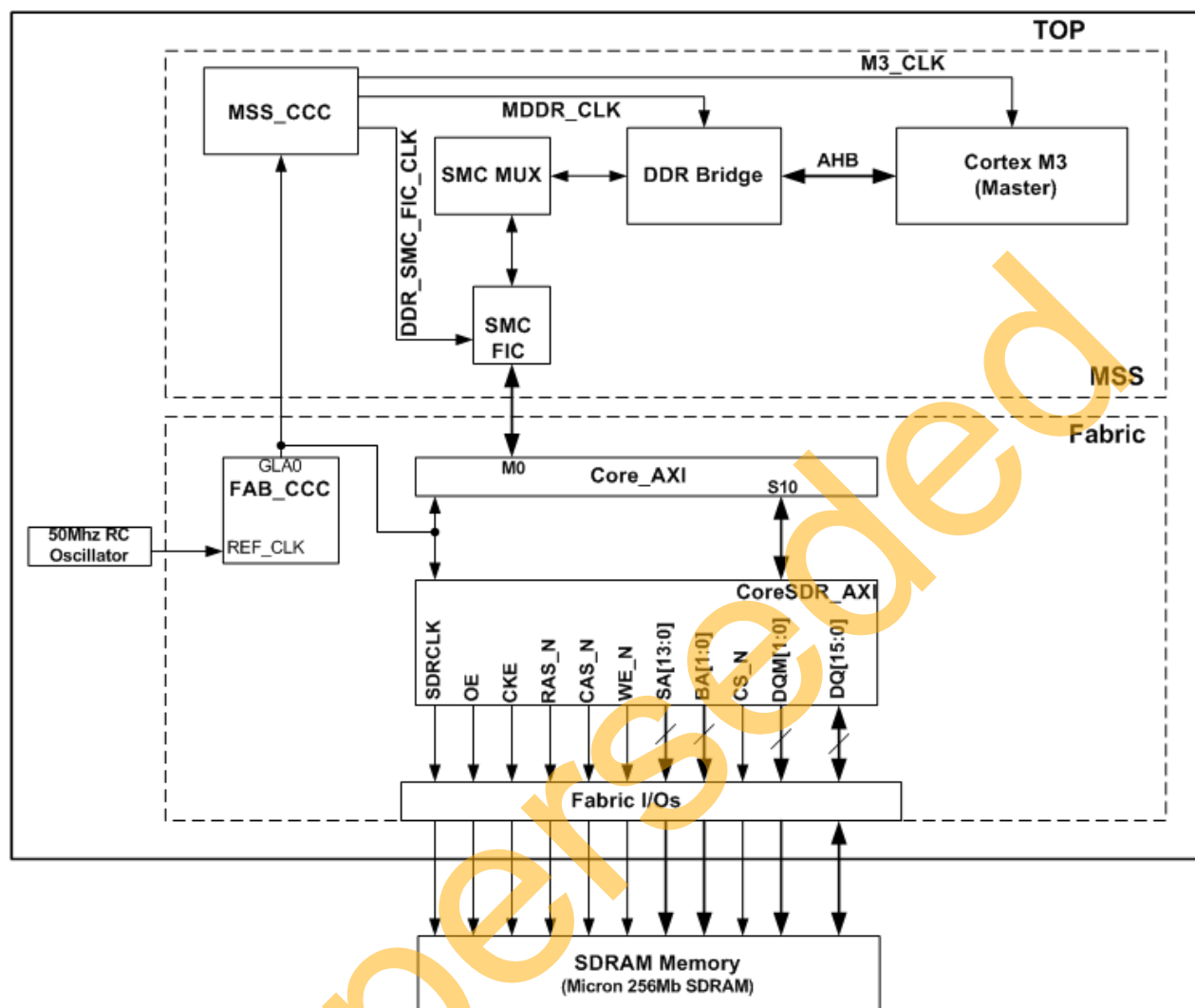


Figure 1. Top-Level Block Diagram

Design Steps

Step 1: Creating a Libero SoC Project

1. Launch Libero SoC v11.3.
2. From the **Project** menu, select **New Project**. Enter the information as displayed in [Figure 3](#).
 - Name : Access_EXT_SDRAM
 - Location: Select an appropriate location (For example, C:/Microsemi_prj)
 - Preferred HDL Type: Leave as Verilog.
 - Family: SmartFusion2
 - Die: M2S050T
 - Package: 896 FBGA
 - Speed: STD
 - Core Voltage(V):1.2
 - Operating Conditions: COM
 - PLL Supply Voltage(V):2.5
3. Select the MSS core in the **Design Templates and Creators** section of the **New Project** window. If the selected MSS core version appears in italics, it means that the selected MSS Core is not available in the vault and it needs to be downloaded. To download select the MSS core and click **OK**. The tool will prompt for downloading the MSS core, click **Yes** on the message prompt. The tool will download the selected MSS core, and then click **OK** on the **New Project** window.

If the selected MSS core appears in normal font, as shown in [Figure 2](#), which indicates that the MSS core is present in vault and it does not require to be downloaded. Click **OK** on the **New Project** window.

Note: The download process requires internet connection to the machine.

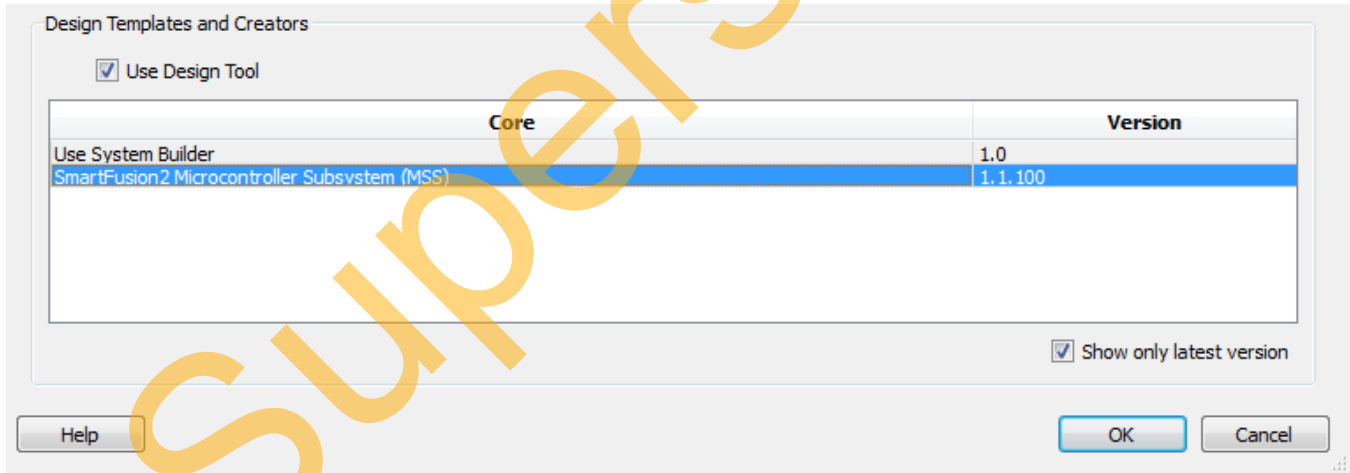
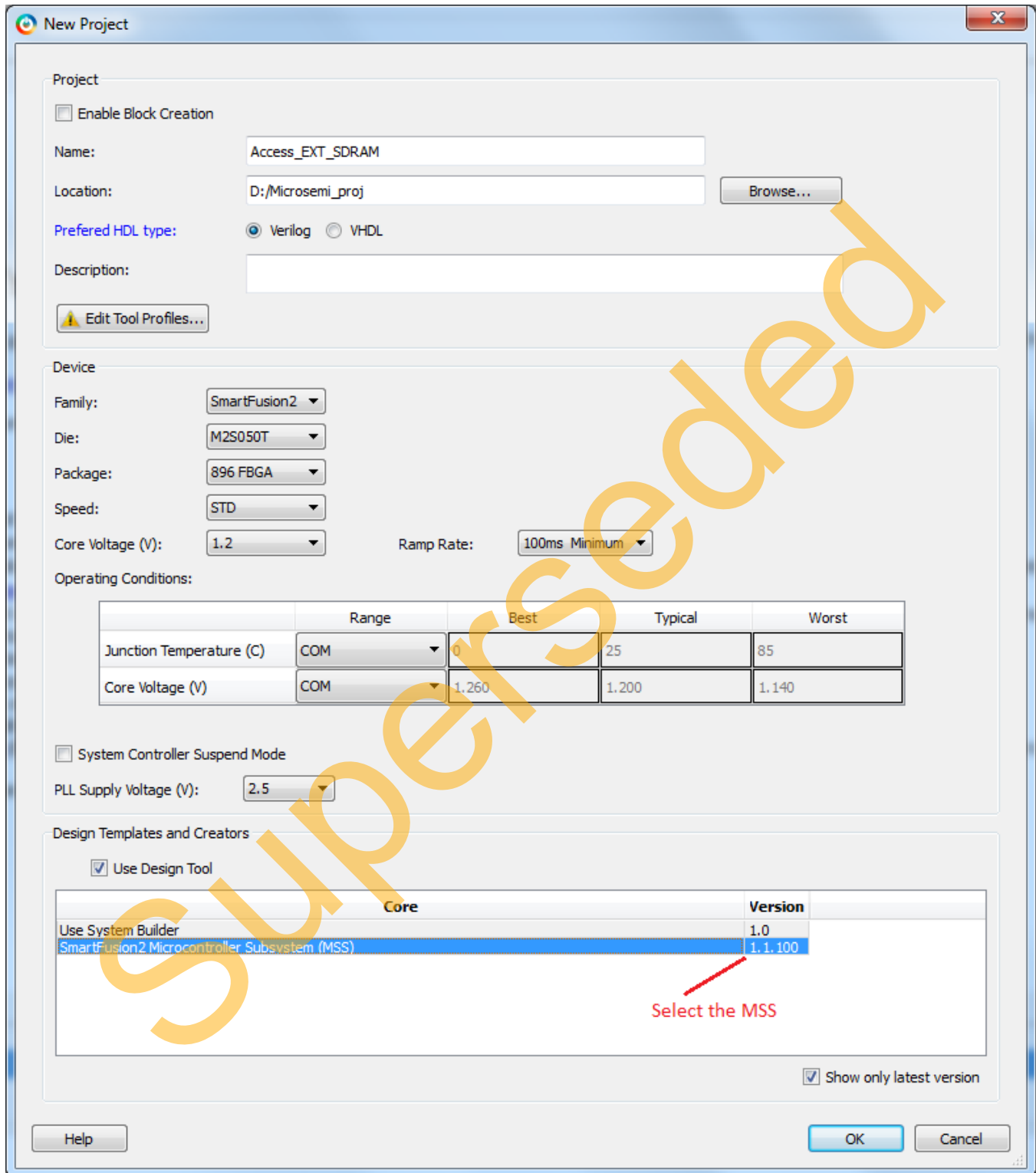


Figure 2. MSS Version

The New Project window is displayed, as shown in Figure 3.



The New Project dialog box is shown with the following settings:

- Project:**
 - ☐ Enable Block Creation
 - Name: Access_EXT_SDRAM
 - Location: D:/Microsemi_proj (Browse... button)
 - Preferred HDL type: ☒ Verilog ☐ VHDL
 - Description: (empty)
 - Edit Tool Profiles... button
- Device:**
 - Family: SmartFusion2
 - Die: M2S050T
 - Package: 896 FBGA
 - Speed: STD
 - Core Voltage (V): 1.2
 - Ramp Rate: 100ms Minimum
 - Operating Conditions:
- Operating Conditions Table:**
- System Controller Suspend Mode:**
 - ☐ System Controller Suspend Mode
 - PLL Supply Voltage (V): 2.5
- Design Templates and Creators:**
 - ☒ Use Design Tool
 - Table with Core and Version columns:

Red arrow pointing to the 'SmartFusion2 Microcontroller Subsystem (MSS)' row in the Design Templates and Creators table:

Select the MSS

Buttons: Help, OK, Cancel

Figure 3. New Project Dialog Box

Step 2: Updating IP Catalog

1. The project is created and the Libero SoC window is displayed, as shown in Figure 4. The **SmartDesign** window opens up and a project named Access_EXR_SDRAM is created with the instantiation of the MSS component.

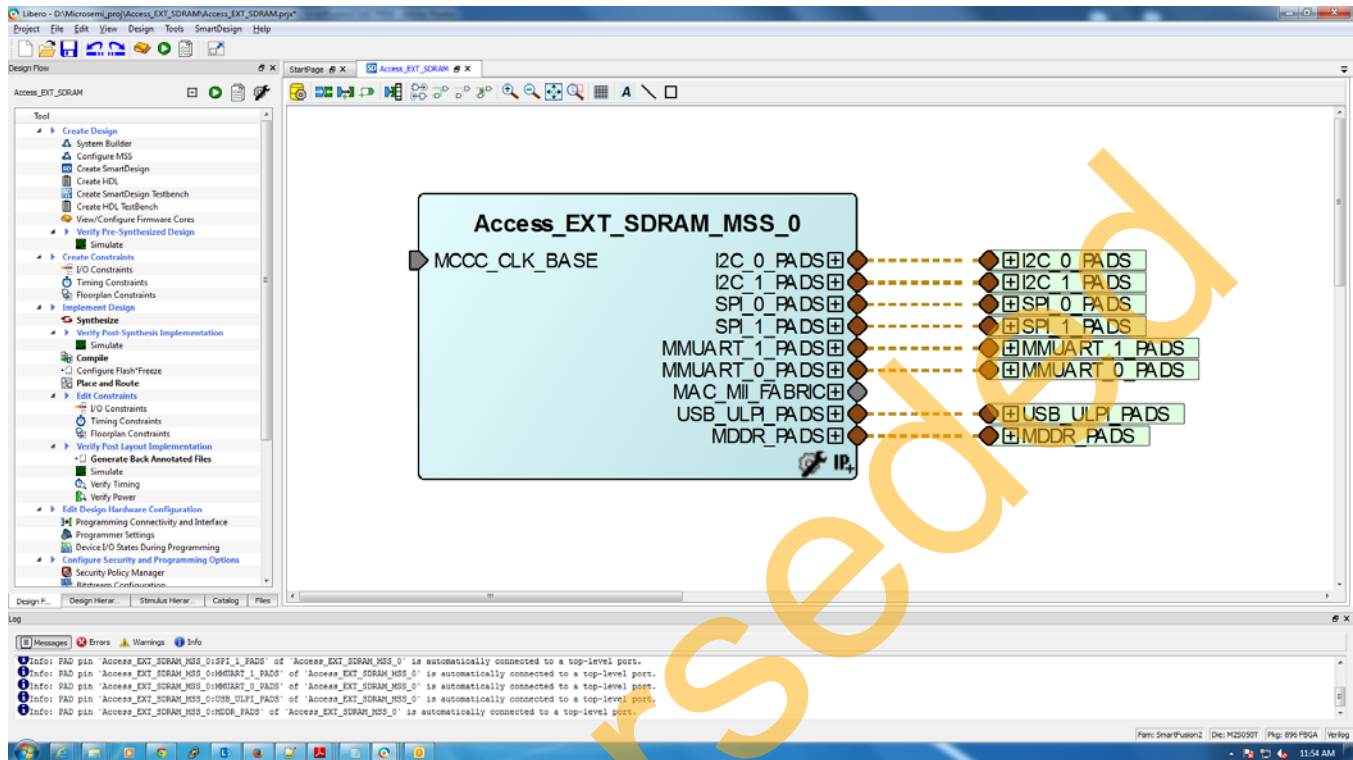


Figure 4. The Libero Window on Completion of New Project Creation Wizard

- Click the **Catalog** tab, as shown in Figure 5. If a message is displayed as “New cores are available”, click **Download them now!** to download all the latest versions of the IP cores.

Note: This process requires internet connection to the machine.

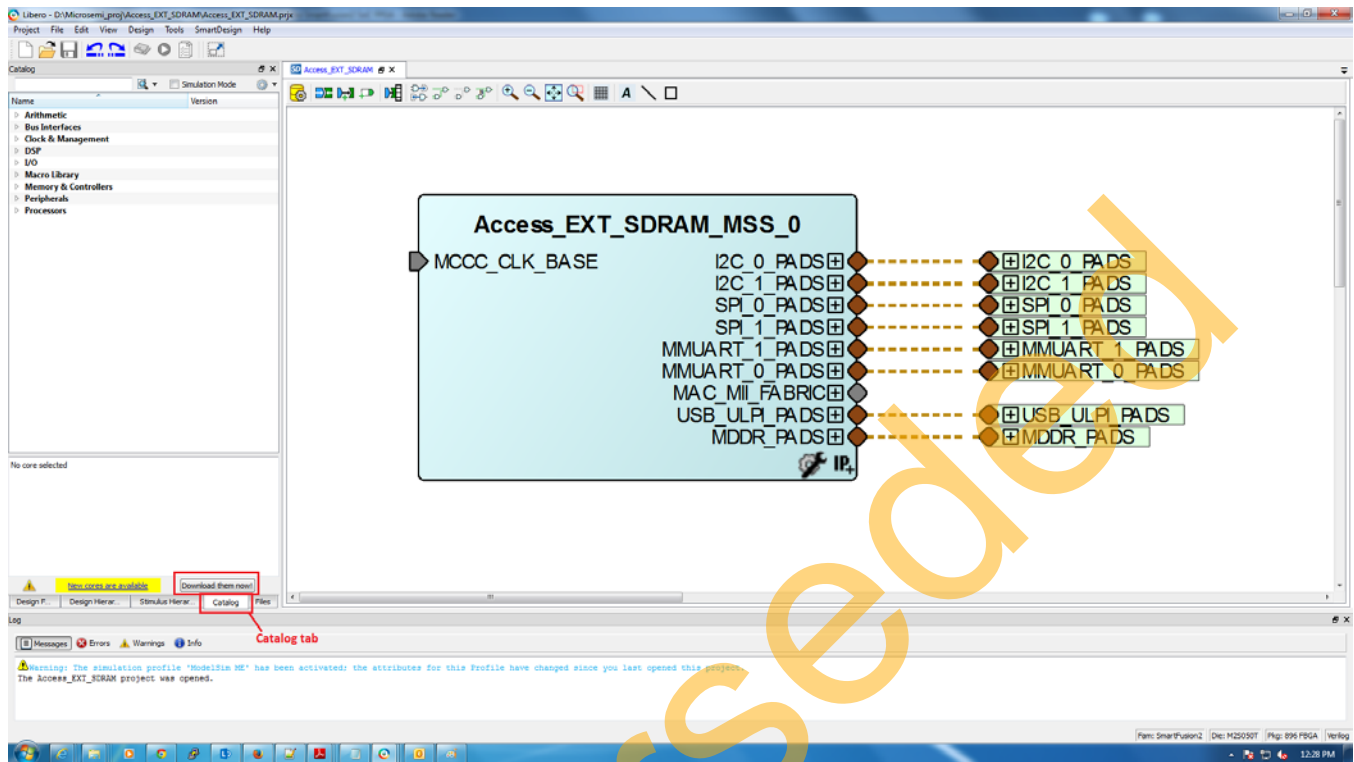


Figure 5. Updating the Catalog

Step 3: Configuring MSS Peripherals

1. Double-click **Access_EXT_SDRAM_MSS_0** to configure the MSS. The MSS is displayed in the SmartDesign canvas in a new tab, as shown in [Figure 6](#).

The enabled MSS blocks are highlighted in blue and can be configured to be included in the hardware. The disabled peripherals are shown in gray.

To disable a peripheral that is not required, right-click the peripheral block and clear the **Disable** check box, as shown in [Figure 7](#), or clear the check box in the lower right corner of the peripheral box. The box turns gray to indicate that the peripheral has been disabled. Disabled peripherals can be enabled by either selecting the check box in the lower right corner of the peripheral box or by right-clicking the peripheral block and selecting the **Enable** check box. An enabled peripheral is shown in [Figure 8](#).

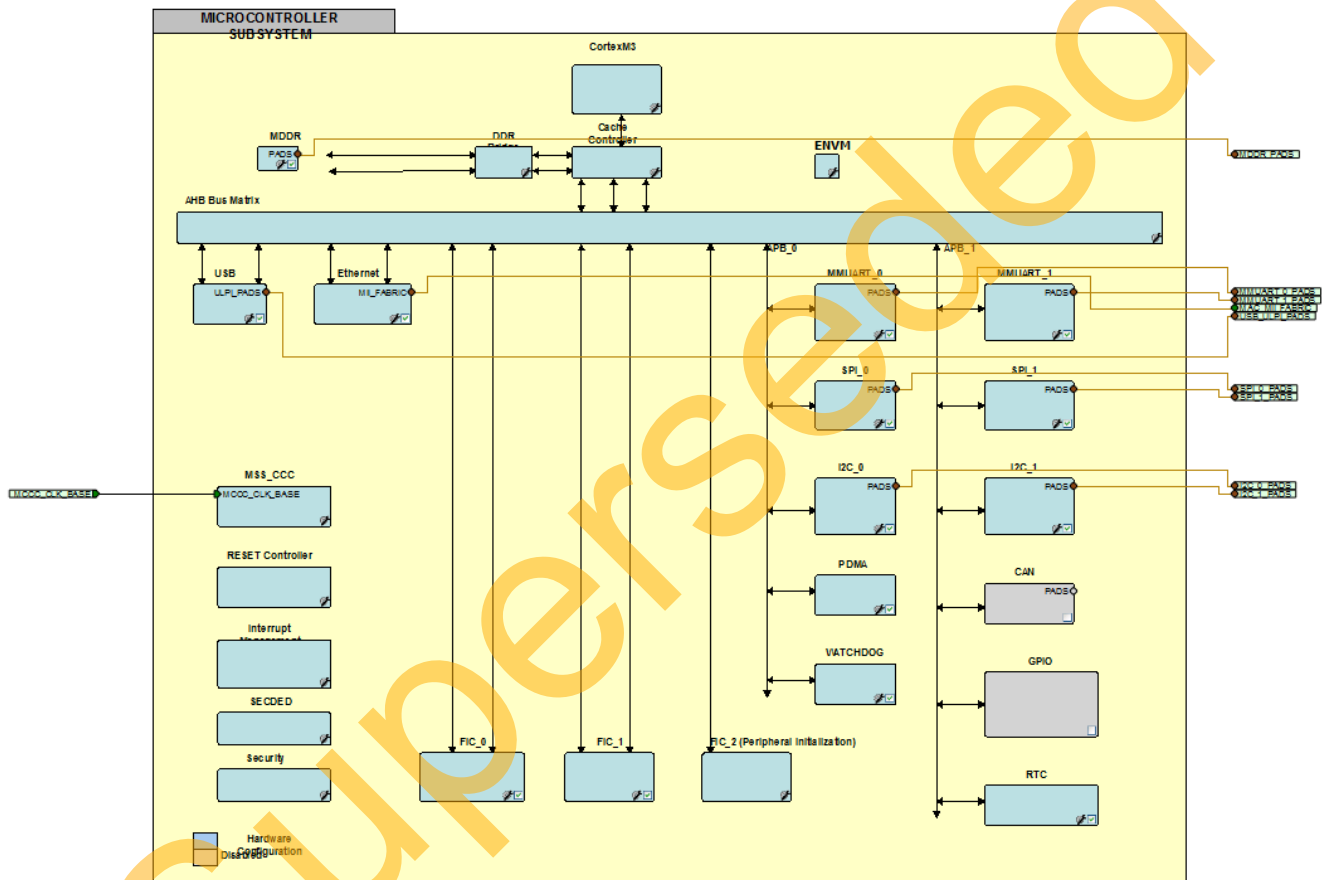


Figure 6. MSS in the SmartDesign Canvas

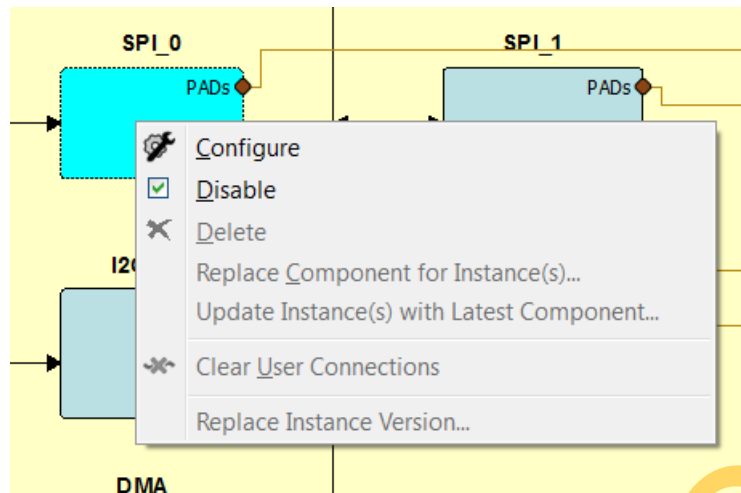


Figure 7. Right-click an Enabled Peripheral Block

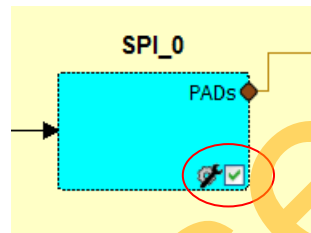


Figure 8. Enabling the Peripheral

2. Disable the following peripherals on the MSS canvas:
 - MMUART_0 and MMUART_1
 - SPI_0 and SPI_1
 - I2C_0 and I2C_1
 - PDMA
 - WATCHDOG
 - FIC_0 and FIC_1
 - USB
 - Ethernet

After disabling the above components, the MSS configuration window will look similar to Figure 9.

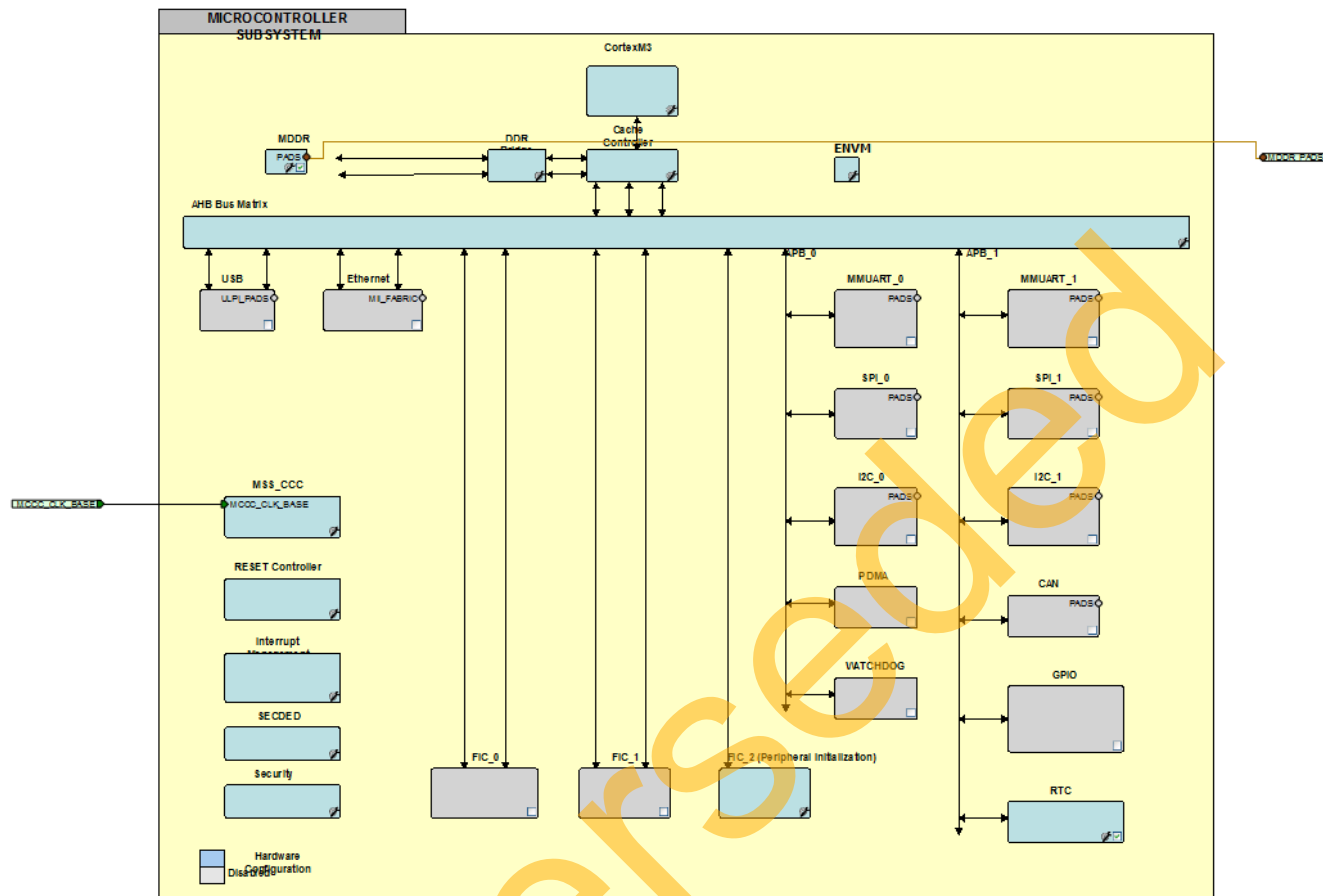


Figure 9. Enabled and Disabled MSS Components

3. Double-click the **MDDR** block and configure as shown in Figure 10.
 - Select **Memory Interface Configuration Mode** as **Soft Memory Controller**.
 - Select **Fabric Interface Settings** as **Use an AXI Interface**.

This selection configures the SMC_FIC interface inside the MDDR as a 64-bit AXI interface for the FPGA fabric from the DDR Bridge.

- Click **OK** on the **Mode Selection** to complete the configuration.

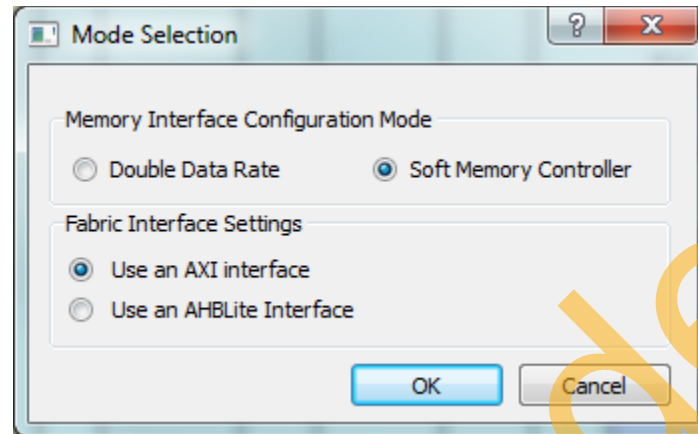


Figure 10. Mode Selection

4. Double-click the **MSS_CCC** block and configure as shown in Figure 11.
 - The clock input is by default selected as **CLK_BASE** with the input frequency of **100 MHz**.
 - Select the check box for **Monitor FPGA Fabric PLL Lock (CLK_BASE_PLL_LOCK)**.
 - Leave the default frequency of **100 MHz** for **M3_CLK**.
 - Click **DDR_SMC_FIC_CLK** to see the clock direction in the GUI. By default, **DDR_SMC_FIC_CLK** is set to the same frequency as that of **M3_CLK** (**M3_CLK** divided by 1; i.e. **100 MHz**)
 - Leave the rest as default.
 - Click **OK** on the **MSS Clock Configurator** to complete the clock configuration.

The above selection configures the MSS CCC to receive the input clock from the fabric CCC. The lock input of the MSS CCC is configured to be received from the fabric CCC block.

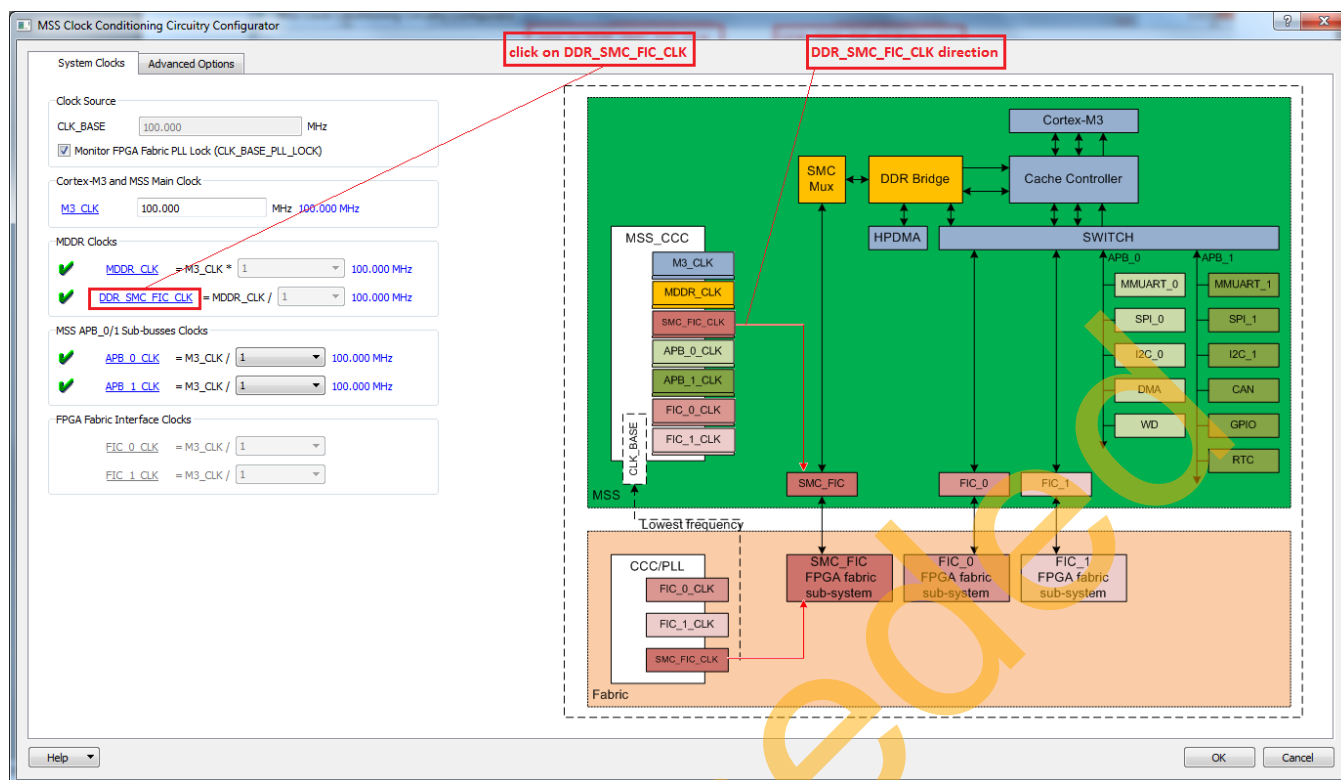


Figure 11. MSS Clock Configurator

- Double-click the **Reset Controller** and select the **Enable MSS to Fabric Reset** and **Enable Fabric to MSS Reset**, as shown in Figure 12. This enables the MSS to generate the Reset signal for all the Fabric blocks. The MSS reset itself will be coming through a system reset pin on the Fabric I/O. Click **OK**.

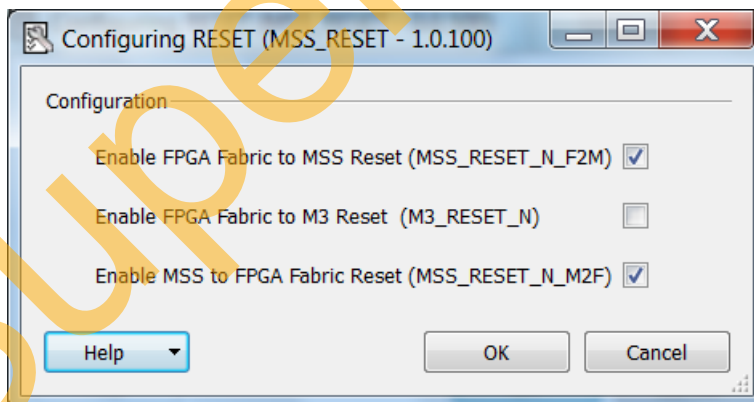


Figure 12. MSS RESET Configurator

- This completes the configuration of the MSS. Select **File > Save** to save **Access_EXT_SDRAM_MSS**.

Step 4: Updating the MSS Component Instance

1. Select the **Access_EXT_SDRAM** tab on the SmartDesign canvas, right-click **Access_EXT_SDRAM_MSS_0** and select **Update Instance(s) with Latest Component**, as shown in Figure 13. After successful updating, the **Access_EXT_SDRAM_MSS_0** instance will look, as shown in Figure 14.

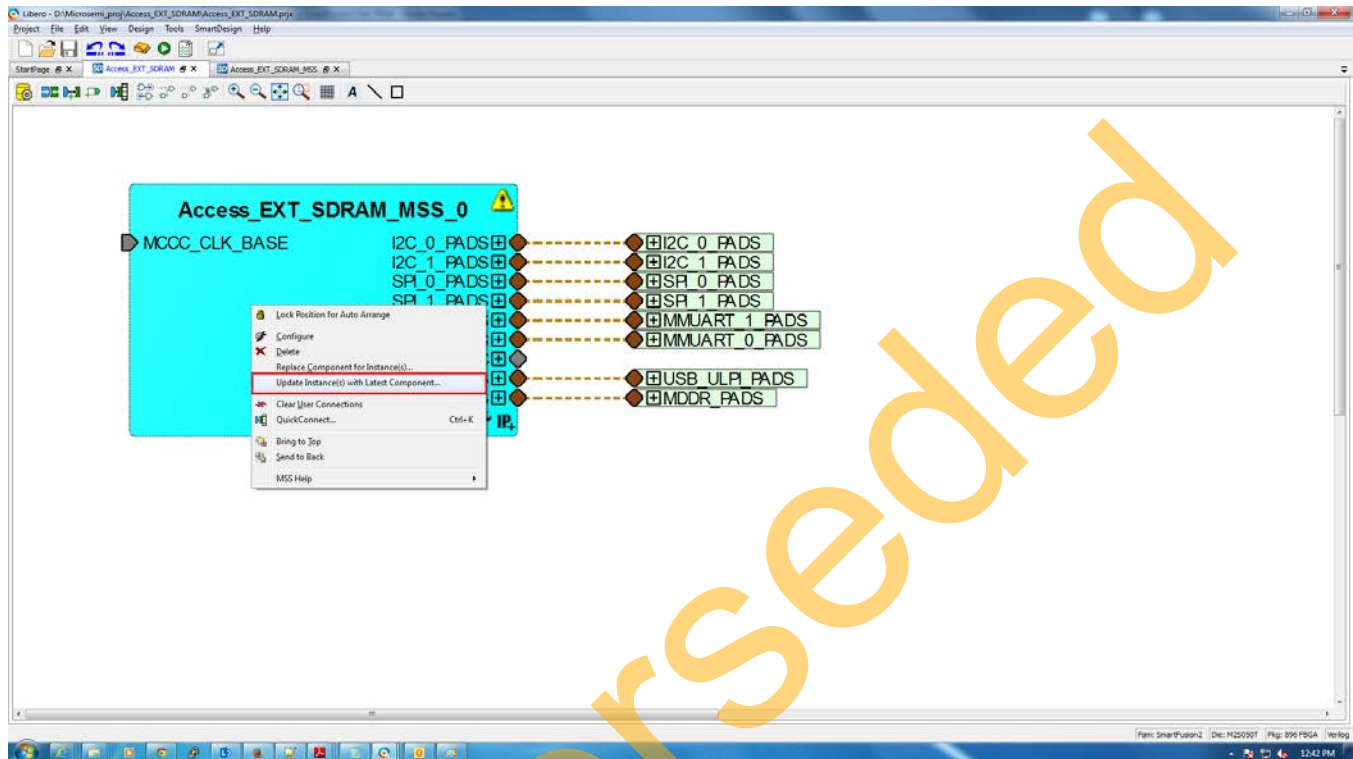


Figure 13. Updating the MSS

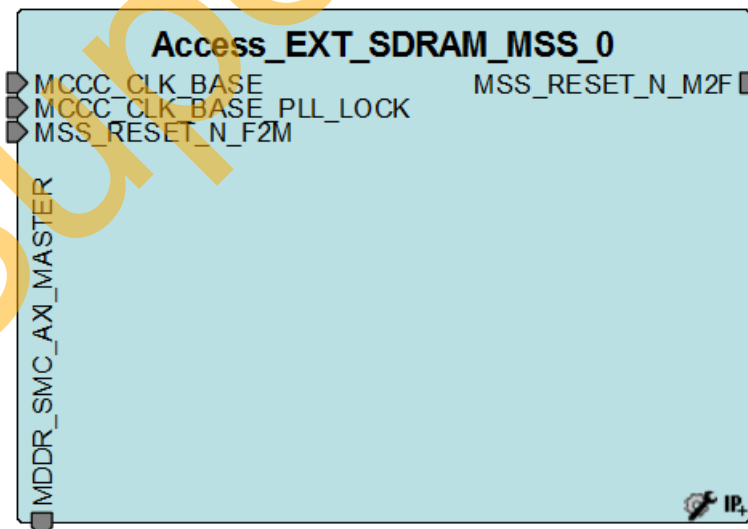


Figure 14. Updated MSS Instance

Step 5: Configuring the Fabric Components

1. Select the **CoreAXI** IP from the Bus Interface sub-section of the IP Catalog, as shown in Figure 15, and drag it onto the **Access_EXT_SDRAM SmartDesign** tab.

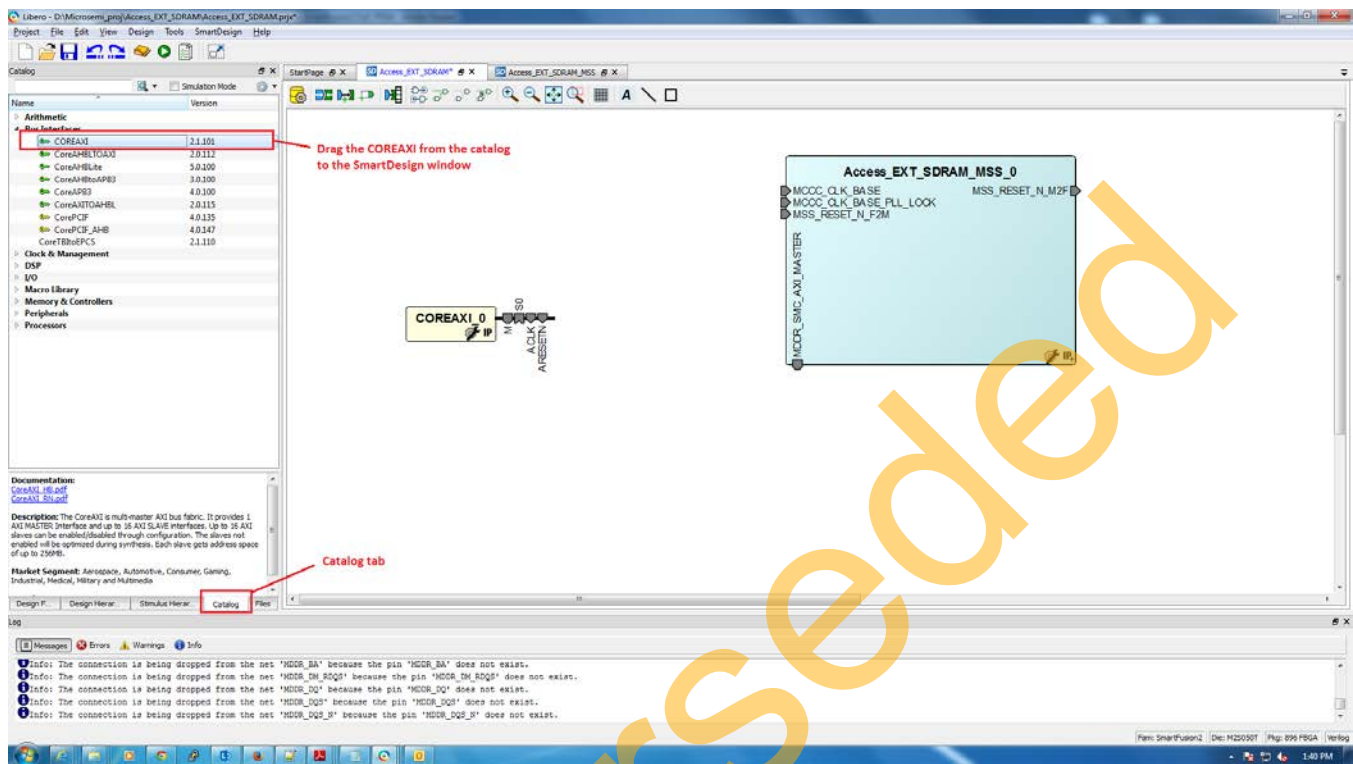


Figure 15. CoreAXI IP from the Catalog

2. Double-click the **COREAXI_0** instance on the SmartDesign pane to open its configuration window. Configure the core, as shown in Figure 16.
 - Leave the **Memory Space** field as **16, 256 MB slots beginning at address 0x00000000** (which is default), as shown in Figure 16.
 - Leave the **AXI Data Width** field as **64** (which is default), as shown in Figure 16.
 - Clear the option of **SLAVE0 for Enable Master Access**
 - Select the option of **SLAVE10 for Enable Master Access**
 - Leave the rest as default.
 - Click **OK** on the Configuration window to complete the configuration.

With the above settings, you have configured the **COREAXI_0** instance as a 64-bit AXI interface with Slave 10 slot enabled for Master0.

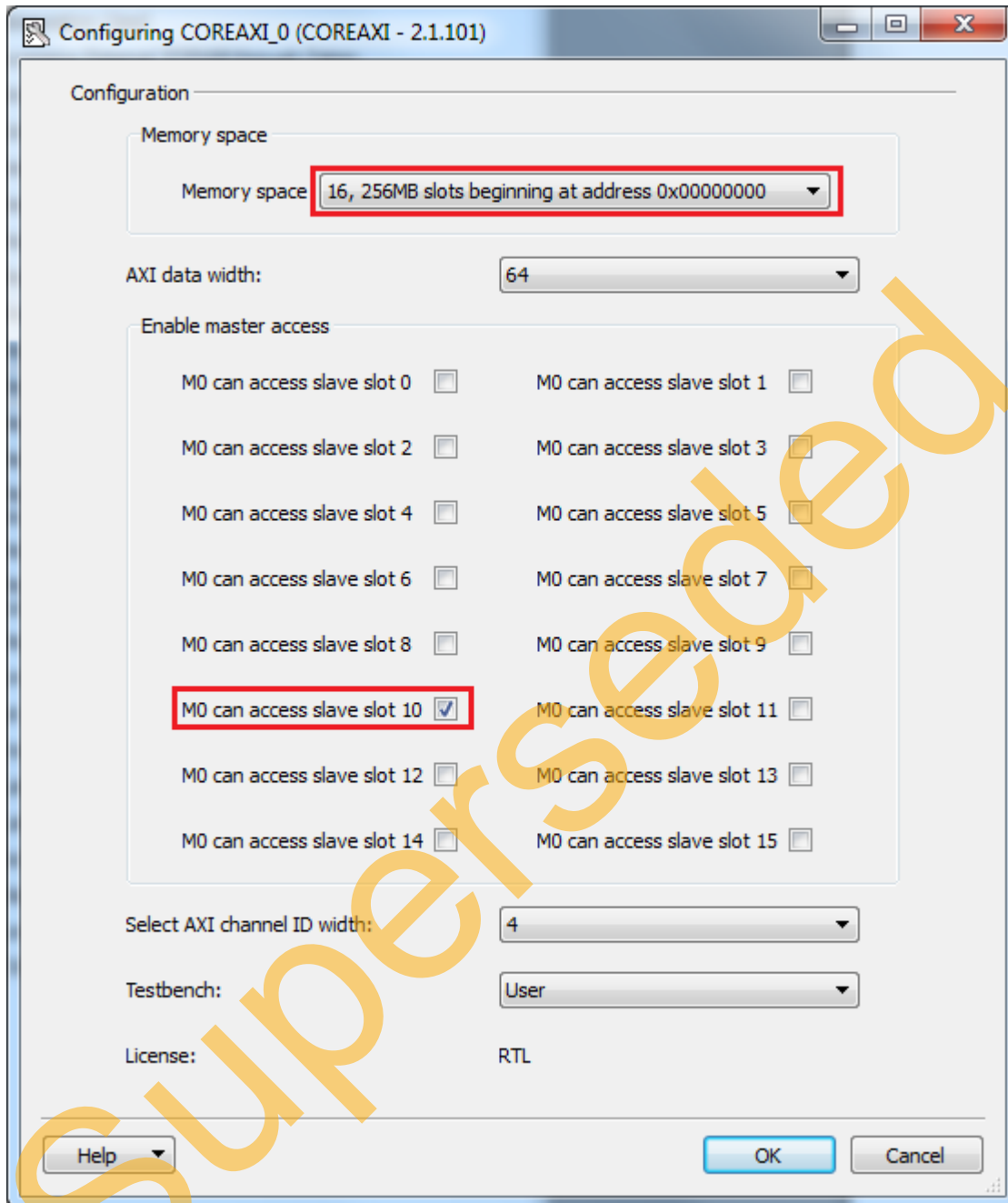
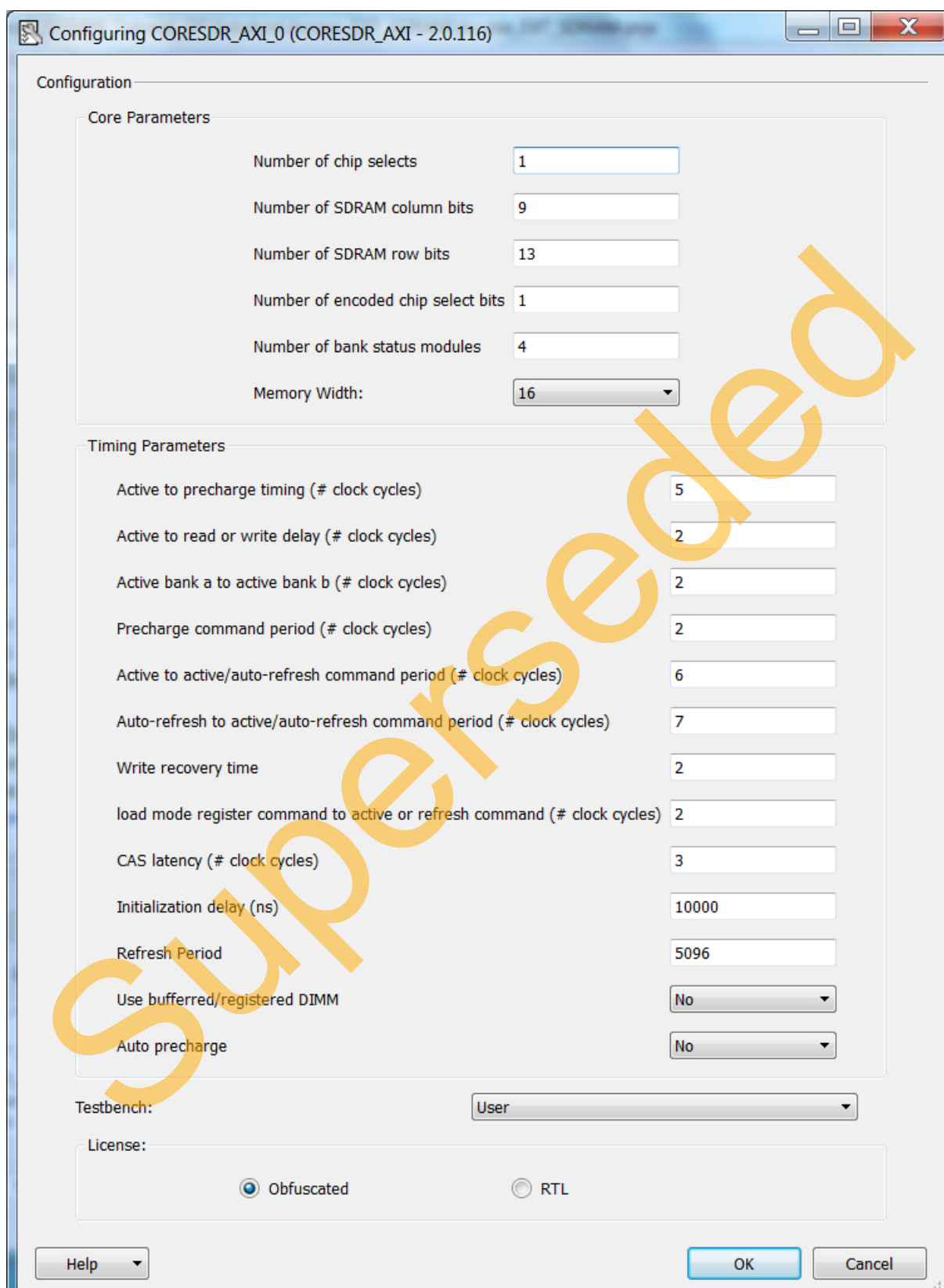


Figure 16. CoreAXI Configurator

3. Drag the **CoreSDR_AXI** IP from the **Peripherals** sub-section of the IP **Catalog**. Double-click on the **CORESDR_AXI_0** instance to access its configuration window. Fill in the details in the configuration window, as shown in Figure 17. These details are filled as per the datasheet of the Micron 256Mb SDRAM, which is simulation model you will use for the functional simulation. The part number of the SDRAM used is MT48LC16M16A2, which is a 4 Meg x 16 x 4 banks SDRAM.

Note: If you are using some other SDRAM simulation model, please configure the **CORESDR_AXI** according to that specific SDRAM memory datasheet.



Configuring CORESDR_AXI_0 (CORESDR_AXI - 2.0.116)

Configuration

Core Parameters

Number of chip selects	<input type="text" value="1"/>
Number of SDRAM column bits	<input type="text" value="9"/>
Number of SDRAM row bits	<input type="text" value="13"/>
Number of encoded chip select bits	<input type="text" value="1"/>
Number of bank status modules	<input type="text" value="4"/>
Memory Width:	<input type="text" value="16"/>

Timing Parameters

Active to precharge timing (# clock cycles)	<input type="text" value="5"/>
Active to read or write delay (# clock cycles)	<input type="text" value="2"/>
Active bank a to active bank b (# clock cycles)	<input type="text" value="2"/>
Precharge command period (# clock cycles)	<input type="text" value="2"/>
Active to active/auto-refresh command period (# clock cycles)	<input type="text" value="6"/>
Auto-refresh to active/auto-refresh command period (# clock cycles)	<input type="text" value="7"/>
Write recovery time	<input type="text" value="2"/>
load mode register command to active or refresh command (# clock cycles)	<input type="text" value="2"/>
CAS latency (# clock cycles)	<input type="text" value="3"/>
Initialization delay (ns)	<input type="text" value="10000"/>
Refresh Period	<input type="text" value="5096"/>
Use buffered/registered DIMM	<input type="text" value="No"/>
Auto precharge	<input type="text" value="No"/>

Testbench:

License:

☒ Obfuscated ☐ RTL

Help

Figure 17. CoreSDR_AXI Configuration Window

4. Drag the clock conditioning circuitry (CCC) block from the Clock & Management sub-section of the IP Catalog. Double-click the **FCCC_0** instance to open up its configuration window. Configure the following items on the Configuration Window, as shown in Figure 18.
 - Select the **Advanced** tab, as shown in Figure 19.
 - In the **Advanced** tab, select the clock source as **Oscillators -> 25/50 MHz Oscillator**, as shown in Figure 19.
 - Leave the output frequency as **100 MHz**.
 - Leave the rest as default.
 - On the **PLL Options** tab, select the **Expose PLL_ARST_N** and **PLL_POWERDOWN_N** check box, as shown in Figure 20.
 - Click **OK** to complete the configuration.

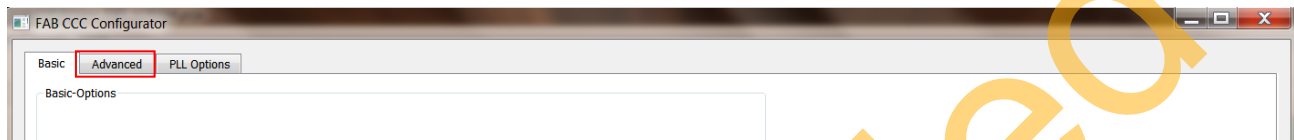


Figure 18. Advanced Tab of the FAB CCC Configurator

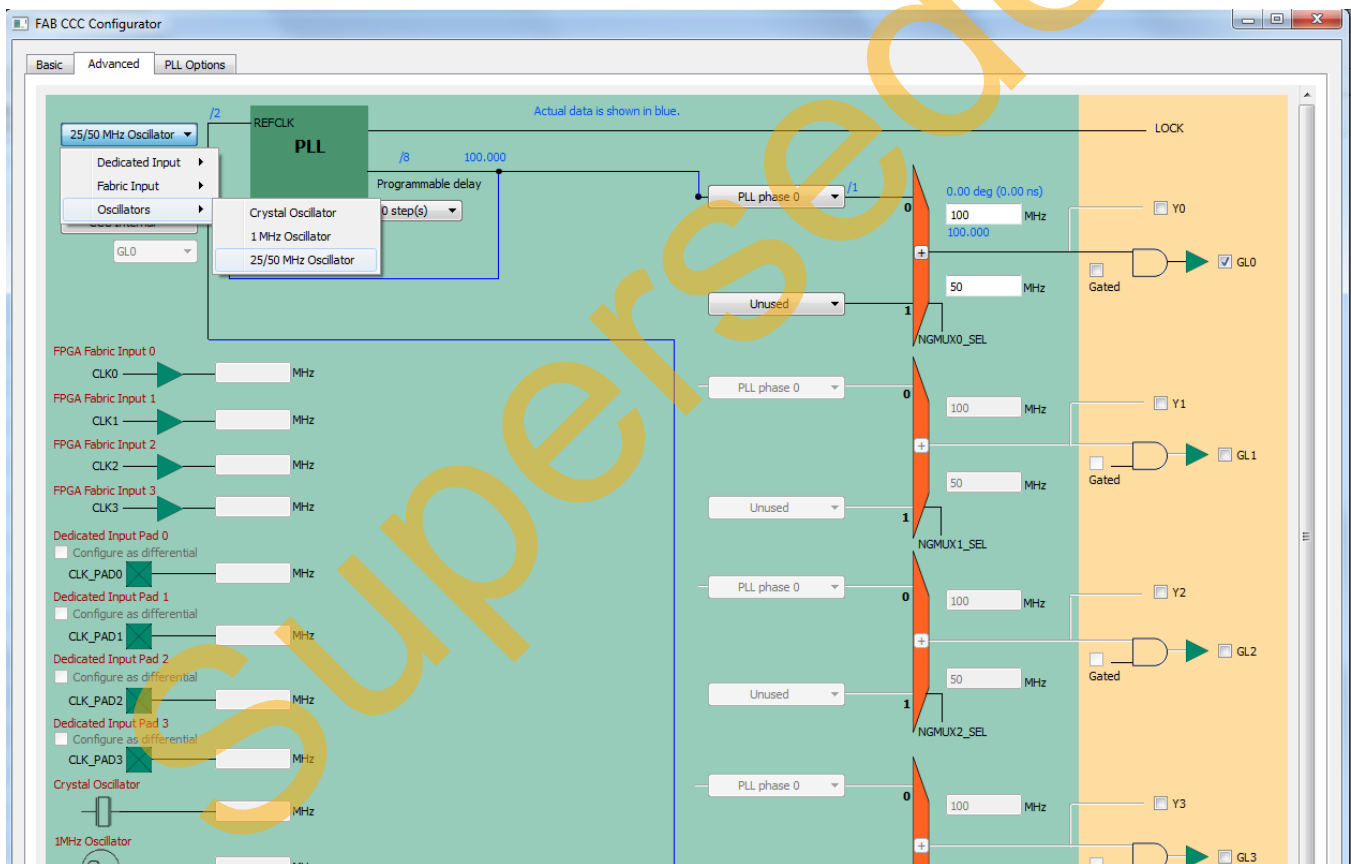


Figure 19. Selecting the Clock Source

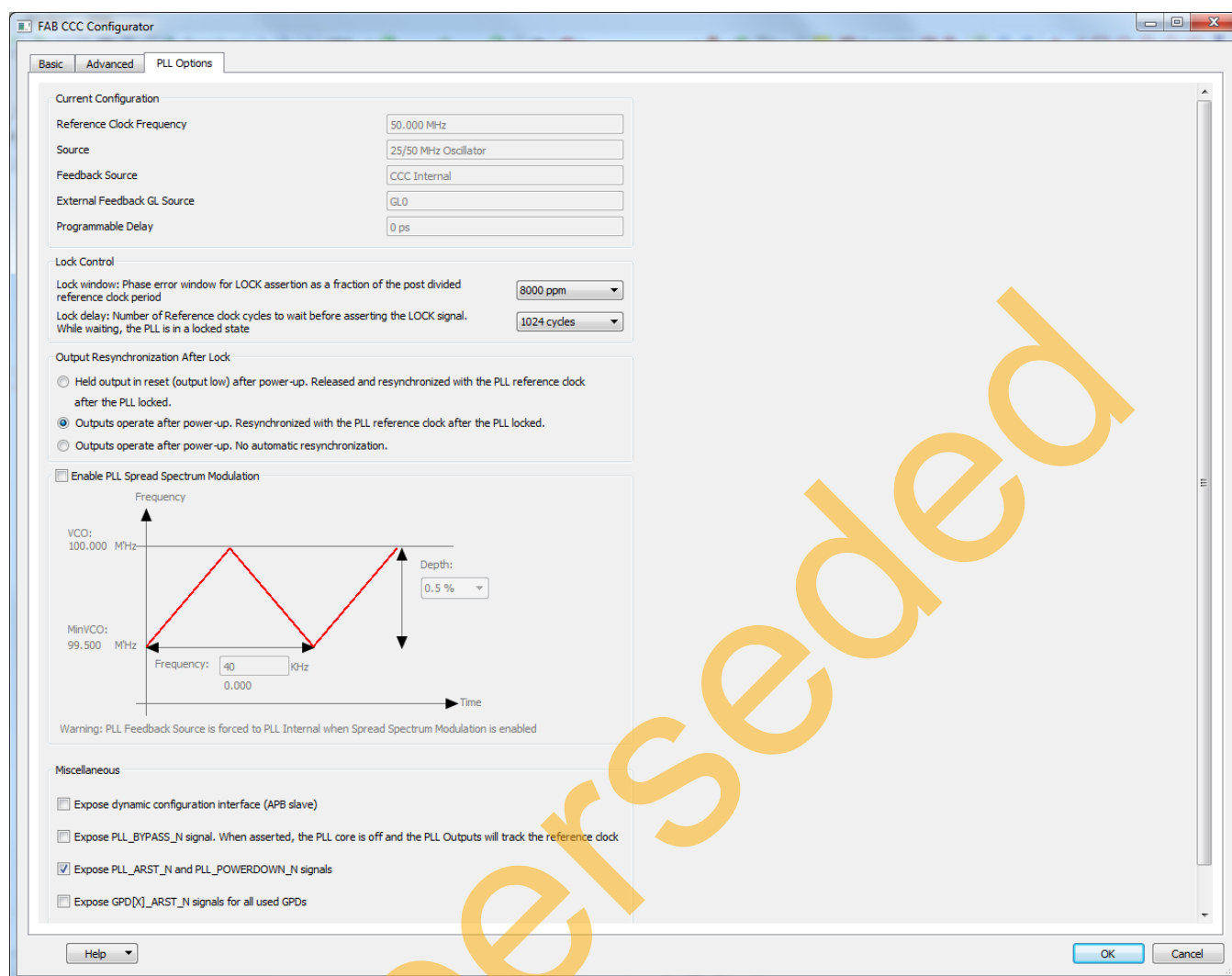


Figure 20. Exposing the PLL Reset and Power-down Signals

5. Drag the **Chip Oscillators** IP from the Clock & Management sub-section of the IP Catalog into the SmartDesign. Double-click the **OSC_0** instance to open up its configuration window. Make the following selections, as shown in Figure 21.
 - Select the check box for **On Chip 25/50 MHz RC Oscillator**
 - Clear the **Drives MSS** check box
 - Select the check box for **Drives Fabric CCC(s)**
 - Leave the rest as default.
 - Click **OK** to complete the configuration.

With this, you have selected the On-chip 50 MHz RC oscillator to drive the input of the fabric CCC block instantiated earlier.

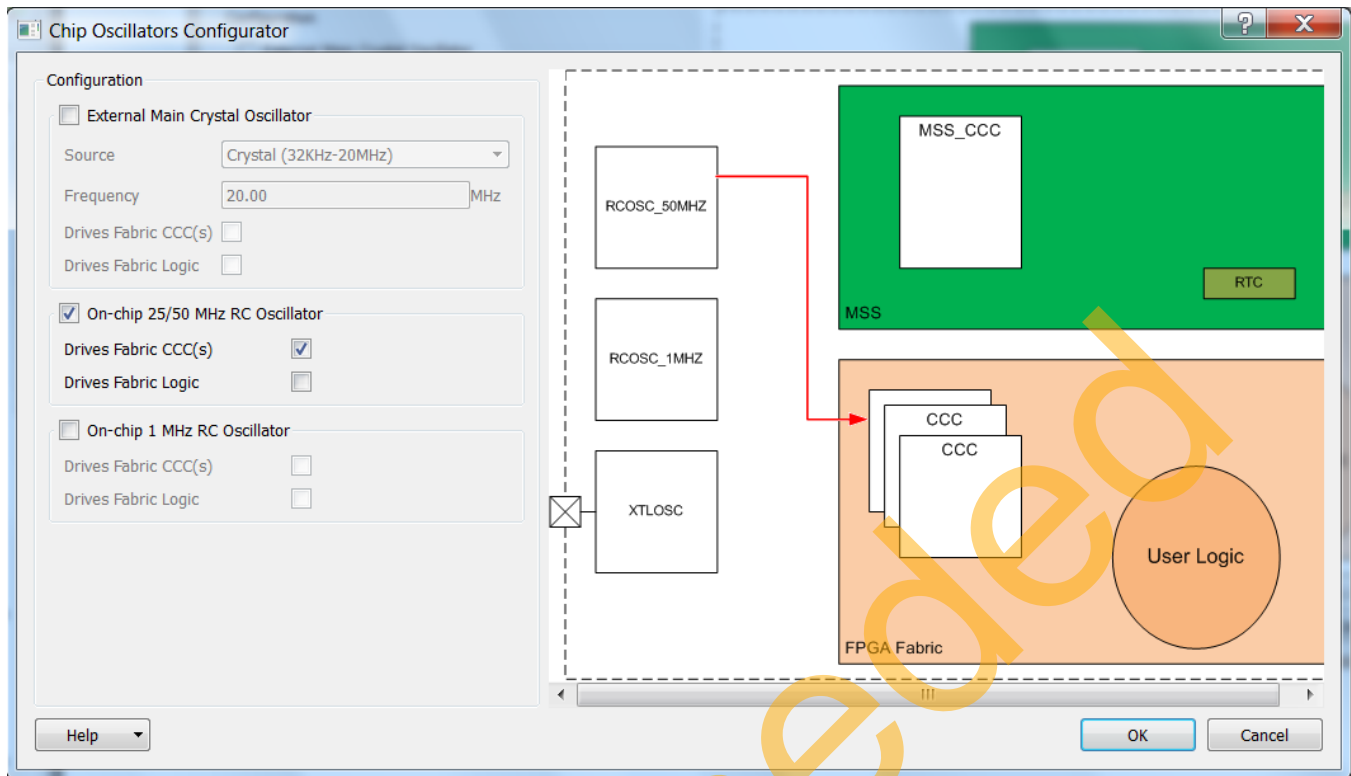


Figure 21. Oscillator Configuration

You have configured all the IPs for the fabric of the SmartFusion2 SoC FPGA device that are required in this design. You can arrange the IP as convenient to you before starting to connect them together.

Step 6: Interconnecting All the Components Together

1. After re-arranging all the components on the SmartDesign window, connect the pins of all the blocks as described below.

You can use the **Auto Arrange Instances** on the SmartDesign canvas to arrange the various instances, automatically. There are two ways to make the connections. The first method is by using the **Connection Mode** option. To use this method, change the SmartDesign to connection mode by clicking the **Connection Mode** button on the SmartDesign window, as shown in Figure 22. Your cursor will change from the normal arrow shape to the connection mode icon shape. To make a connection in this mode, click on the first pin and drag-drop to the second pin that you want to connect.

The second method is by selecting the pins to be connected together and selecting **Connect** from the context menu. To select multiple pins to be connected together, hold the **CTRL** key as you select the pins. Right-click the input source signal and select the option of **Connect** to connect all the signals together. In the same way, select the input source signal, right-click it, and select the option of **Disconnect** to disconnect the signals already connected.

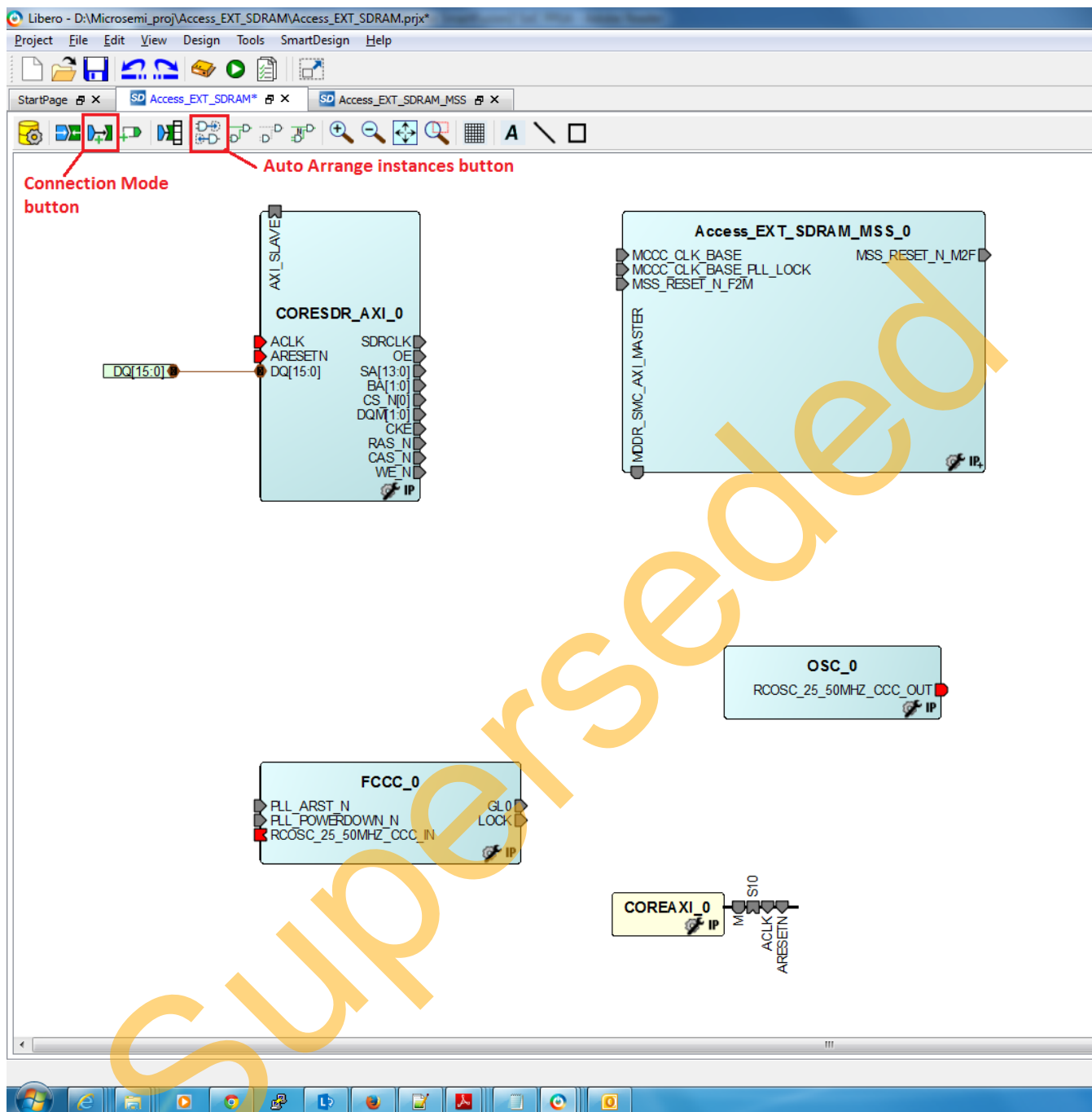


Figure 22. Changing to Connection Mode

Do all the connections as described below:

- Connect **ROSC_25_50MHZ_CCC_OUT(M)** of the **OSC_0** to the **ROSC_25_50MHZ_CCC_IN(S)** of the **FCCC_0**.
- Connect **GL0** of the **FCCC_0** to **MCCC_CLK_BASE** of **Access_EXT_SDRAM_MSS_0**, **ACLK** of **COREAXI_0**, and **ACLK** of **CORESDR_AXI_0**. The fabric CCC clock output clocks all the blocks inside the fabric and is input source clock for the MSS CCC block.
- Connect **LOCK** of **FCCC_0** to **MCCC_CLK_BASE_PLL_LOCK** input of the **Access_EXT_SDRAM_MSS_0**.

- Connect **MSS_RESET_N_M2F** of **Access_EXT_SDRAM_MSS_0** to **ARESETN** of **COREAXI_0** and **ARESETN** of **CORESADR_AXI_0**.
- Connect **M** of **COREAXI_0** to **MDDR_SMC_AXI_MASTER** of the **Access_EXT_SDRAM_MSS_0**.
- Connect **S10** of **COREAXI_0** to **AXI_Slave** of **CORESADR_AXI_0**.
- Tie **PLL_POWERDOWN_N** inputs of **FCCC_0** to logic '1'. Select each input signal, right-click the signal, and select **Tie High**.
- Promote the input signal of **MSS_RESET_N_F2M** of **Access_EXT_SDRAM_MSS_0** to top-level. To do this, select the input signal, right-click it, and select **Promote to Top Level**.
- Select the top-level signal of **MSS_RESET_N_F2M** and the input signal **PLL_ARST_N** of the **FCCC_0** instance and connect them. This connects the resets of the MSS and Fabric CCC to the top-level system reset Input.
- Next promote all the output signals of the **CORESADR_AXI_0** to the top level. Hold the **CTRL** key and select each of them, right-click and select **Promote to Top Level**.

That finishes the connection. Click **Auto arrange instances** to arrange the instances, as shown in [Figure 23](#). Save the design by selecting **File > Save**.

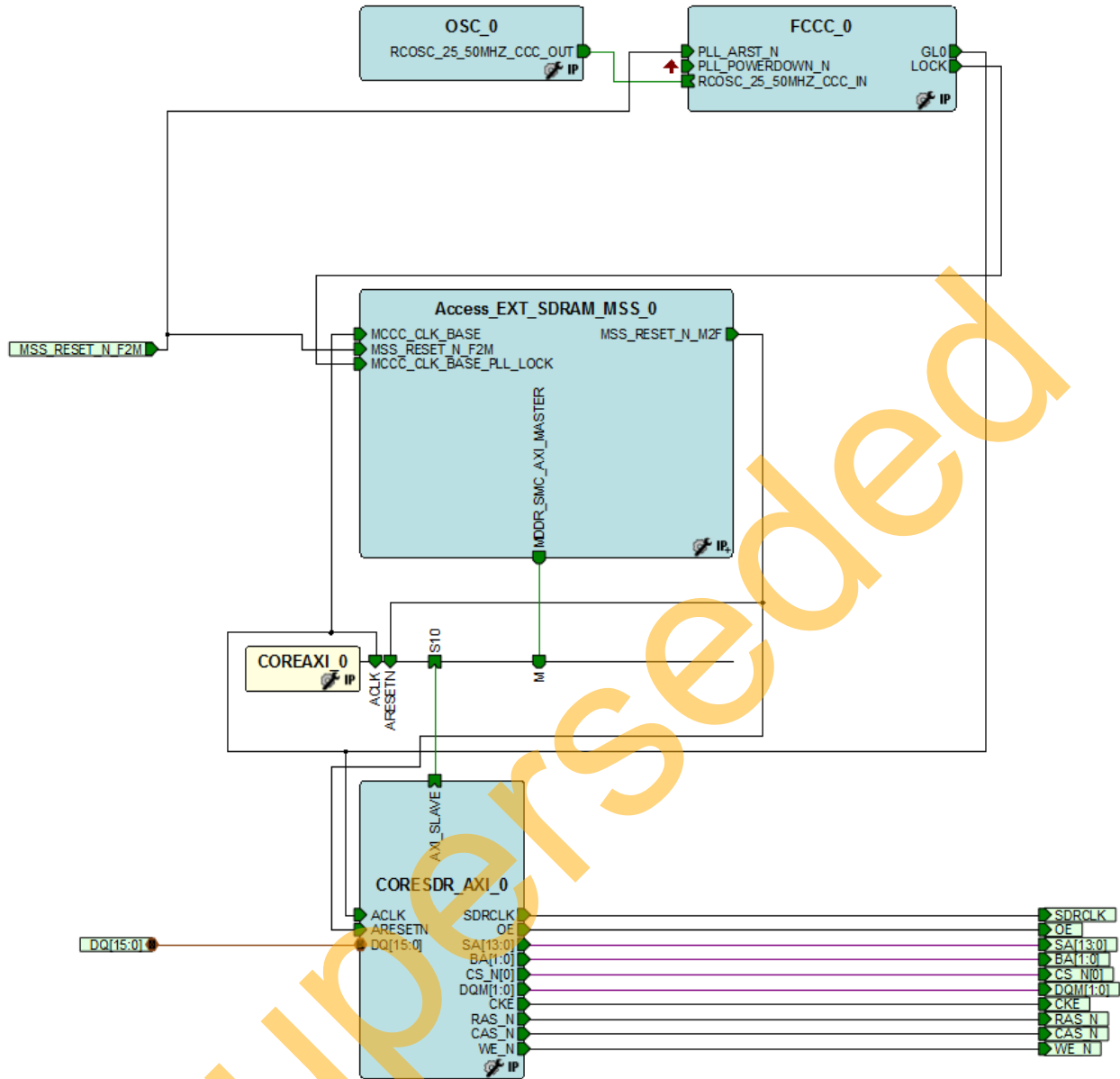


Figure 23. After Making the Top-Level Connection

Step 7: Generating the MSS and the Top-Level Design

1. Select **Access_EXT_SDRAM** tab on the **SmartDesign** canvas and click **Generate Component** on the SmartDesign pane, as shown in Figure 24. Or you can select from **SmartDesign > Generate Component**.

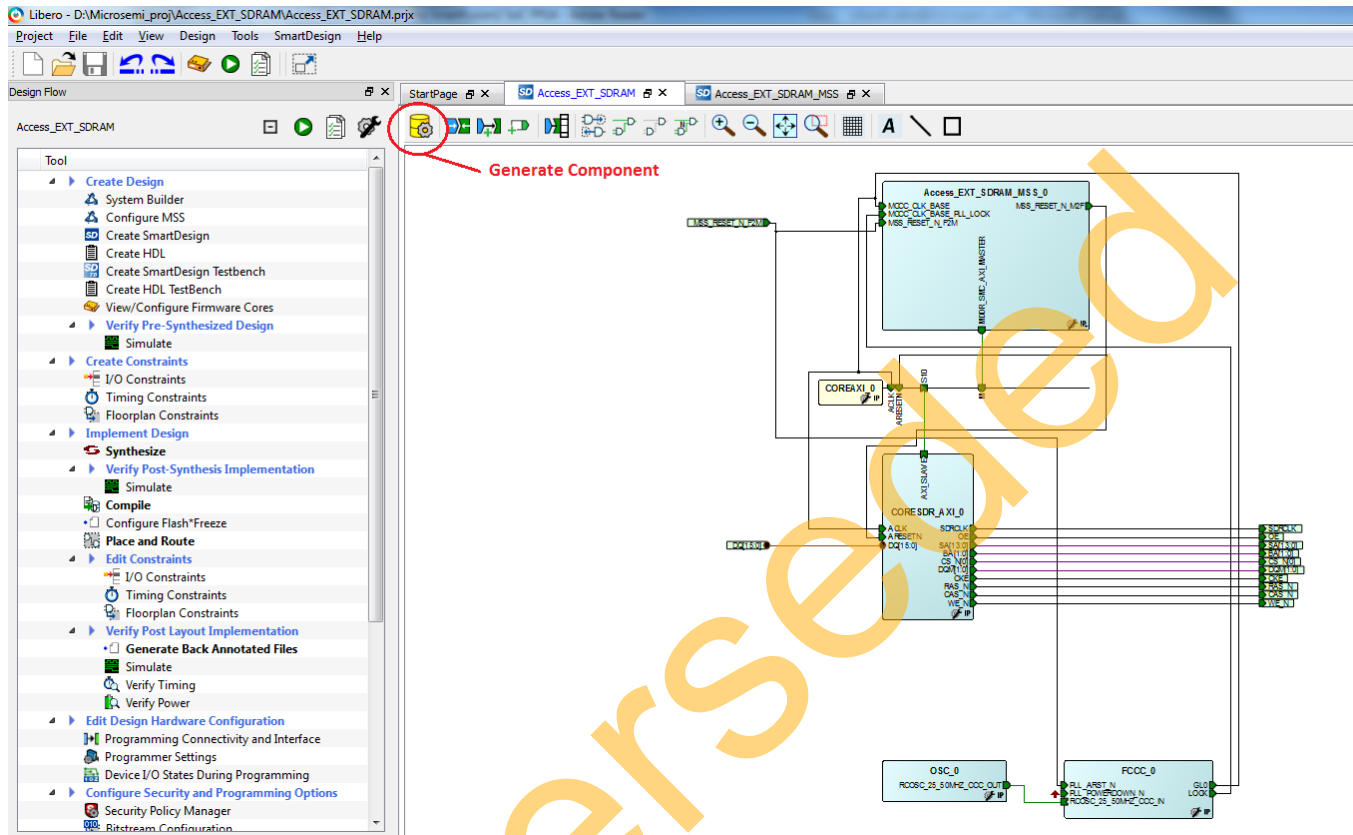


Figure 24. Generating the MSS Component

2. After successful generation of all the components, you will see the following **message** on the log window:
Info: 'Access_EXT_SDRAM' was successfully generated. **Open datasheet for details**
3. After generation, you can see the design hierarchy in the **Design Hierarchy** pane of the Libero SoC, as shown in Figure 25.

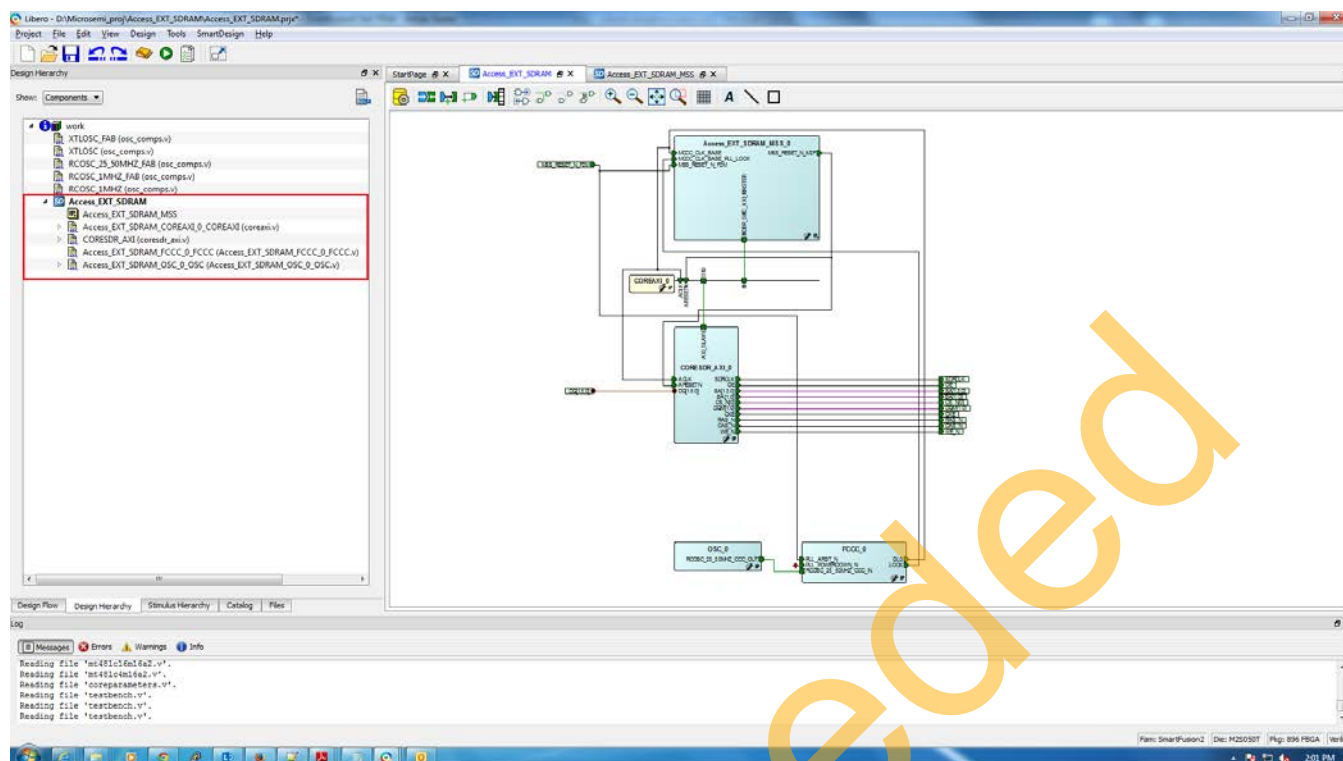


Figure 25. Design Hierarchy

4. After generation, you can see the Memory Map for the CORESDR_AXI_0 component. Right-click the **Access_EXT_SDRAM** SmartDesign window and select **Modify Memory Map**. Figure 26 shows the resultant memory map. The starting address of the MDDR Space 0 is 0xa0000000 in the Cortex-M3 processor's address space.

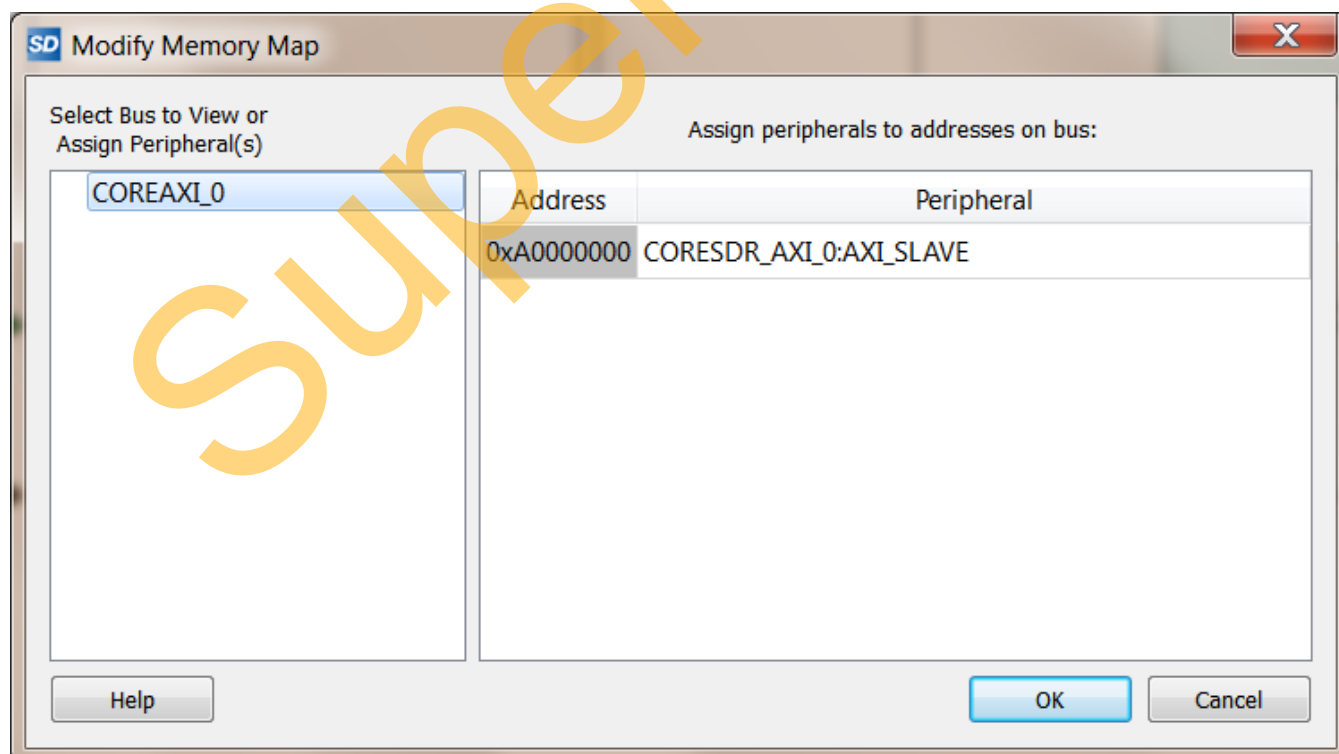


Figure 26. Memory Address of the CORESDR_AXI_0

Step 8: Modifying the Testbench to Add the SDR SDRAM Simulation Model

- While generating the top-level of the design, SmartDesign generates a default testbench template for the design. The Verilog file for the testbench can be found in the following location:

<Project_directory>\Access_EXT_SDRAM\component\work\Access_EXT_SDRAM\

You can also locate it by browsing through the Files tab of the Libero SoC. In this default testbench, the top-level is already instantiated, as shown in Figure 27.

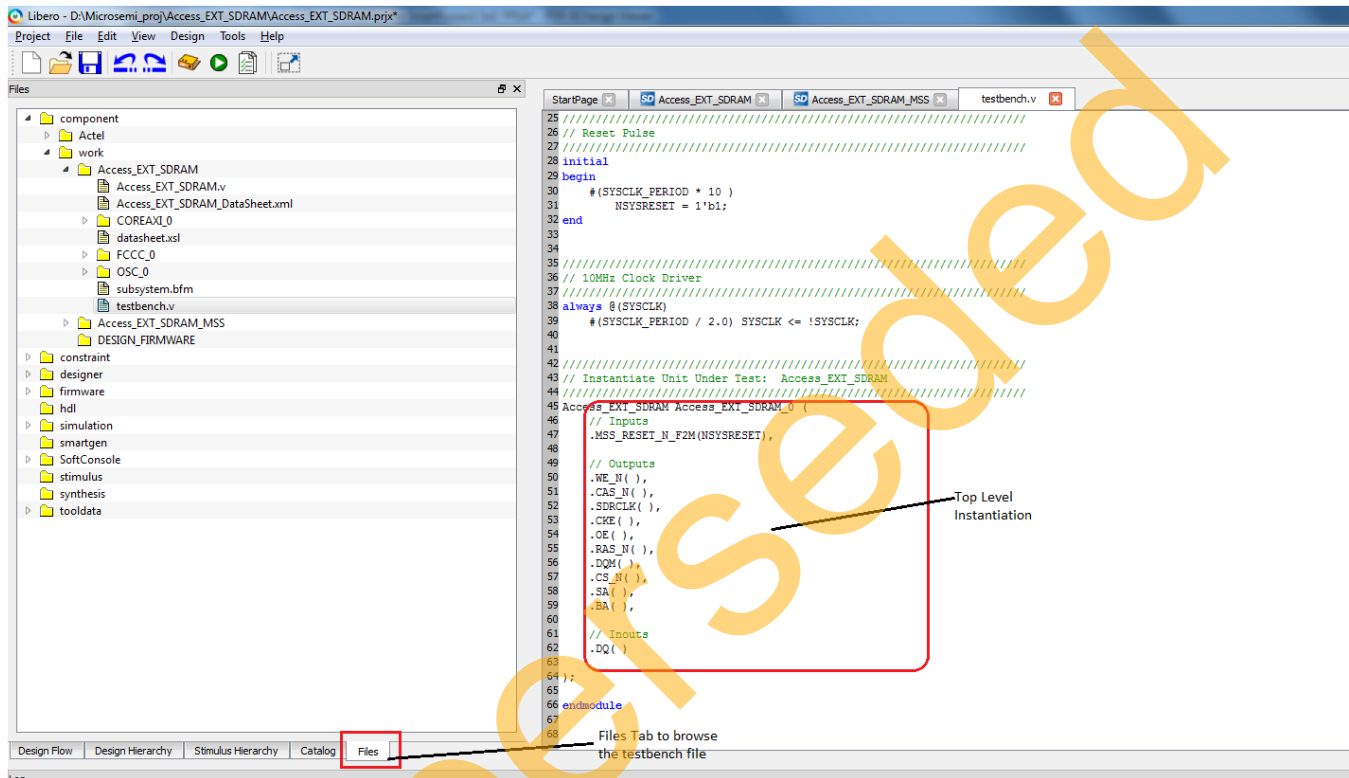


Figure 27. Default Testbench

- In this default testbench, the external SDR SDRAM's simulation model needs to be added and port mapped with the top-level design SDRAM interface signals. Double-click **testbench.v** in the Files tab to open the file. Add the following lines of Verilog code in this testbench.

At the top of the file, include the SDR SDRAM simulation file:

```
`include "mt48lc16m16a2.v"
```

Now declare the following signals in the testbench module.

```
// CORESDR_AXI signals
wire CAS_N_mem;
wire OE_mem;
wire WE_N_mem;
wire CS_N_mem;
wire [1:0] BA_mem;
wire SDRCLK_mem;
wire CKE_mem;
wire RAS_N_mem;
wire [13:0] SA_mem;
wire [15:0] DQ_mem;
wire [1:0] DQM_mem;
```

```
// SDR SDRAM interface signals with the CORESDR_AXI
wire CAS_N_mem_out;
wire WE_N_mem_out;
wire CS_N_mem_out;
wire [1:0] BA_mem_out;
wire CKE_mem_out;
wire RAS_N_mem_out;
wire [13:0] SA_mem_out;
wire [15:0] DQ_mem_out;
wire [1:0] DQM_mem_out;
```

Now modify the top-level instantiation of the **Access_EXT_SDRAM** as shown below:

```
////////////////////////////////////
// Instantiate Unit Under Test: Access_EXT_SDRAM
////////////////////////////////////
Access_EXT_SDRAM Access_EXT_SDRAM_0 (
    // Inputs
    .MSS_RESET_N_F2M (NSYSRESET),
    // Outputs
    .CAS_N(CAS_N_mem ),
    .OE(OE_mem ),
    .WE_N(WE_N_mem ),
    .CS_N(CS_N_mem ),
    .BA(BA_mem ),
    .SDRCLK(SDRCLK_mem ),
    .CKE(CKE_mem ),
    .RAS_N(RAS_N_mem ),
    .SA(SA_mem),
    .DQM(DQM_mem ),
    // Inouts
    .DQ(DQ_mem)
);
```

SDRAM uses source-synchronous clock. So, you need to make sure the SDRAM signals are coming after the rising edge of the clock. So 1 ns delay is added to the SDR SDRAM interface signals with the CORESDR_AXI, as shown below:

```
assign #1 CKE_mem_out = CKE_mem;
assign #1 RAS_N_mem_out = RAS_N_mem;
assign #1 CAS_N_mem_out = CAS_N_mem;
assign #1 WE_N_mem_out = WE_N_mem;
assign #1 SA_mem_out = SA_mem;
assign #1 CS_N_mem_out = CS_N_mem;
assign #1 BA_mem_out = BA_mem;
assign #1 DQM_mem_out = DQM_mem;
assign #1 DQ_mem_out = OE_mem ? DQ_mem: {16{1'bz}};
assign DQ_mem = OE_mem ? {16{1'bz}}: DQ_mem_out;
```

Now Micron's "MT48LC16M16A2" SDR SDRAM is instantiated in the testbench as shown below.

```

////////////////////////////////////
// Instantiate SDR SDRAM
////////////////////////////////////
mt48lc16m16a2 mt48lc16m16a2_0 (
  // Inputs
    .Addr(SA_mem_out[12:0]),
    .Ba(BA_mem_out ),
    .Clk(SDRCLK_mem ),
    .Cke(CKE_mem_out ),
    .Cs_n(CS_N_mem_out),
    .Ras_n(RAS_N_mem_out ),
    .Cas_n(CAS_N_mem_out ),
    .We_n(WE_N_mem_out ),
    .Dqm(DQM_mem_out ),

    // Inouts
    .Dq(DQ_mem_out )
);

```

Save the file by selecting **File > Save testbench.v as**, select the Stimulus folder under the Access_EXT_SDRAM project (<Project_directory>\Access_EXT_SDRAM\Stimulus). Save the file as **testbench.v**.

The testbench file is saved under the stimulus file so it is not overwritten when the SmartDesign Access_EXT_SDRAM is regenerated. After saving the modified testbench file, it can be checked for the syntax errors. On the testbench.v source window, right-click and select **Check HDL file**. It will check the testbench.v for any syntax errors.

Note: The modified testbench.v file is provided in the following location in the attached compressed project:

<Project_directory>\ACCESS_EXT_SDRAM\Source

If you want to use the provided modified *testbench.v*, import it as a stimulus file by selecting **File > Import Files**. In **Import Files** dialog box, select the file type as **HDL Stimulus Files (*.vhd, *.v)**. Browse to the above mentioned location of *testbench.v* and import it as shown in [Figure 28](#). The testbench.v file now shows under the Stimulus folder in the Files tab.

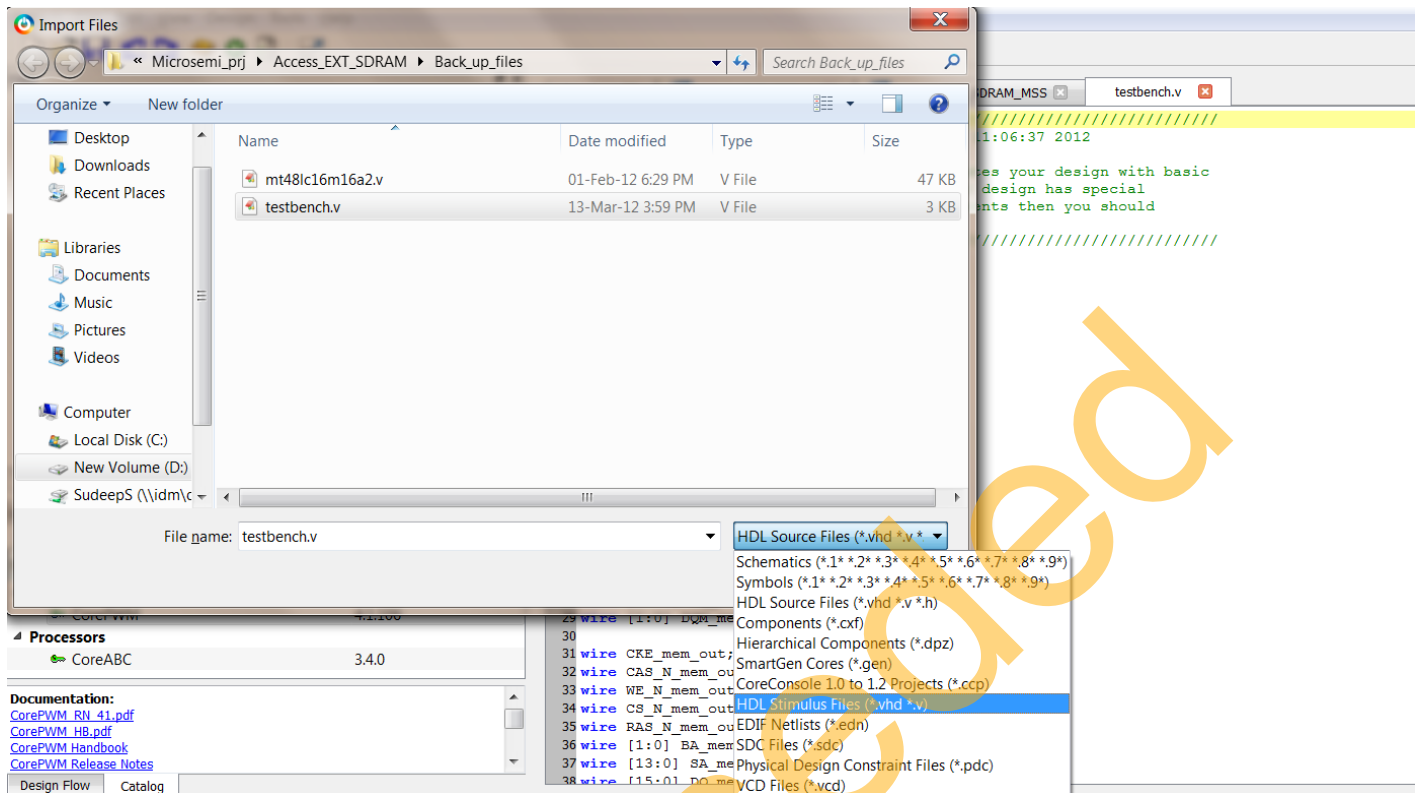


Figure 28. File Import to Stimulus Folder

- Import the **mt48lc16m16a2.v** file from the location in the attached compressed project <Project_directory>\ ACCESS_EXT_SDRAM\Source to your project's **Stimulus** folder location as follow:

Select **File > Import File**. In the **Import Files** dialog box, select the file type as **HDL Stimulus Files (*.vhd, *.v)**. Browse to the above mentioned location of the **mt48lc16m16a2.v** file and import it. The **mt48lc16m16a2.v** file now shows under the **Stimulus** folder in the **Files** tab.

Step 9: Adding BFM Commands to Perform the Simulation

- The user BFM commands are added in to a file named *user.bfm*, which can be found in the following location in your project:

<Project_directory>\Access_EXT_SDRAM\simulation

Browse the user.bfm under simulation file in the Files tab in Libero SoC and double-click it to open the file. Add the following commands to it.

Before the "procedure user_main", add the following command:

```
memmap CORESDR_AXI_0 0xA0000000;
```

Comment out the following line in the user.bfm file by putting hash(#) before it:

```
"include "subsystem.bfm"
```

Under the "procedure user_main" section, add the BFM commands which are circled below:

```
int i
# perform subsystem initialization routine
#call subsystem_init;
print "M_DDR0_CTRL_REGS TEST START";
loop i 0 110 1
    wait 100ns
endloop
# add your BFM commands below:
write w CORESDR_AXI_0 0x0000 0xA1B2C3D4 ;
write w CORESDR_AXI_0 0x0004 0x10100101 ;
write w CORESDR_AXI_0 0x0008 0xA5DEF6E7 ;
write w CORESDR_AXI_0 0x000C 0xD7D7E1E1 ;

readcheck w CORESDR_AXI_0 0x0000 0xA1B2C3D4 ;
readcheck w CORESDR_AXI_0 0x0004 0x10100101 ;
readcheck w CORESDR_AXI_0 0x0008 0xA5DEF6E7 ;
readcheck w CORESDR_AXI_0 0x000C 0xD7D7E1E1 ;
print "M_DDR0_CTRL_REGS TEST ENDS";
print ""
```

Comment out this line in the bfm file

Save the *user.bfm* file after adding the above lines by selecting **File > Save**. Refer to the CoreAMBA BFM User's Guide for more details on the above BFM commands.

www.microsemi.com/soc/ipdocs/CoreAMBA_BFM_UG.pdf

Note: The sample user.bfm file can be found in the following location in the attached compressed project: <Project_directory>\ACCESS_EXT_SDRAM\Source

Step 10: Setting up the Simulation and Invoking the Simulation Tool

1. The simulation tool must be set up before invoking so that it loads with your desired settings. Select **Project > Project Settings**. On the Project Settings pane, under the Simulation Options, select **Do File**. Modify the Simulation Runtime to **158 us**, as shown in [Figure 29](#).

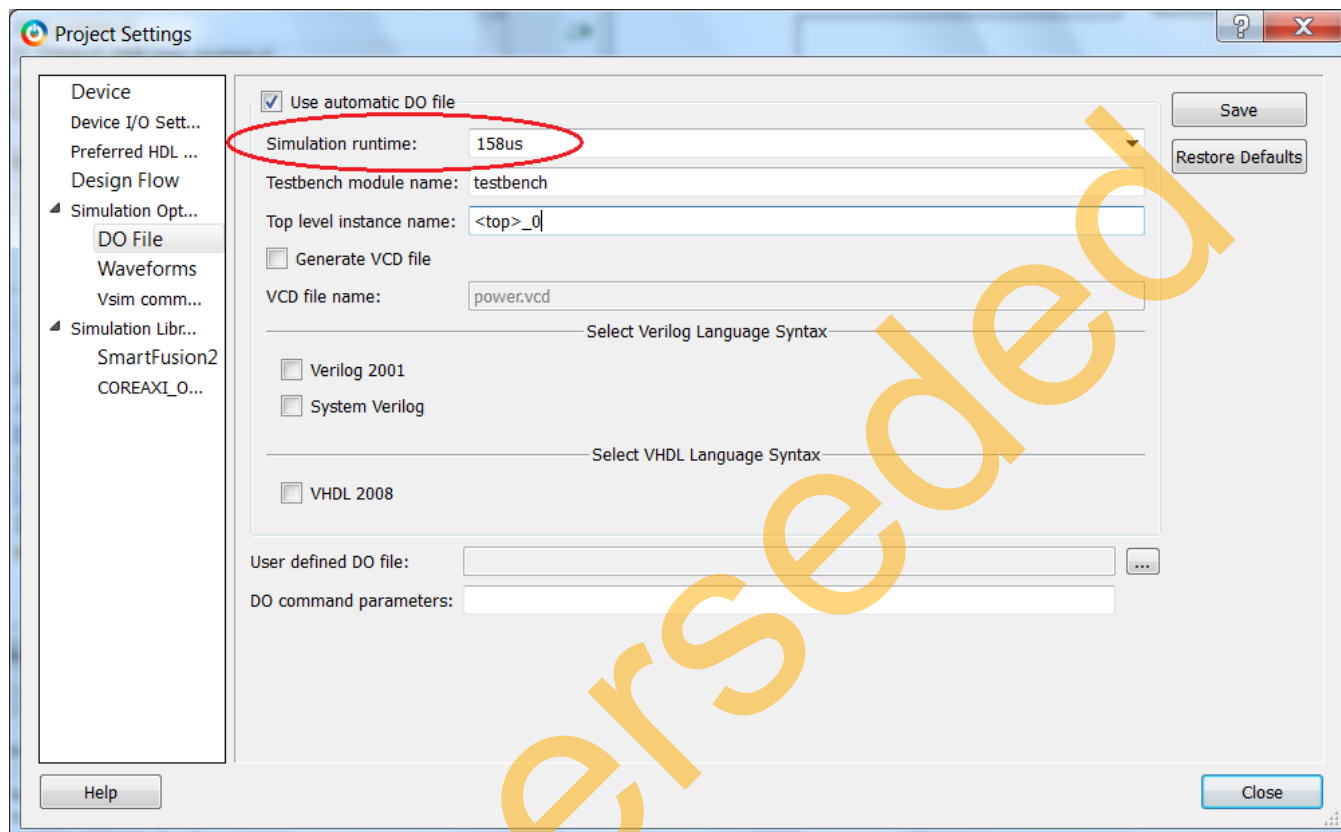


Figure 29. Simulation Runtime

Note for VHDL flow:

- Since the Micron SDRAM memory models are only available in Verilog, if you are using the VHDL flow, you need to use the ModelSim full version, for example ModelSim SE, since ModelSim AE does not support mixed-language flow. If you are using the ModelSim full version, you need to compile with **-novopt** switch.
- A .do file, **run_novopt.do** which has the switch already set, is provided along with the source files in the tutorial zip files. To use the provided run_novopt.do file, clear the **Use automatic DO file** check box and browse to the location of the provide run_novopt.do file, as shown in [Figure 30](#).

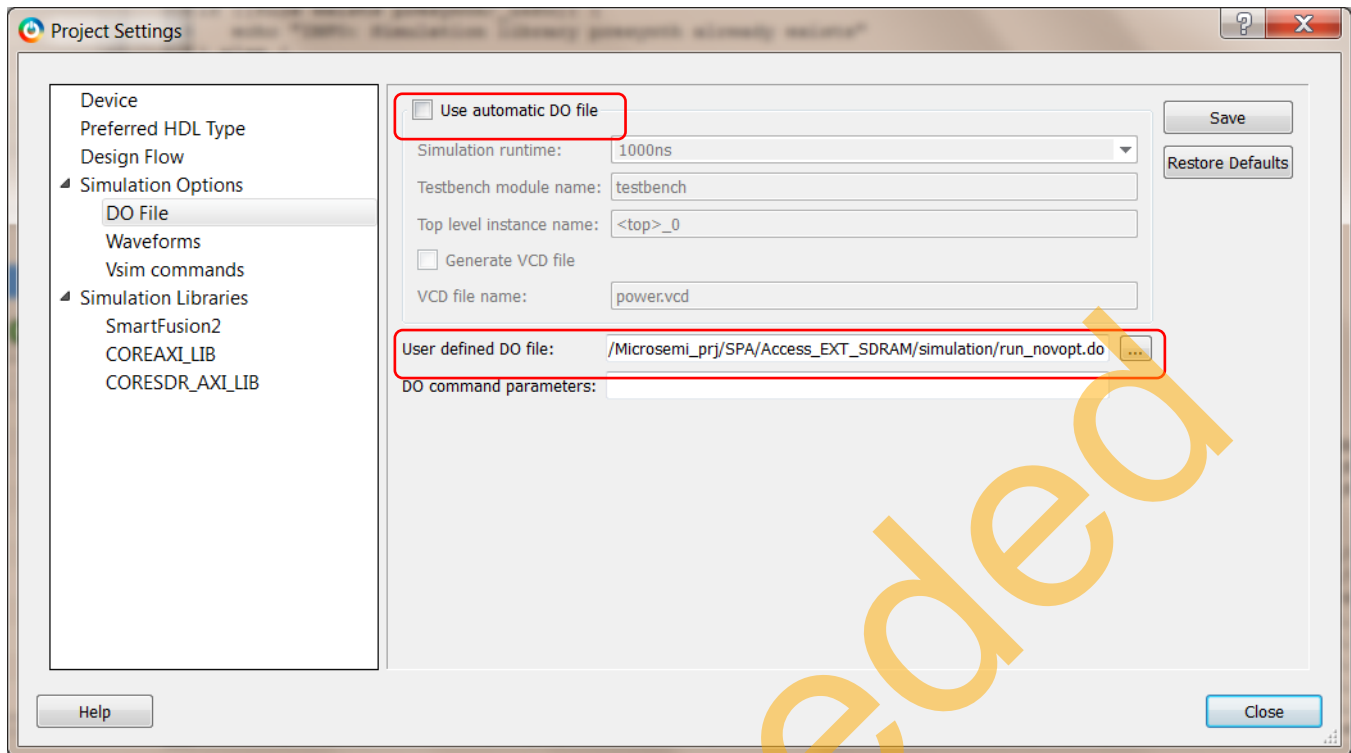


Figure 30. Specifying run_novopt.do for VHDL ModelSim Full Version

2. Select the waveforms under Simulation Options and select the **Include DO File** option. This option allows you to specify a custom macro file which sets up the ModelSim's wave window with the required signals added to the wave window. A custom macro file (**wave.do**) is provided at the following location in the attached compressed project:

<Project_directory>\ ACCESS_EXT_SDRAM\Source

This **DO** file will add all the AXI bus signals and the CORESDR_AXI interface signals with external SDR SDRAM memory.

Browse this **wave.do** file from the above specified location, as shown in Figure 31.

Note: If you want to add your own signals in the ModelSim wave window during simulation, ignore the above step and leave it as default; that is, Do not select the **Include DO File** option.

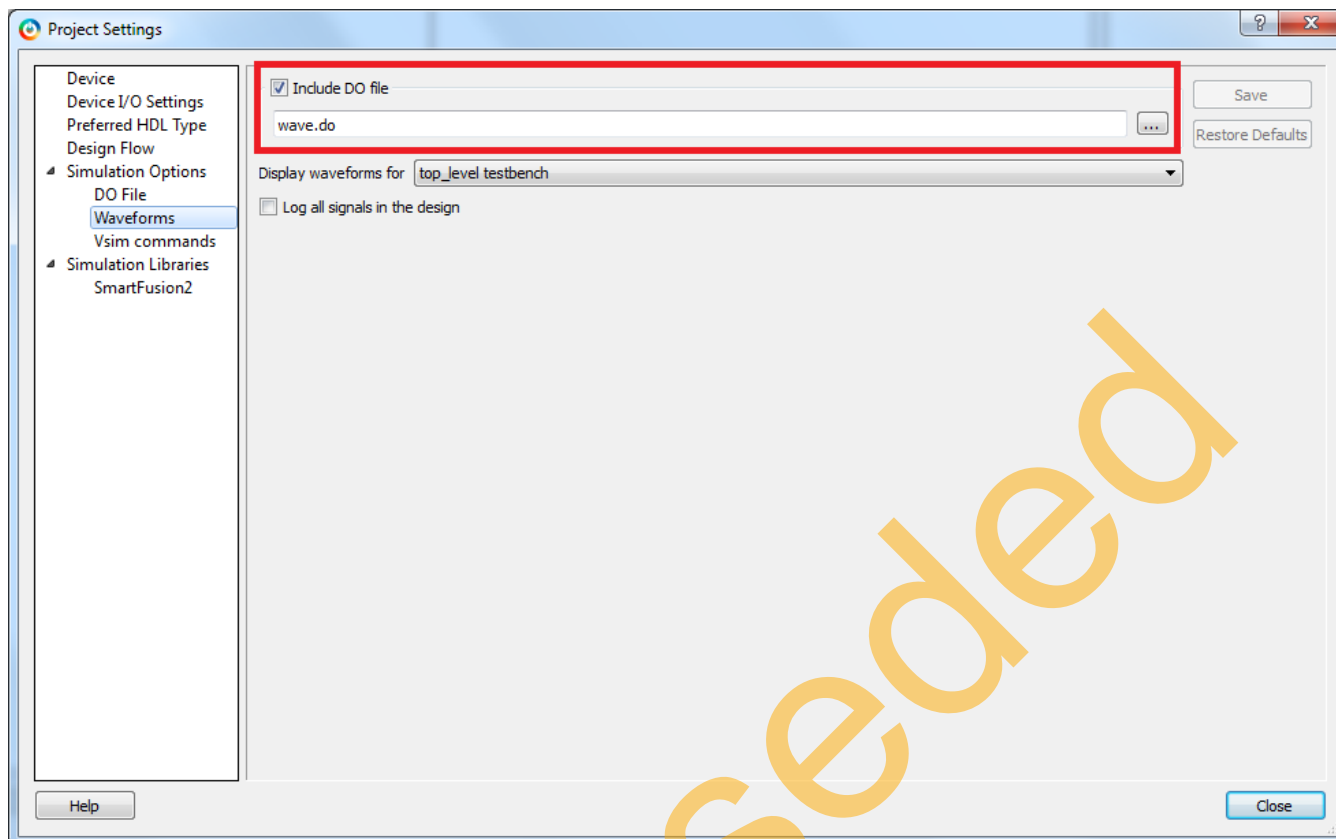


Figure 31. Adding Custom DO File for ModelSim Wave Window

3. Select the **Vsim Commands** option under the **Simulation Options**, and modify the **Resolution** to **1ps**, as shown in Figure 32. This options sets the simulation resolution to 1ps.

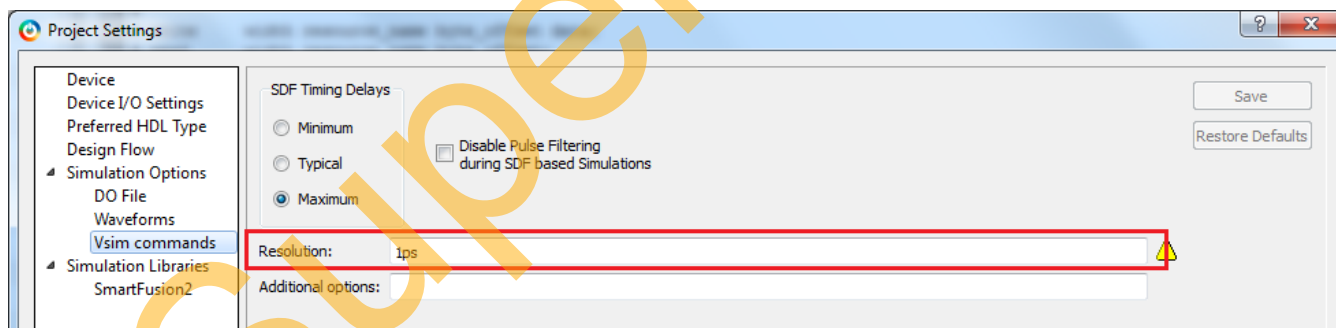


Figure 32. Simulation Resolution

4. Click the **Save** button, then **Close** to exit the **Project Settings** window.
5. On the **Design Flow** tab on Libero SoC, expand the **Verify Pre-Synthesized Design** option and select the **Simulate** option under it:

In the first step, you need to specify which testbench ModelSim will be using during simulation. To do so, right-click the **Simulate** option and select **Organize Input Files > Organize Stimulus Files**. The **Organize Stimulus files of Access_EXT_SDRAM for Simulate tool** window will open. Select **Use List of files organized by** from **Libero** to **User**. Select the default **testbench.v** in the Associated Stimulus files and click **Remove**. Select the **testbench.v** and **mt48lc16m16a2.v** files under Stimulus Files in the project and click the **Add** button to add them to the Associated Stimulus files, as shown in Figure 33.

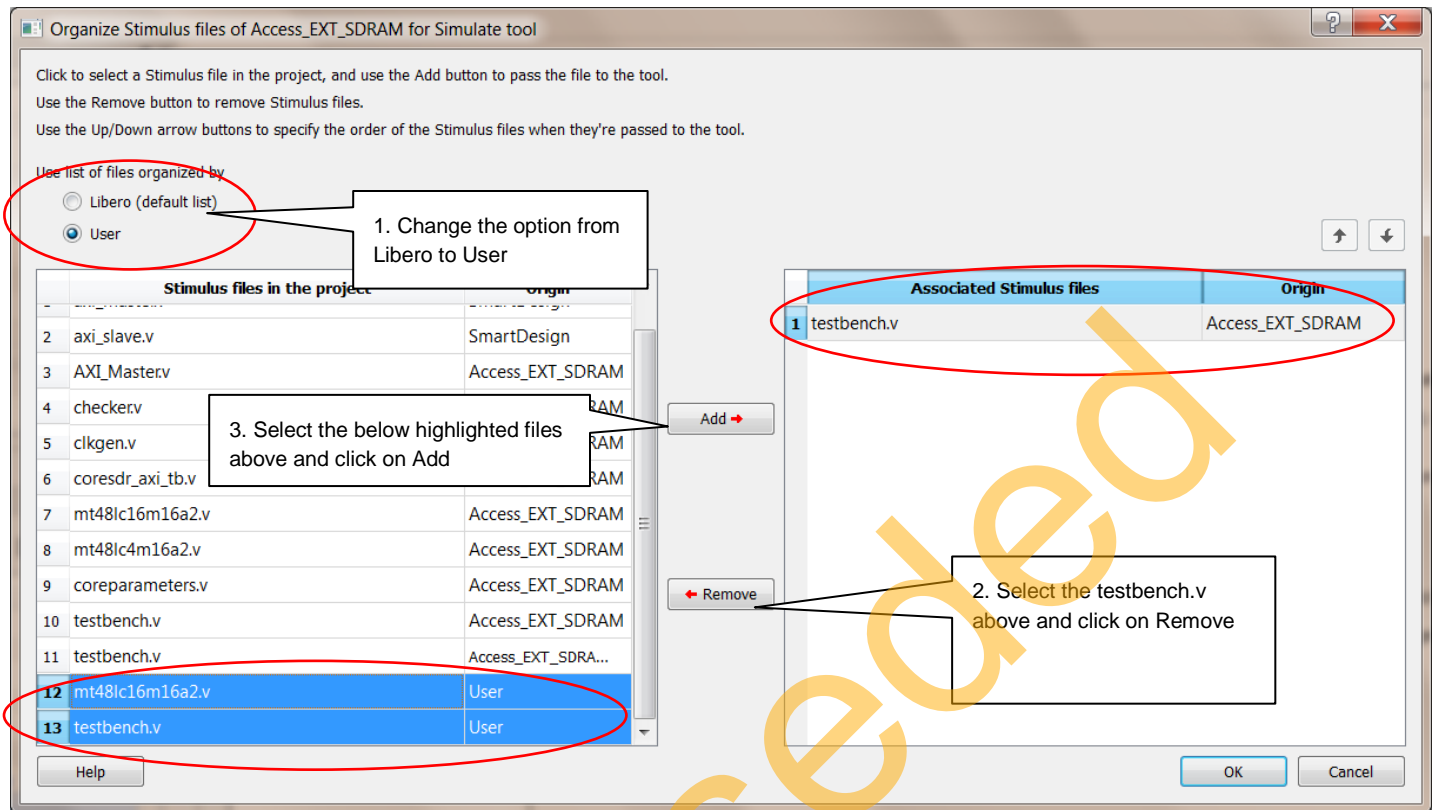


Figure 33. Organizing Stimulus Files

Once you have organized the stimulus file, the above window will look similar to [Figure 34](#). If the files are not in the order, as shown in [Figure 34](#), then use up and down arrows to move the files in correct order.

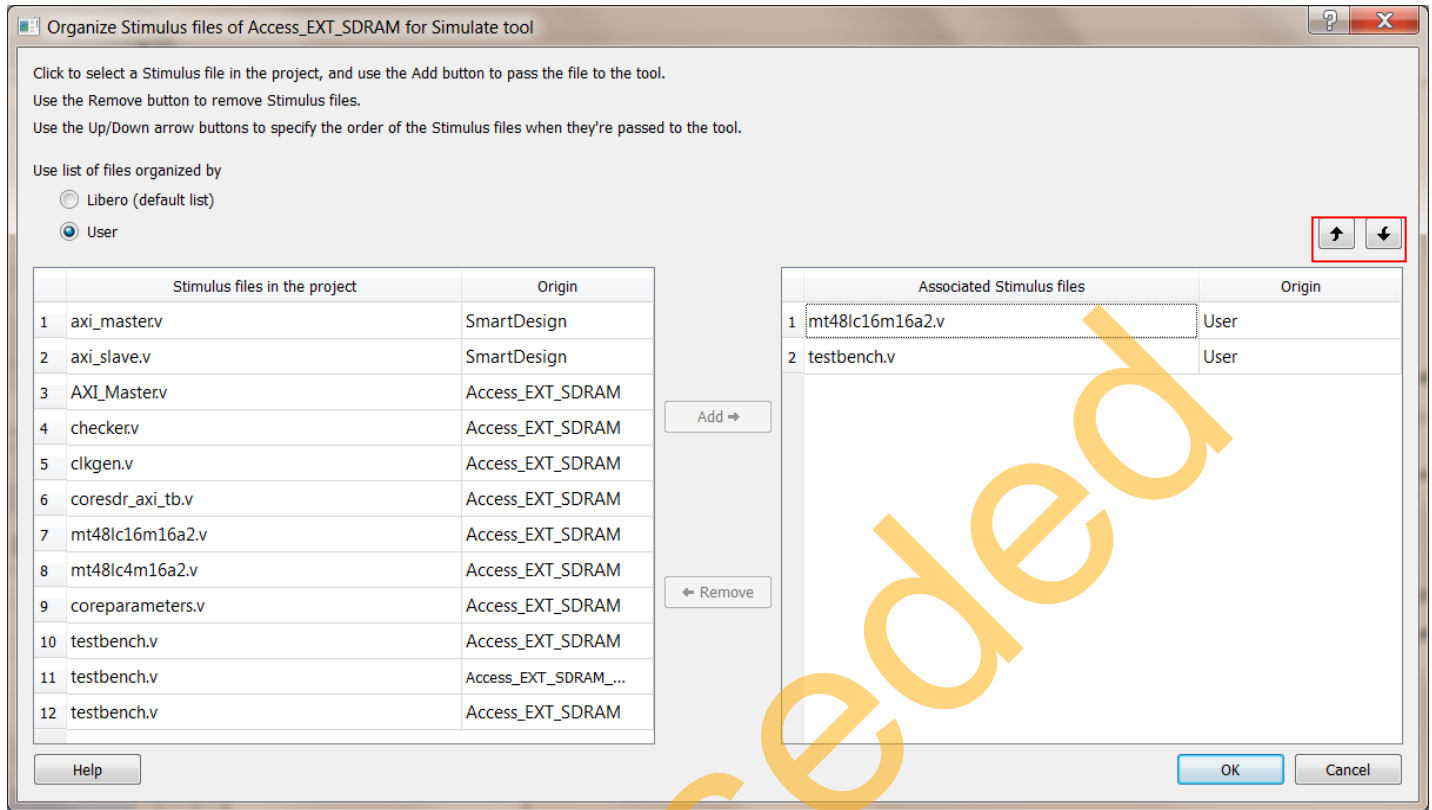


Figure 34. Organized Stimulus Files for the Simulation

Click **OK** to close the Organize Stimulus files dialog box.

After specifying the testbench stimulus file, expand the **Verify Pre-Synthesized Design** option, select the **Simulate** option under it, right-click and select **Open Interactively** to invoke ModelSim, as shown in [Figure 35](#). ModelSim will be invoked and will load the design.

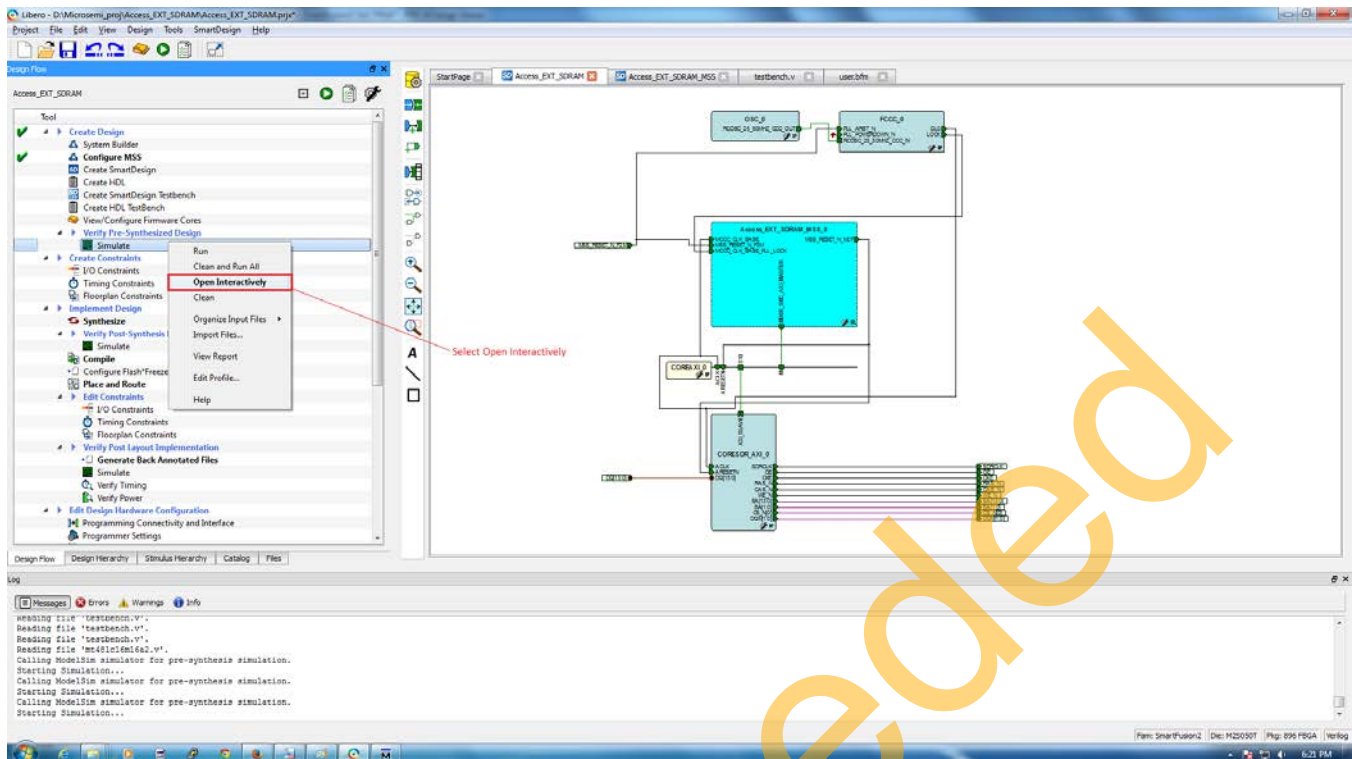


Figure 35. Invoke ModelSim

Step 11: Seeing the Simulation Results

1. ModelSim runs the design for about 158 us, as specified in the Project Settings window. Once the simulation has run completely, **undock** the Wave window. The Wave window can be undocked by clicking the **Dock/Undock** button on the Wave window, as shown in Figure 36.



Figure 36. Dock/Undock

2. Once the Wave window has been undocked, click the **Zoom Full** button to fit all the waveforms in the single view (Figure 37).

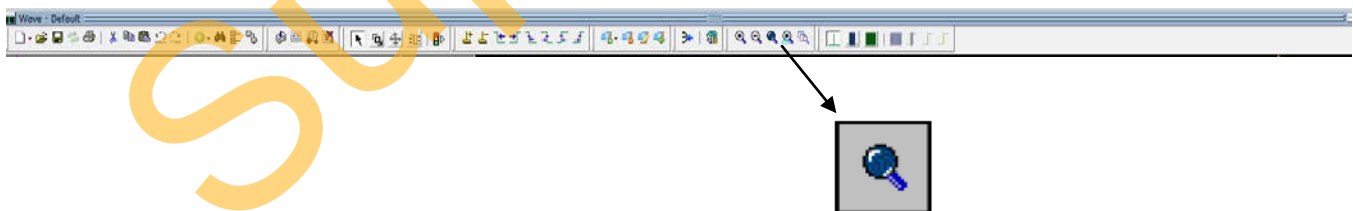


Figure 37. Zoom Full

- Place the cursor at 155 us on the Wave window and click the **Zoom In on the Active Cursor** button to zoom in at that location, as shown in Figure 38. Click as needed until you see the complete write and read transactions to the external SDR SDRAM in the Wave window, as shown in Figure 39.

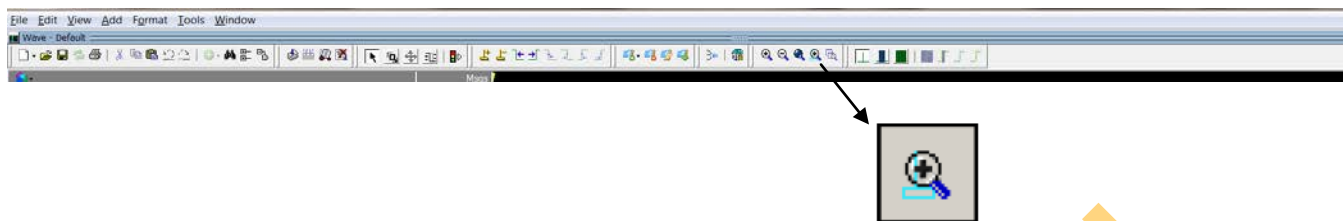


Figure 38. Zoom In on the Active Cursor

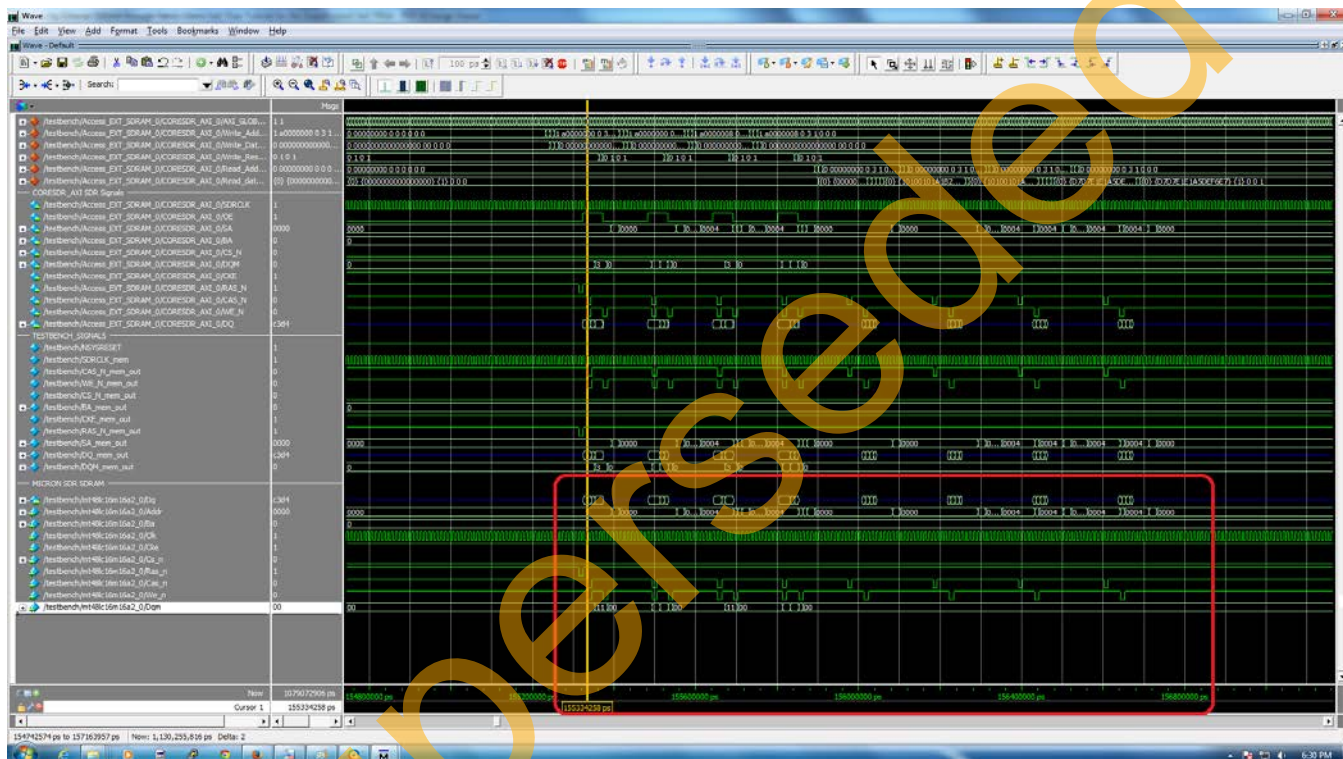


Figure 39. Write/Read transactions

Analyze the Read and Write transactions as on the Wave window by expanding the required signals.

4. The simulation results can also be seen on Transcript Window of ModelSim, as shown in [Figure 40](#).

```

# BFM: Data Read a0000000 a1b2c3d4 MASK:ffffffff at 156082.058000ns
# BFM: Data Read a0000004 10100101 MASK:ffffffff at 156291.722000ns
# BFM: Data Read a0000008 a5def6e7 MASK:ffffffff at 156501.386000ns
# BFM: Data Read a000000c d7d7e1e1 MASK:ffffffff at 156711.050000ns

BDM BFM Simulation Complete - 200 Instructions - NO ERROR

```

Figure 40. Transcript Window

You will see the following messages printed in the Transcript Window:

```

# BFM: Data Read a0000000 a1b2c3d4 MASK:ffffffff at 156082.058000ns
# BFM: Data Read a0000004 10100101 MASK:ffffffff at 156291.722000ns
# BFM: Data Read a0000008 a5def6e7 MASK:ffffffff at 156501.386000ns
# BFM: Data Read a000000c d7d7e1e1 MASK:ffffffff at 156711.050000ns

```

In the BFM script provided in the user.bfm file earlier, the readcheck command reads the data from the AXI bus and verifies whether the data read matches with the value provided along with the readcheck command. If the value read does not match, the simulation will error out.

5. Quit the ModelSim simulator by selecting **File > Quit**.

Conclusion

That concludes this tutorial.

In this tutorial, you created a new project in Libero SoC, configured the MSS component to access an external SDR SDRAM memory through the fabric, added and configured the CoreSDR_AXI IP inside the fabric, and connected the IP to the MSS component. You configured the fabric and MSS CCC blocks to generate the clocks.

Finally, you verified the design in ModelSim using AMBA AXI BFM simulation.

Superseded

List of Changes

Revision	Changes	Page
Revision 7 (May 2014)	Updated the document for Libero version 11.3 (SAR 56971).	NA
Revision 6 (November 2013)	Updated the document for Libero version 11.2 (SAR 52903).	NA
Revision 5 (April 2013)	Updated the document for 11.0 production SW release (SAR 47102).	NA
Revision 4 (March 2013)	Updated the document for Libero 11.0 Beta SP1 software release (SAR 44867).	NA
Revision 3 (November 2012)	Updated the document for Libero 11.0 beta SPA software release (SAR 42845).	NA
Revision 2 (October 2012)	Updated the document for Libero 11.0 beta launch (SAR 41584).	NA
Revision 1 (May 2012)	Updated the document for LCP2 software release (SAR 38953).	NA

Note: The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.

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