SmartFusion2 SoC FPGA Demo: Error Detection and Correction of eSRAM Memory

User's Guide

Microsemi

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SmartFusion2 SoC FPGA - Error Detection and Correction of eSRAM Memory

Introduction

This demo is intended to demonstrate the error detection and correction (EDAC) capabilities of SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) on the embedded static random-access memory (eSRAM). The EDAC controllers implemented in SmartFusion2 SoC FPGAs support single error correction and double error detection (SECDED). All memories within the microcontroller subsystem (MSS) of the SmartFusion2 SoC FPGA are protected by SECDED. The eSRAM memory can be eSRAM_0 or eSRAM_1. The address range of eSRAM_0 is 0x20000000 to 0x20007FFF and the address range of eSRAM_1 is 0x20008000 to 0x2000FFFF.

When SECDED is enabled, a write operation computes and adds 8 bits of SECDED code to every 32 bits of data, and a read operation reads and checks the data against the stored SECDED code to support 1-bit error correction and 2-bit error detection.

In this demo the error detection and corrections can be identified by the blinking LED on the board and by GUI.

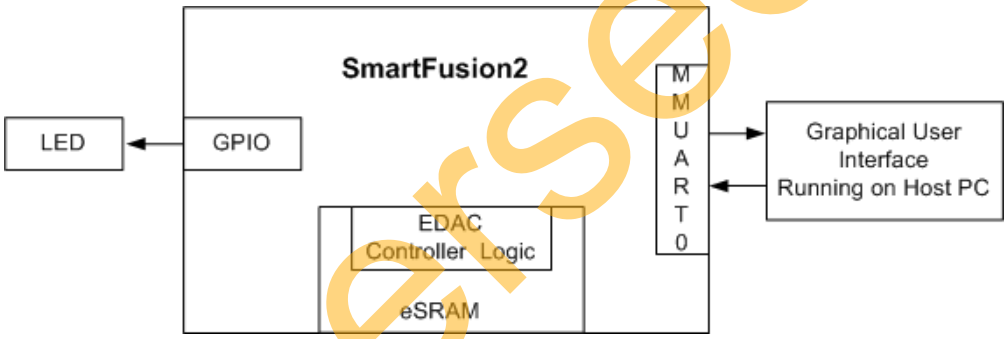

Figure 1. Top Level Block Diagram of the Demo

The EDAC of eSRAM supports the following features:

1. SECDED mechanism
2. Provides interrupts to the ARM® Cortex™-M3 processor and to FPGA fabric upon the detection of a 1-bit error or 2-bit error.
3. Stores the number of 1-bit and 2-bit errors to the error counter registers.
4. Stores the address of the last 1-bit or 2-bit error affected memory location.
5. Stores the 1-bit or 2-bit error data into the SECDED registers.
6. Provides error bus signals to the FPGA fabric

Refer to the EDAC chapter of the SmartFusion2 Reliability and Security User's Guide and the eSRAM chapter of the SmartFusion2 Cortex-M3 User's Guide.

Demo Requirements

Hardware and Software Requirements

The hardware and software required to run the demo are listed in the below Table 1:

Table 1. Required Hardware and Software to Run the Demo

Hardware	**Version**
SmartFusion2 Development Kit	Rev C or later
FlashPro4 programmer	
USB A to Mini - B USB cable	
12 V Adapter	
Software	
FlashPro Programming Software	11.3
USB to UART drivers	
Microsoft .NET Framework 4 client for launching demo GUI	
Operating system	Windows XP SP2 – 32-bit/64-bit Windows 7 – 32-bit/64-bit

Design Files

The design files for this demo can be downloaded from the Microsemi website:
http://soc.microsemi.com/download/rsc/?f=SF2_eSRAM_EDAC_DF

Design files include:

1. Libero® System-on-Chip (SoC) project
2. Programming files
3. GUI executable
4. Readme file

Refer to the Readme.txt file provided in the design files for the complete directory structure.

Demo Design Description

Each eSRAM within the MSS is protected by a dedicated EDAC controller. EDAC detects a 1-bit error or 2-bit error when data is read from the memory. If EDAC detects the 1-bit error, the EDAC controller corrects the same error bit. If EDAC is enabled for all the 1-bit and 2-bit errors, corresponding error counters in the system registers are incremented and corresponding interrupts and error bus signals to the FPGA fabric are generated.

In a single event upset (SEU) susceptible environment, random access memory (RAM) is prone to transient errors caused by heavy ions. This happens in real-time scenario. To demonstrate this, the error is introduced manually and detection and correction is observed.

This demo design involves implementation of following tasks:

1. Enable EDAC
2. Write data to eSRAM
3. Read data from eSRAM
4. Disable EDAC
5. Corrupt one or two bits
6. Write data to eSRAM
7. Enable EDAC

8. Read the data
9. In the case of a 1-bit error, the EDAC controller corrects the error, updates the corresponding status registers, and gives the data written in step 2 at the read operation done at step 8.
10. In the case of a 2-bit error, a corresponding interrupt is generated and the application must correct the data or take the appropriate action in the interrupt handler. These two methods are demonstrated in this demo.

There are two tests implemented in this demo: loop test and manual test and these two are applicable to both 1-bit and 2-bit errors.

Loop Test

This method is executed when the SmartFusion2 SoC FPGA receives a loop test command from the GUI. Initially all the error counters and EDAC related registers are placed in the **RESET** state. Now the following steps are executed for each iteration.

1. Enable the EDAC controller.
2. Write the data to the specific eSRAM memory location.
3. Disable the EDAC controller.
4. Write the 1-bit or 2-bit error induced data to the same eSRAM memory location.
5. Enable the EDAC controller.
6. Read the data from the same eSRAM memory location.
7. Send the 1-bit or 2-bit error detection and 1-bit error correction data incase of 1-bit error to the GUI.

Manual Test

This method allows manual testing for enabling/disabling EDAC and write/read operations. Using this method, 1-bit or 2-bit errors can be introduced to any location within the eSRAM. Enable the EDAC and write data to the specified address using the GUI fields. Disable the EDAC and write 1-bit or 2-bit corrupted data to the same address location. Enable the EDAC and read the data from the same address location then the light-emitting diode (LED) on the board should blink to notify the detection and correction of errors. The corresponding error counter is displayed on to the GUI. The GUI Serial Console will log all the actions performed in the SmartFusion2 SoC FPGA.

The flow chart shown in Figure 2 explains the eSRAM EDAC demo operations.

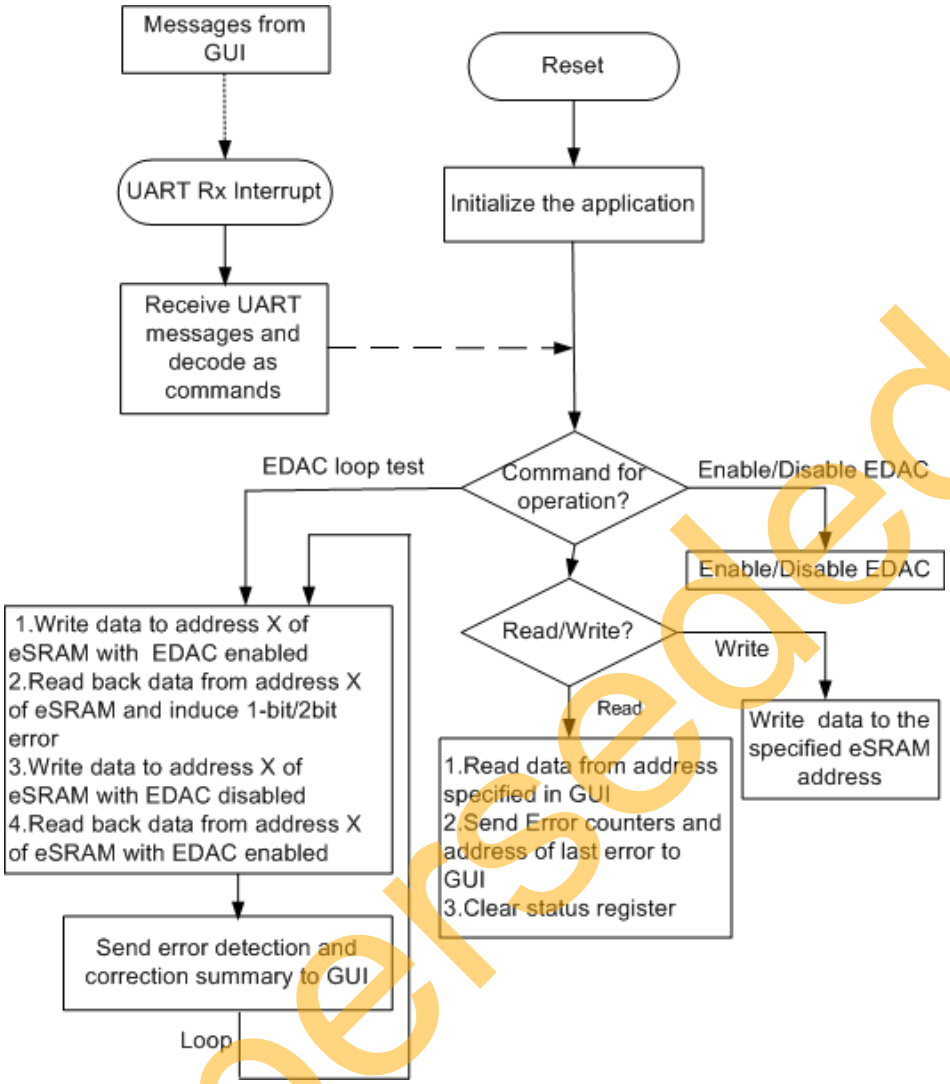

Figure 2. Design Flow

Running the Demo

This section describes the Development Kit Board setup, the graphical user interface (GUI) options, and how to execute the demo design.

Demo Setup

1. Connect the FlashPro4 programmer to the J59 connector of SmartFusion2 SoC FPGA Development Kit
2. Connect one end of the USB mini-B cable to the J24 connector provided in the SmartFusion2 Development Kit. Connect the other end of the USB cable to the host PC. Make sure that the USB to UART Bridge drivers are automatically detected (can be verified in the Device Manager), as shown in Figure 3.

   Note: Copy the COM port number for serial port configuration. Ensure that the COM port **Location** is specified as 'on USB Serial Converter D' as shown in Figure 3.

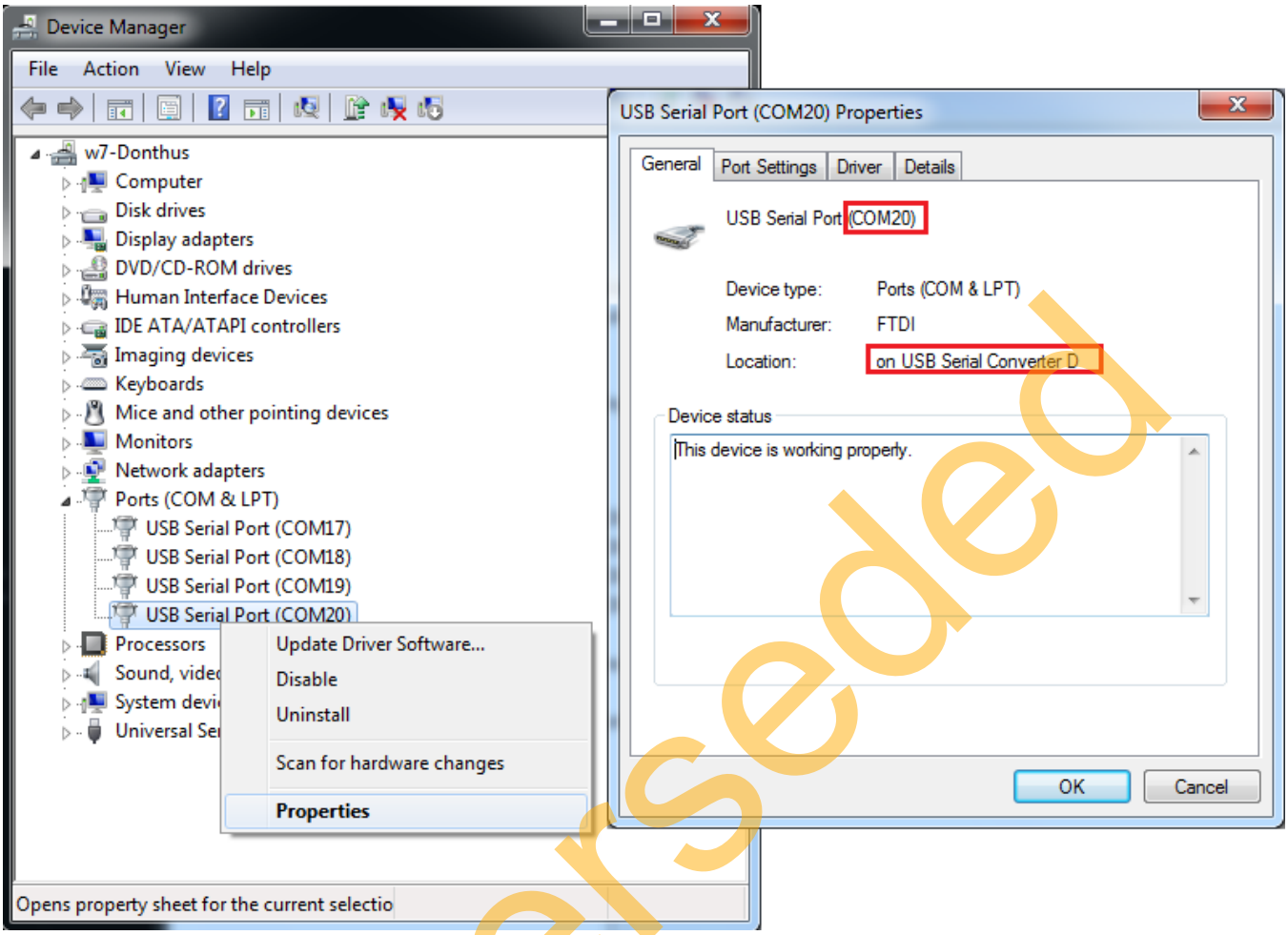

Figure 3. USB to UART Bridge Drivers

3. If USB to UART bridge drivers are not installed, download and install the drivers from www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip
4. Connect the jumpers on the SmartFusion2 Development Kit, as shown in Table 2. While making the jumper connections, the power supply switch SW7 on the board should be in the **OFF** position.

Table 2. SmartFusion2 SoC FPGA Development Kit Jumper Settings

Jumper	Pin (from)	Pin (to)
J70, J93, J94, J117, J123, J142, J157, J160, J167, J225, J226, J227	1 (default)	2
J2	1 (default)	3
J23	2 (default)	3
J129, J133	2	3

5. Connect the power supply to J18 connector.

Figure 4 shows the board setup for running the demo on the SmartFusion2 Development Kit.

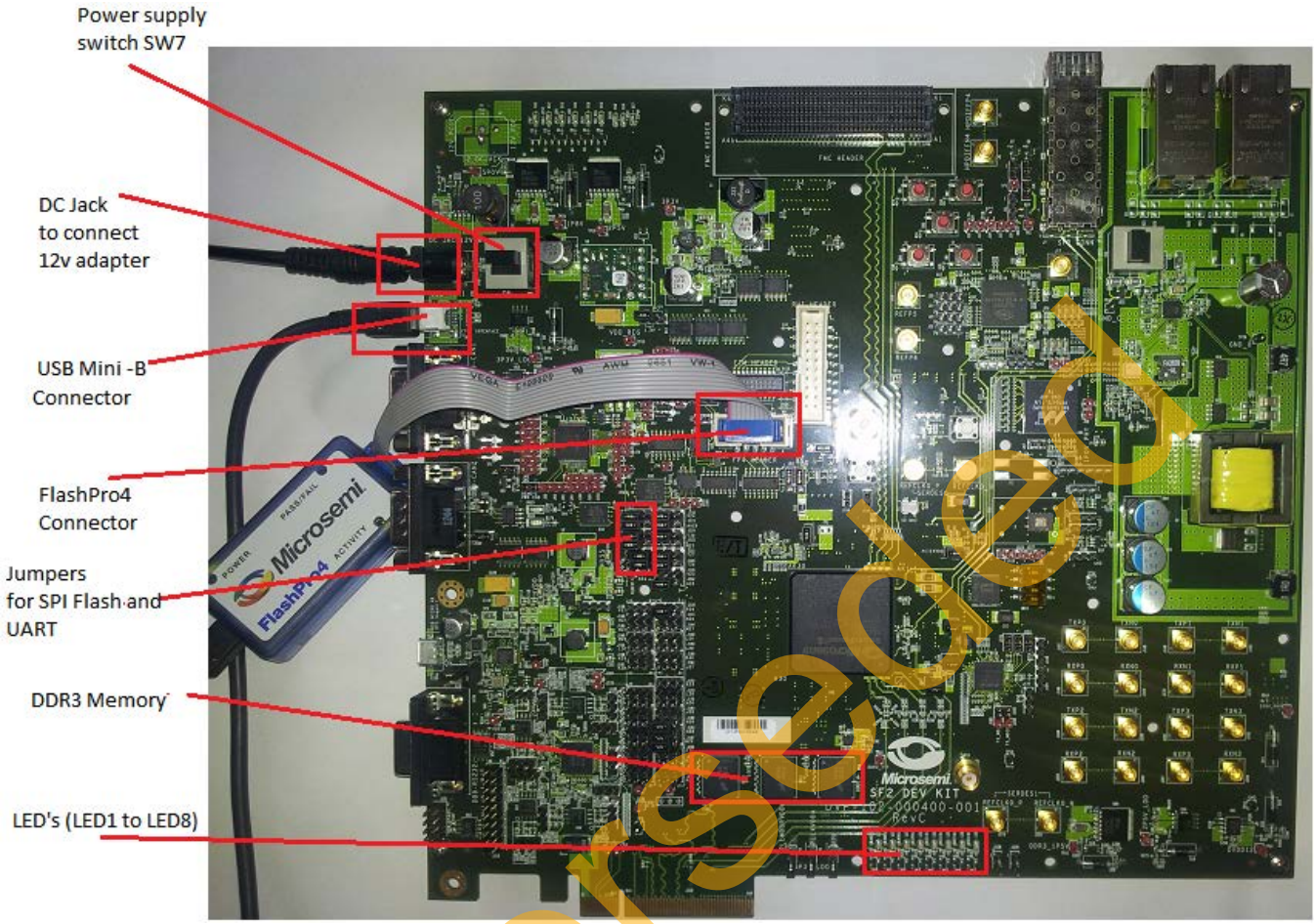

Figure 4. SmartFusion2 SoC FPGA Development Kit Board Setup

Graphical User Interface

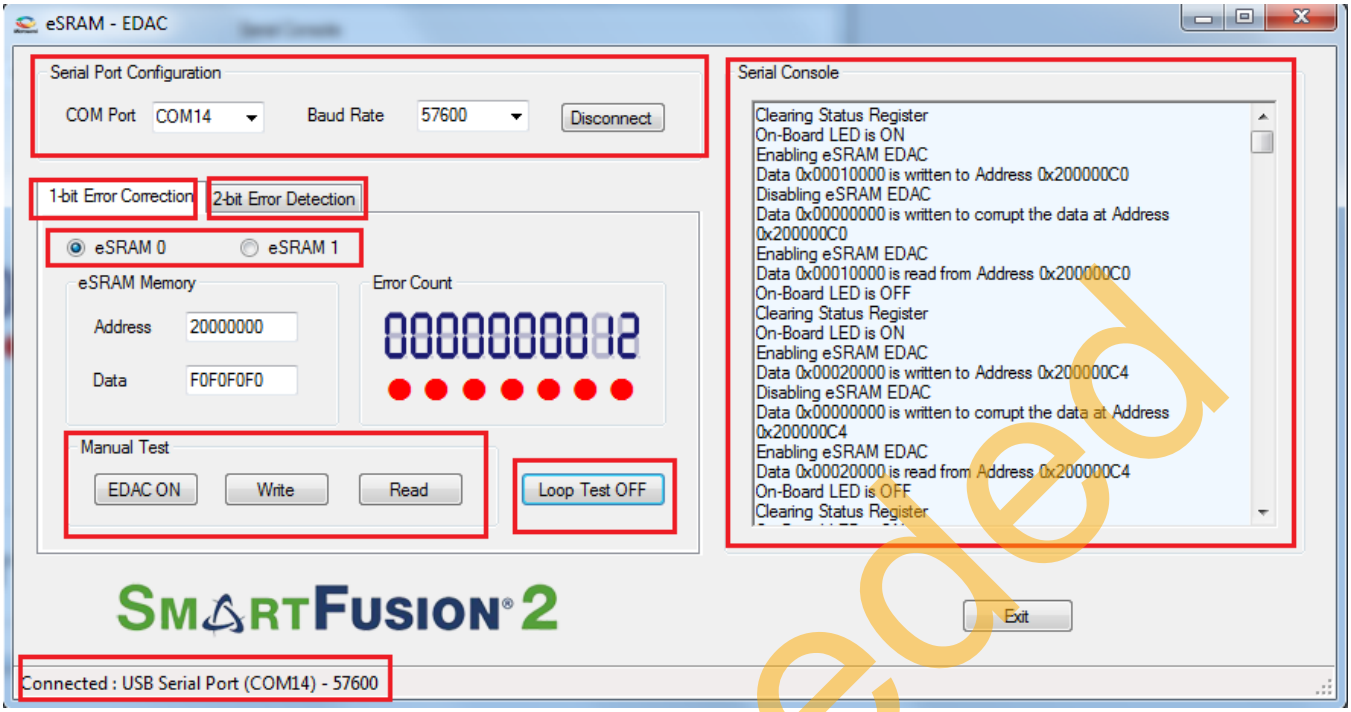

Figure 5. eSRAM – EDAC Demo GUI

The GUI supports the following features:

1. Selection of COM port and Baud Rate.
2. Selection of 1-bit error correction tab or 2-bit error detection tab.
3. Selection of eSRAM0 or eSRAM1.
4. Address field to write or read data to or from specified eSRAM address.
5. Data field to write or read data to or from specified eSRAM address.
6. Serial Console section to print the status information received from the application.
7. **EDAC ON/OFF** - enables or disables the EDAC.
8. **Write** - allows to write data to the specified address.
9. **Read** - allows to read data from the specified address.
10. **LOOP test ON/OFF** - allows to test the EDAC mechanism in a loop method.

Running the Design

1. Change the power supply switch SW7 to the **ON** position.
2. Program the SmarFusion2 device with the programming file provided in the design files (\ProgrammingFiles\eSRAM_0\EDAC_Demo_ESRAM0.stp or \ProgrammingFiles\eSRAM_1\EDAC_Demo_ESRAM1.stp) using FlashPro design software, as shown in Figure 6.

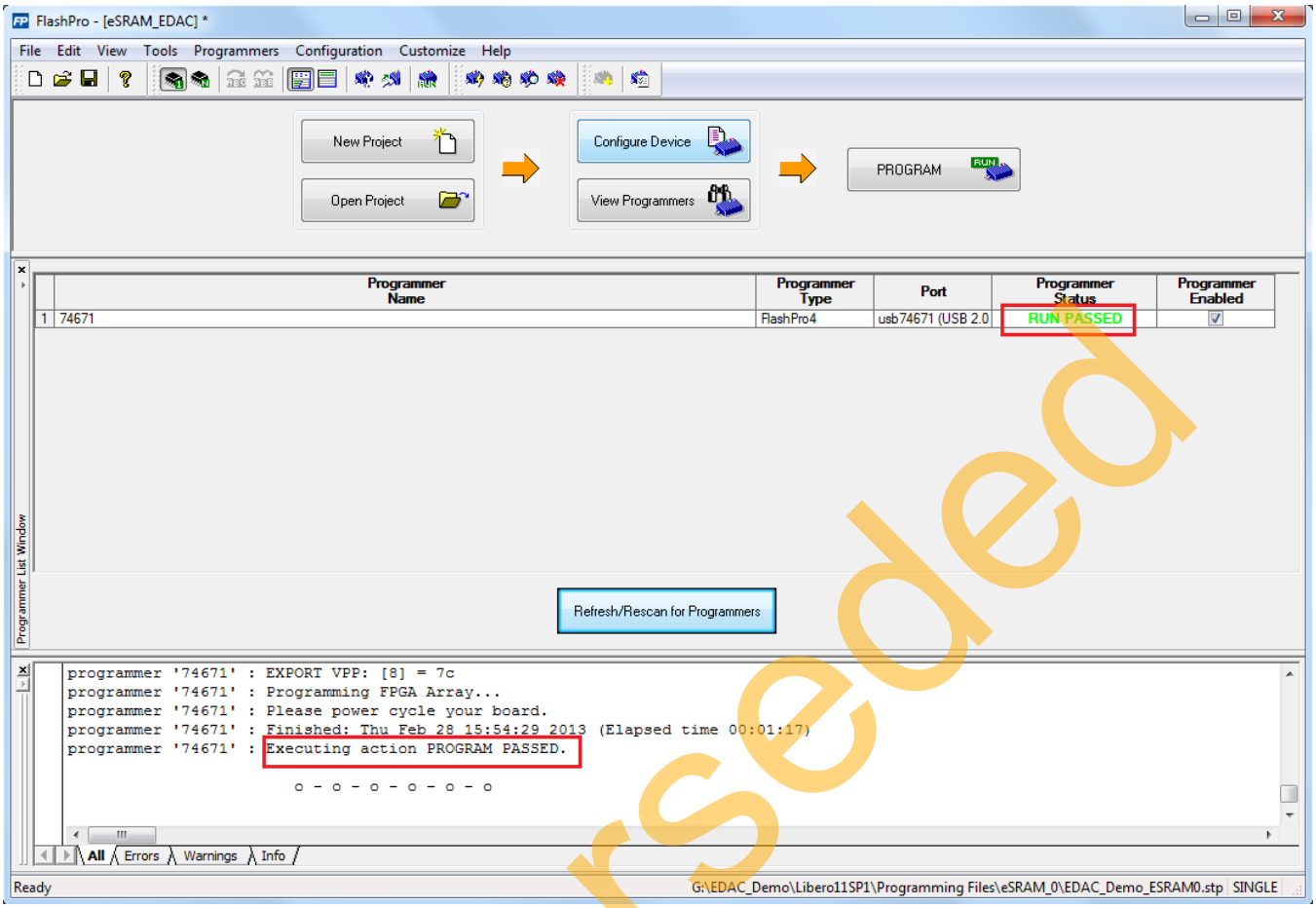

Figure 6. FlashPro Programming Window

3. Press **SW9** switch to Reset the board after successful programming.
4. Launch the **EDAC_eSRAM Demo** GUI executable file available in the design files (\GUI Executable\ EDAC_eSRAM.exe). The GUI window is displayed, as shown in Figure 5.
5. Select the appropriate COM port (to which USB to UART Bridge drivers are pointed) from the **COM Port** drop-down list.
6. Select the **Baud Rate** as 57600 and click **Connect**. After establishing the connection, **Connect** changes to **Disconnect**.
7. Select eSRAM 0 or eSRAM 1 depending upon the programming file selected in step 2.
8. Select the 1-bit **Error Correction** tab or 2-bit **Error Detection** tab, as shown in Figure 7 and Figure 8.
9. Two types of tests can be performed: Manual and Loop.

Performing Loop Test

Click **Loop Test ON**. It runs in loop mode where continuous correction and detection of errors is done. The loop runs for 200 iterations. All actions performed in the SmartFusion2 SoC FPGA are logged in the **Serial Console** section of the GUI. The 2-bit Error Detection loop test prints the error affected eSRAM address offset in Serial Console.

Table 3. eSRAM Memory Addresses Used in Loop Test

Memory	1-bit error correction	2-bit error detection
eSRAM0	0x20000000	0x20002000
eSRAM1	0x20008000	0x2000A000

Performing Manual Test

In this method, errors are introduced manually using GUI. Use the following steps to execute 1-bit error correction or 2-bit error detection.

1. Input Address and Data fields (use 32-bit Hexadecimal values).
2. Click **EDAC ON**.
3. Click **Write**.
4. Click **EDAC OFF**.
5. Just change one bit (in case of 1-bit error correction) or two bits (in case of 2-bit error detection) in Data field (introducing error).
6. Click **Write**.
7. Click **EDAC ON**.
8. Click **Read**.
9. Observe Error Count display and Data field in the GUI. The error count value increases by 1.

All the actions performed in SmartFusion2 SoC FPGA are logged in Serial Console section of GUI.

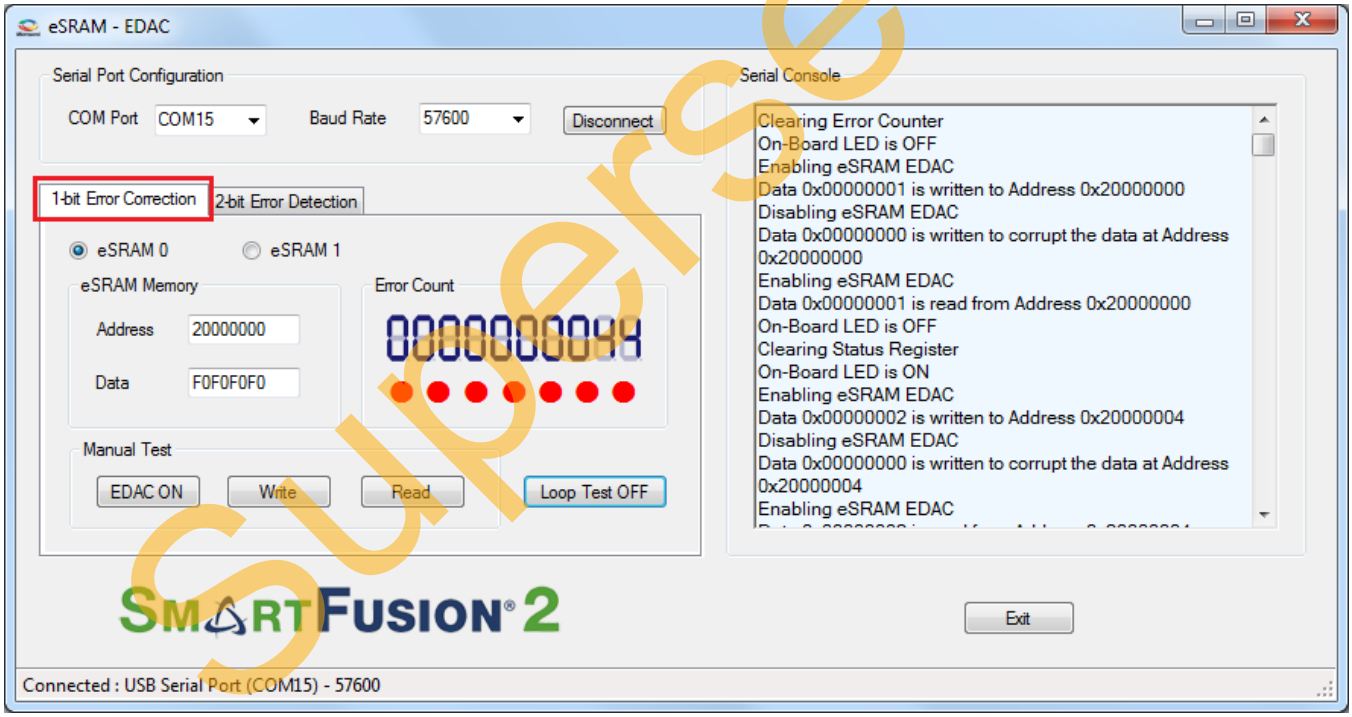

Figure 7. 1-Bit Error Correction Tab

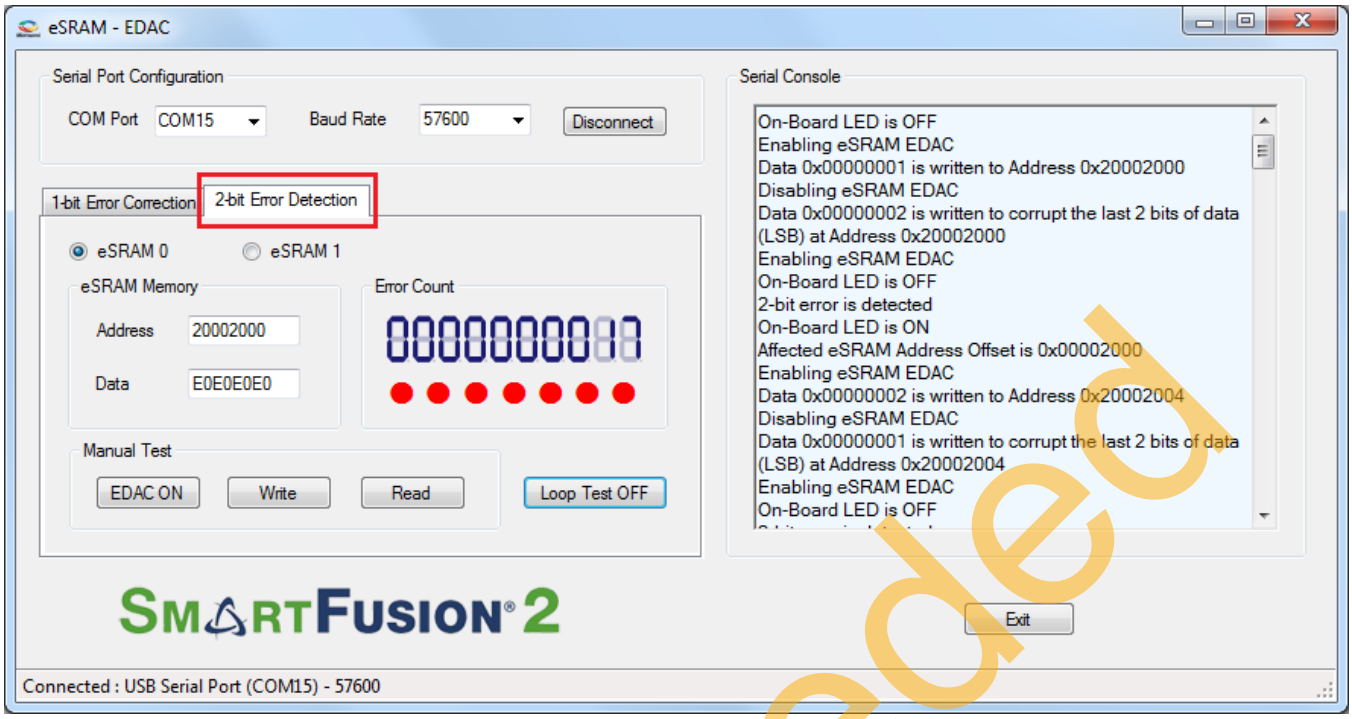

Figure 8. 2-Bit Error Detection Tab

Conclusion

This demonstration shows SmartFusion2 SECDED capabilities of the eSRAM.

List of Changes

Revision	Changes	Page
Revision 4 (May 2014)	Updated the document for Libero SoC v11.3 software release (SAR 56852).	NA
Revision 3 (November 2013)	Updated the document for Libero SoC v11.2 software release (SAR 52960).	NA
Revision 2 (May 2013)	Updated the document for Libero SoC v11.0 software release (SAR 47858).	NA
Revision 1 (March 2013)	Updated the document for Libero SoC v11.0 Beta SP1 (SAR 45586).	NA
Note: The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.		

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From the rest of the world, call **650.318.4460**
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