SmartFusion2 SoC FPGA DSP FIR Filter

Demo Guide

July 2014

Microsemi

Revision History

Date	Revision	Change
2 July 2014	2	Third release
30 November 2013	1	Second release
22 April 2013	0	First release

Confidentiality Status

This is a non-confidential document.

Table of Contents

Preface

About this document

This demo is for SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) devices. It provides instructions on how to use the corresponding reference design.

Intended Audience

SmartFusion2 devices are used by:

- FPGA designers
- Embedded designers
- System-level designers

References

Microsemi Publications

- SmartFusion2 Microcontroller Subsystem User Guide
- SmartFusion2 System Builder User Guide
- SmartFusion2/IGLOO2 Digital Signal Processing Reference Guide

See the following web page for a complete and up-to-date listing of SmartFusion2 device documentation: http://www.microsemi.com/products/fpga-soc/soc-fpga/sf2docs

SmartFusion2 SoC FPGA - DSP FIR Filter Demo

Introduction

SmartFusion2 SoC FPGA devices integrate a fourth generation flash-based FPGA fabric and an ARM® Cortex™-M3 processor. SmartFusion2 SoC FPGA fabric includes embedded mathblocks, which are optimized specifically for digital signal processing (DSP) applications such as, finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast fourier transform (FFT) functions.

This demo shows a DSP FIR filter application using the SmartFusion2 device. In this DSP FIR filter application, the FIR filter is implemented in fabric for Low pass, High pass, Band pass, and Band reject filtering operations. The Host interface is implemented in microcontroller subsystem (MSS) to communicate with the Host PC. A user friendly graphical user interface (GUI) generates the filter coefficients, input signals (Pass band frequency + stop band frequency) and also plots the input/output waveforms and the required spectrum. Microsemi® CoreFIR filter IP is used to suppress the unwanted frequency components, and CoreFFT IP is used to generate the output spectrum to verify the filtering operation.

Figure 1 shows the top level diagram for DSP FIR filter demo.

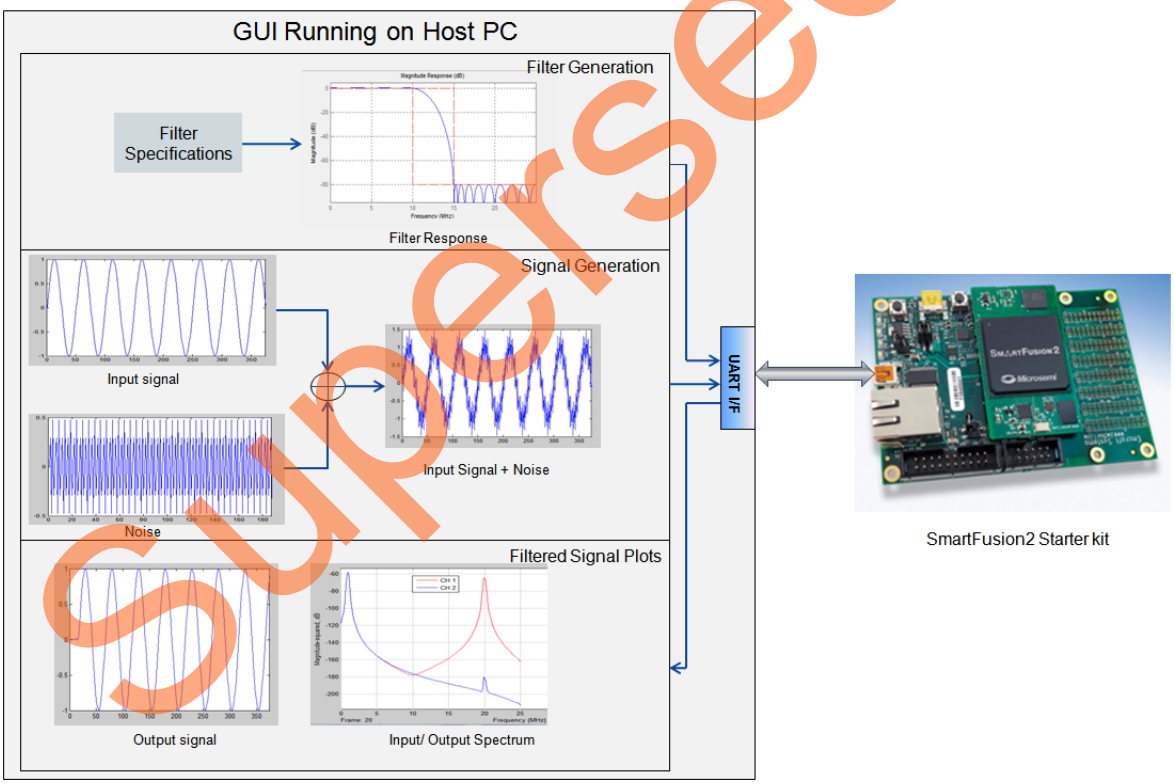

***Figure 1* • Top Level Diagram of DSP FIR Filter Demo**

Design Requirements

Table 1 • **Design Requirements**

Design Requirements	Description
Hardware Requirements	
SmartFusion2 Starter Kit • FlashPro4 programmer • USB A to Mini-B cable	SF2-484-STARTER-KIT
Host PC or Laptop	Windows 7 64-bit Operating System
Software Requirements	
Libero® System-on-Chip (SoC)	11.3
FlashPro Programming Software	11.3
Host PC Drivers	USB to UART drivers
Framework	Microsoft .NET Framework 4 client for launching demo GUI

Demo Design

Introduction

The design files are available for download from the following path in the Microsemi website:
http://soc.microsemi.com/download/rsc/?f=FIR_FILTER_DEMO_DF

The design files include:

- Design files
- Programming file
- GUI executable
- Readme.txt file

Figure 2 shows the top-level structure of the design files. Refer to the Readme.txt file provided in the demo file folder for the complete directory structure.

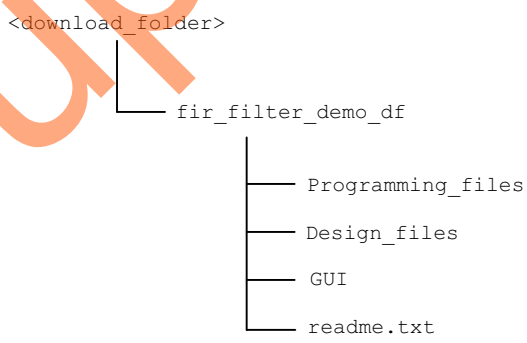

Figure 2 • **Demo Design Files Top-Level Structure**

Demo Design Description

This demo design uses the following blocks:

- "MSS Block"
- "Control Logic" (user RTL)
- "TPSRAM IP" (IPcore)
- "CoreFIR" (IPcore)
- "CoreFFT" (IPcore)

Figure 3 shows the detailed block diagram of the demo design.

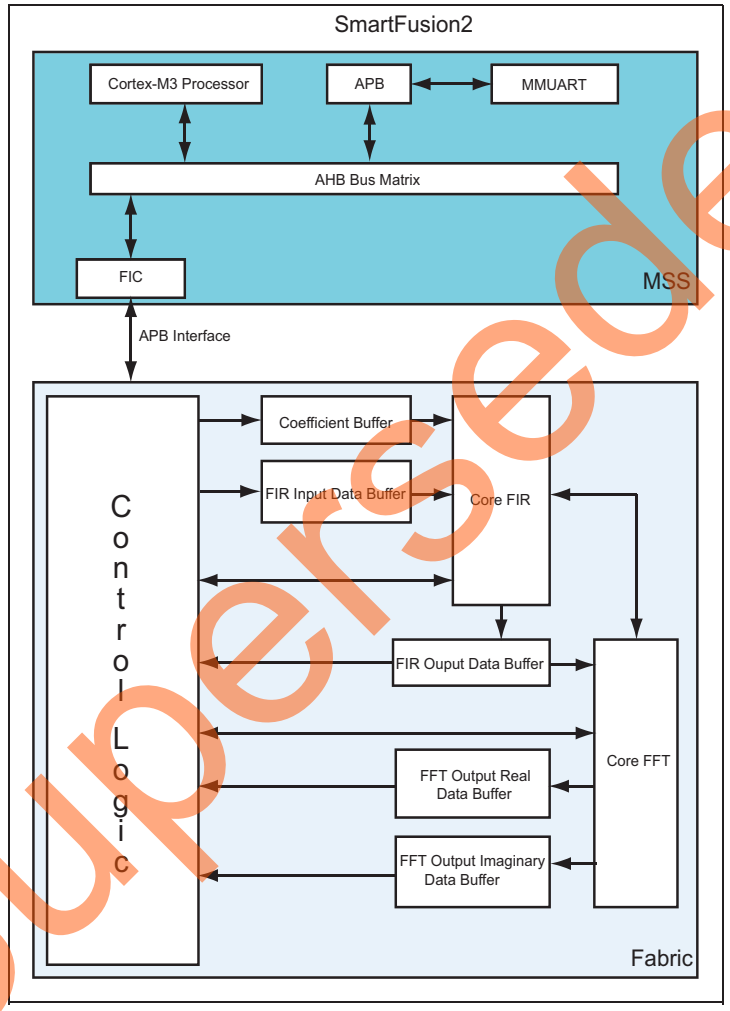

***Figure 3* • DSP FIR Filter Demo Design Block Diagram**

MSS Block

MSS block sends and receives the data between Host PC (GUI interface) and fabric logic. MMUART interface is used to communicate with the Host PC. FIC_0 interface (APB master) is used to communicate with the fabric user logic.

Control Logic

This is the user logic implemented in the fabric and consists of the following two finite-state machine (FSM)s:

- **Data Handling**: Implements and controls operations like loading the filter input data to the corresponding input data buffer and loading filter coefficients to the corresponding coefficient memory buffers. An APB bus slave is implemented to communicate with the MSS APB master.
- **Filter Control**: Controls the FIR filter and FFT operations. Loads the filtered data to corresponding output buffer and moves the FFT output data to the corresponding output data buffer.

TPSRAM IP

TPSRAM IP is used to implement the following:

- Filter coefficient buffer (depth: 63, width: 16)
- Input signal data buffer (depth: 1024, width: 16)
- Output signal buffer (depth: 1024, width: 16)
- Output signal FFT real data buffer (depth: 1024, width: 16)
- Output signal FFT imaginary data buffer (depth: 1024, width: 16)

CoreFIR

The Core FIR IP is used in Reloadable coefficient mode to support Low pass, High pass, Band pass, and Band reject filters. Core FIR IP configuration is as follows:

- Version: 8.5.104
- Filter Type: Single rate fully enumerated
- No of taps: 31
- Coefficients type: Reloadable
- Coefficients bit width: 16(signed)
- Data bit width: 16 (signed)
- Filter structure: Transposed with symmetry

CoreFFT

The Core FFT IP is used for generating the frequency spectrum of the filtered data. Core FFT IP configuration is as follows:

- Version: 6.3.102
- FFT Architecture: In place
- FFT type: Forward
- FFT Scaling: Conditional
- FFT Transform Size: 256
- Width: 16

Setting Up the Demo Design

The following steps describe how to setup the hardware demo:

1. Connect the jumpers on the SmartFusion Starter Kit board as shown in Table 2.

Table 2 • **SmartFusion2 Starter Kit Jumper Settings**

Jumper	Configuration	Comments
JP1	1-2 Closed, 3-4 Open	Enable power on the M2S-FG484 SOM (VCC3)
JP2	1-2 Open, 3-4 Closed	Select appropriate JTAG mode and enable power to the SmartFusion2 JTAG controller.
JP3	1-3 Open, 2-4 Closed	Use the mini-USB port as the power source

2. Connect the FlashPro4 programmer to the P5 connector of the SmartFusion2 Starter Kit board.
3. Connect the Host PC USB port to the P1 Mini USB connector on the SmartFusion2 Starter Kit board using the USB Mini-B cable.

   Figure 4 shows the board setup for running the DSP FIR filter demo on the SmartFusion2 Starter Kit.

Figure 4 • **SmartFusion2 SoC FPGA Starter Kit Setup**

4. Ensure that the USB to UART bridge drivers are automatically detected. This can be verified in the **Device Manager** of the Host PC. Figure 5 shows the USB Serial port.

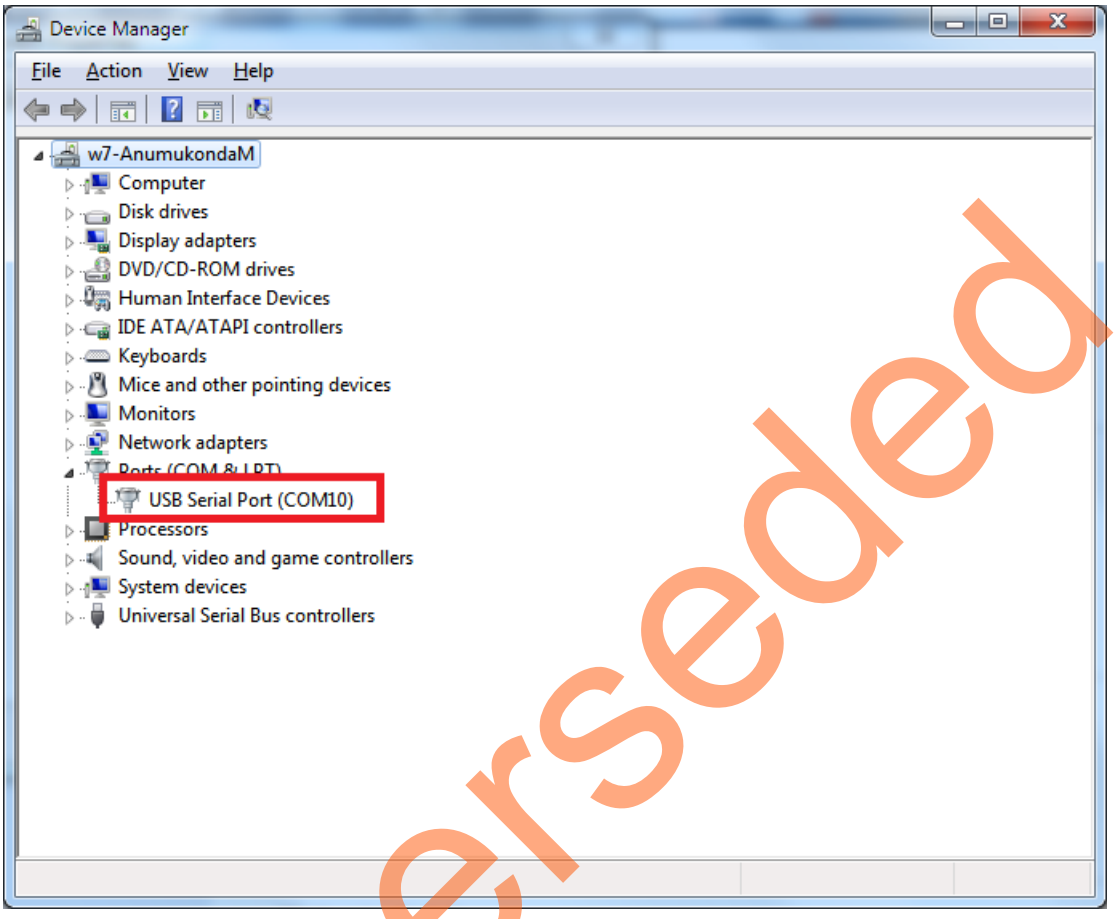

Figure 5 • **USB to UART Bridge Drivers**

5. If USB to UART bridge drivers are not installed, download and install the drivers from www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip.

Programming the Demo Design

The following steps describe how to program the demo design:

1. Download the demo design from: http://soc.microsemi.com/download/rsc/?f=FIR_FILTER_DEMO_DF
2. Launch the FlashPro software.
3. Click **New Project**.

4. In the **New Project** window, type the project name as SF2_FIR_FILTER.

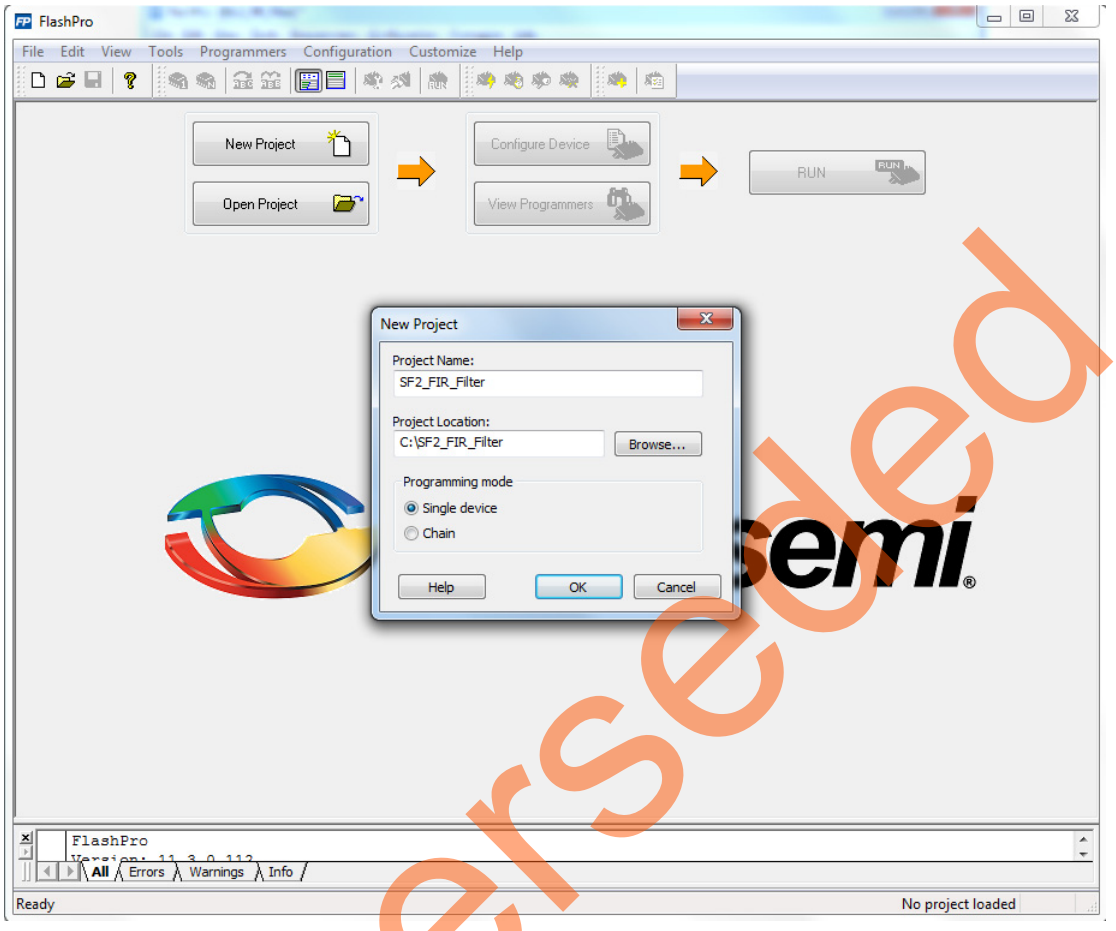

***Figure 6* • FlashPro - New Project**

5. Click **Browse** and navigate to the location where you want to save the project.
6. Select **Single device** as the **Programming mode**.
7. Click **OK** to save the project.

Setting Up the Device

The following steps describe how to configure the device:

1. Click **Configure Device** on the FlashPro GUI.
2. Click **Browse** and navigate to the location where the `FILTER_FIR_DEMO.stp` file is located and select the file. The default location is: *<download_folder>\FIR_FILTER_DEMO_DF\ProgrammingFiiles\FILTER_FIR_DEMO.stp*.
3. Click **Open**. The required programming file is selected and is ready to be programmed in the device.

Programming the Device

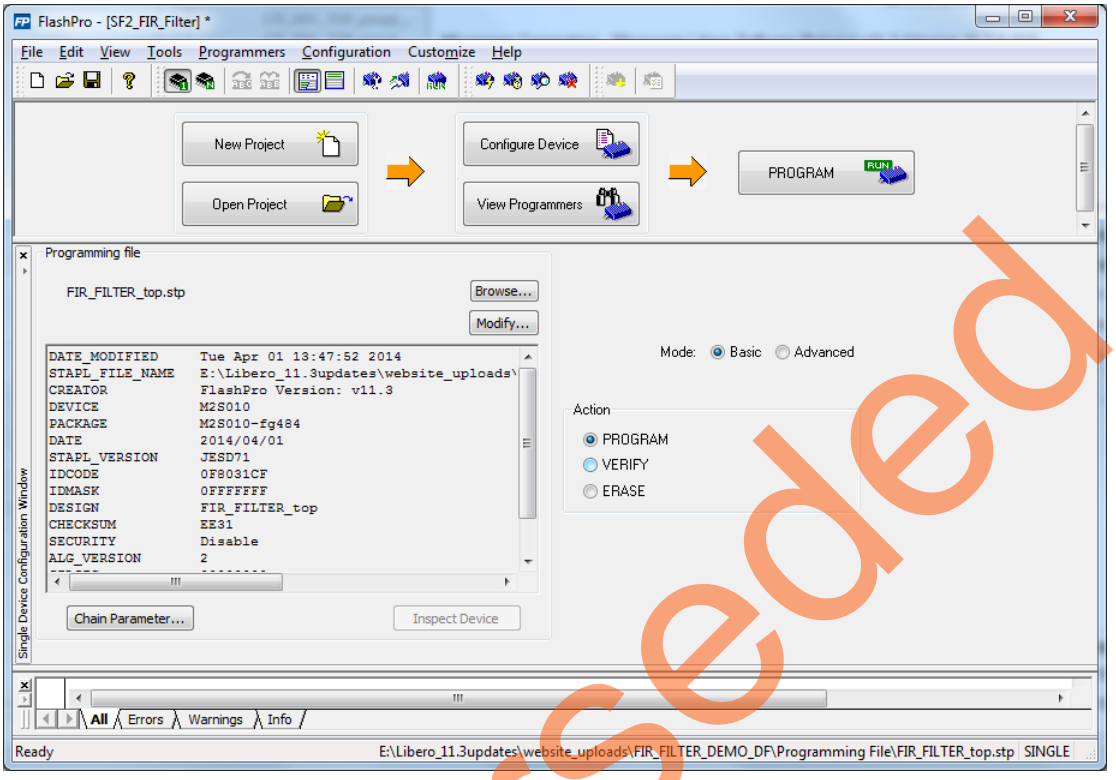

Figure 7 • **FlashPro Project Configured**

The following steps describe how to program the device:

1. Click **PROGRAM** to start programming the device. Wait until you get a message indicating that the **RUN PASSED**.

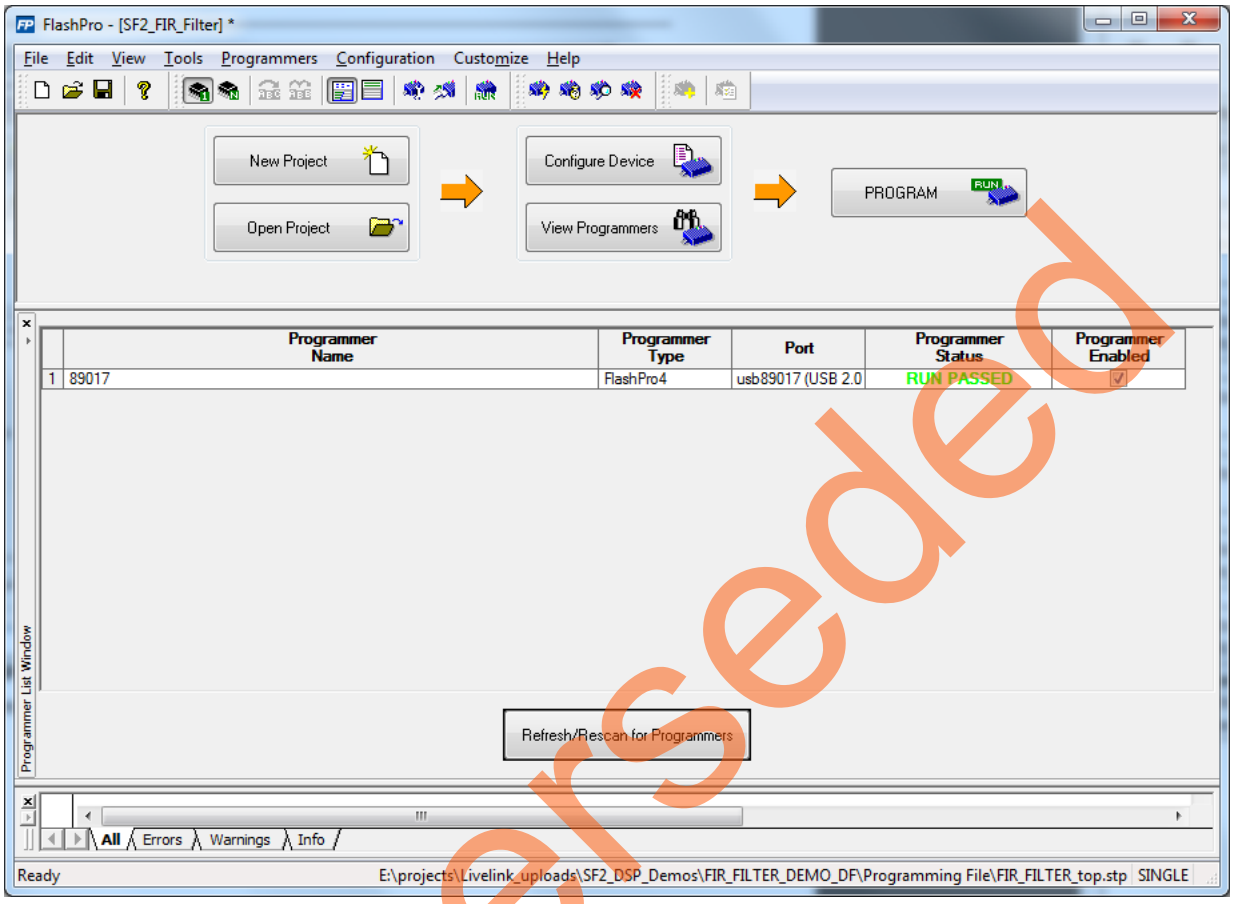

Figure 8 • **FlashPro Project RUN Passed**

DSP FIR Demo GUI

The DSP FIR demo is provided with a user-friendly GUI that runs on the Host PC which communicates with the SmartFusion2 Starter Kit. The UART is used as the underlying communication protocol between the Host PC and the SmartFusion2 Starter Kit. Figure 9 shows the DSP FIR demo GUI.

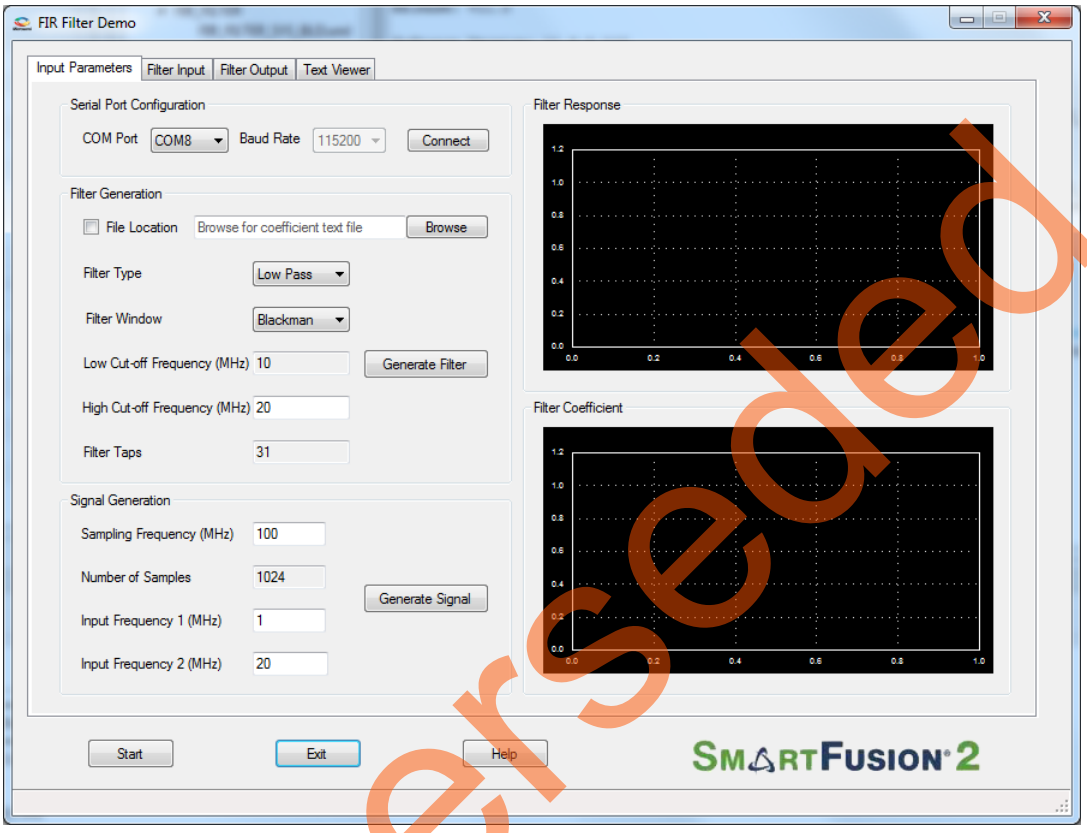

***Figure 9* • DSP FIR Demo Window**

The DSP FIR demo window consists of the following tabs:

- **Input Parameters**: Configures the serial COM port, filter generation, and signal generation.
- **Filter Input**: Plots the input signal and its frequency spectrum
- **Filter Output**: Plots the output signal and its frequency spectrum
- **Text Viewer**: Shows the coefficients, input signal, output signal, and FFT data values

Click **Help** for more information on the GUI.

Running the Demo Design

1. Launch the DSP FIR Demo GUI executable file available in the design files (*\\FIR_FILTER_DEMO_DF\GUI\SF2_FIR_Filter.exe*). The FIR Filter Demo window is displayed, refer to Figure 10.

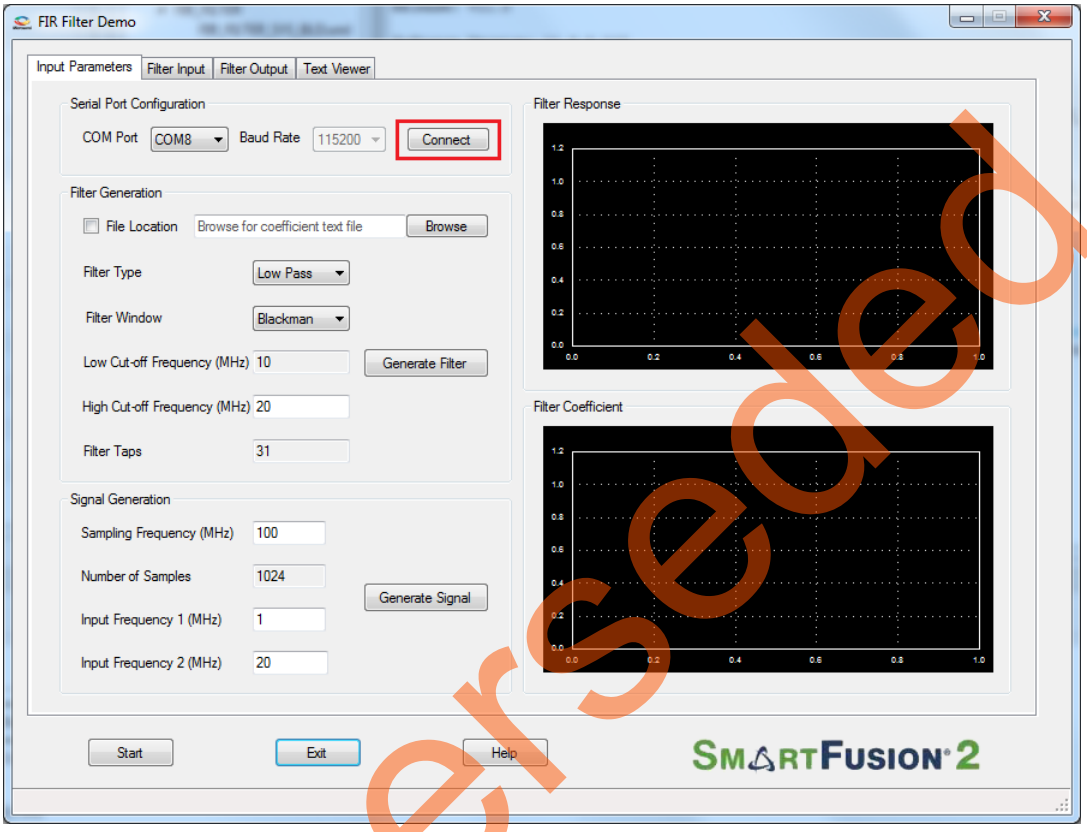

***Figure 10* • Serial Port Configuration**

2. **Serial Port Configuration**: The COM port number is automatically detected and baud rate is fixed at 115200. Press **Connect** as shown in Figure 10.
3. **Filter Generation**: Two options are provided for generating the filter coefficients:

- Generate the coefficients using MATLAB or any similar tool and save it as a text file (Refer "Appendix 3 - Coefficient Text File Format" for the format of the text file). The GUI can be used to browse and load this file as shown in Figure 11.

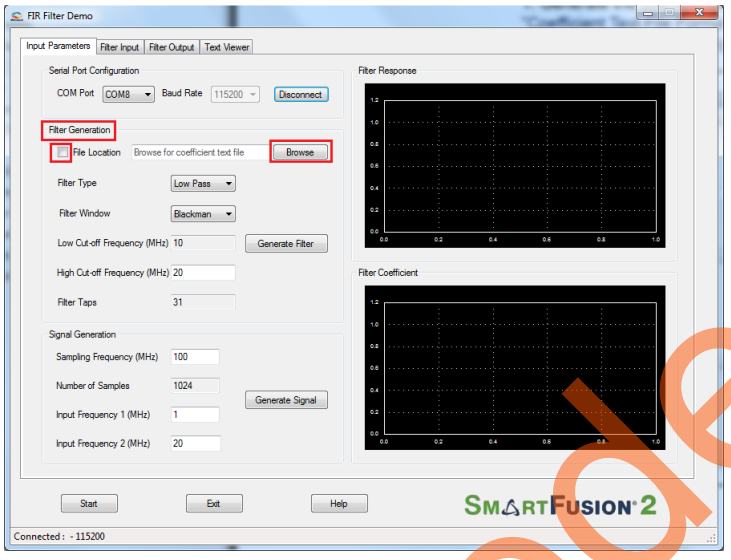

***Figure 11* • Filter Generation - 1**

- Generate the Filter coefficients using GUI as given below:

  The following parameters are required to generate filter coefficients. Refer to Figure 12 on page 17.

  – **Filter Type**: Low Pass (Low-pass/High-pass /Band-pass/Band-reject filter)
  – **Filter Window**: Blackman (Blackman/Hamming window)
  – **Low Cut-off Frequency**: Disabled for Low-pass filter required (High cut-off frequency is disabled for High-pass filter)
  – **High Cut-off Frequency**: 20 MHz
  – **Filter Taps**: 31 (Fixed)

  Press **Generate Filter** to generate the filter coefficients.

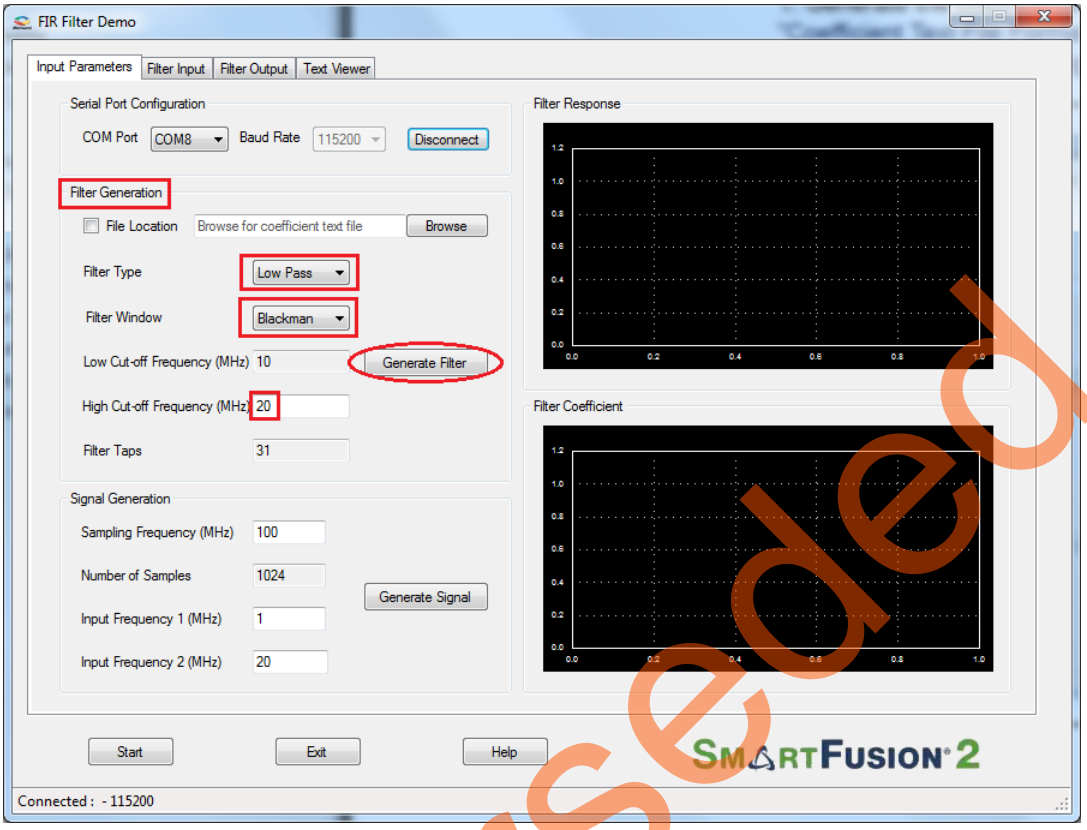

***Figure 12* • Filter Generation - 2**

4. The successful after-generation graphs of the filter coefficients, filter response, and the filter coefficient plots, are displayed. Refer to Figure 13.

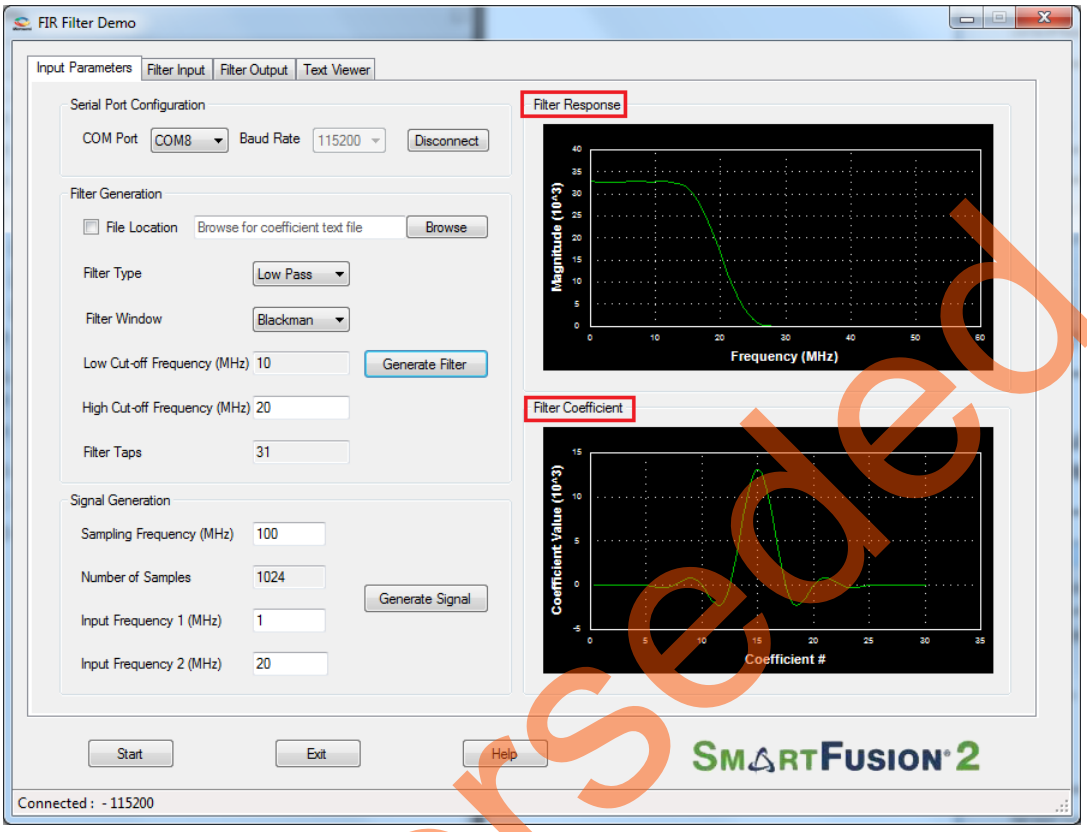

***Figure 13* • Filter Response and Filter Coefficient Plot**

5. **Signal Generation**:
   - **Sampling Frequency**: 100 MHz (Fixed)
   - **Number of Samples**: 1024 (Fixed)
   - **Input Frequency 1**: Enter the signal frequency in the Pass-band region. For example, 1 MHz to High cut-off frequency.
   - **Input Frequency 2**: Enter the signal frequency in the Stop-band region. For example, High cut-off frequency to Sampling frequency/2.

   Click **Generate Signal**, as shown in Figure 14.

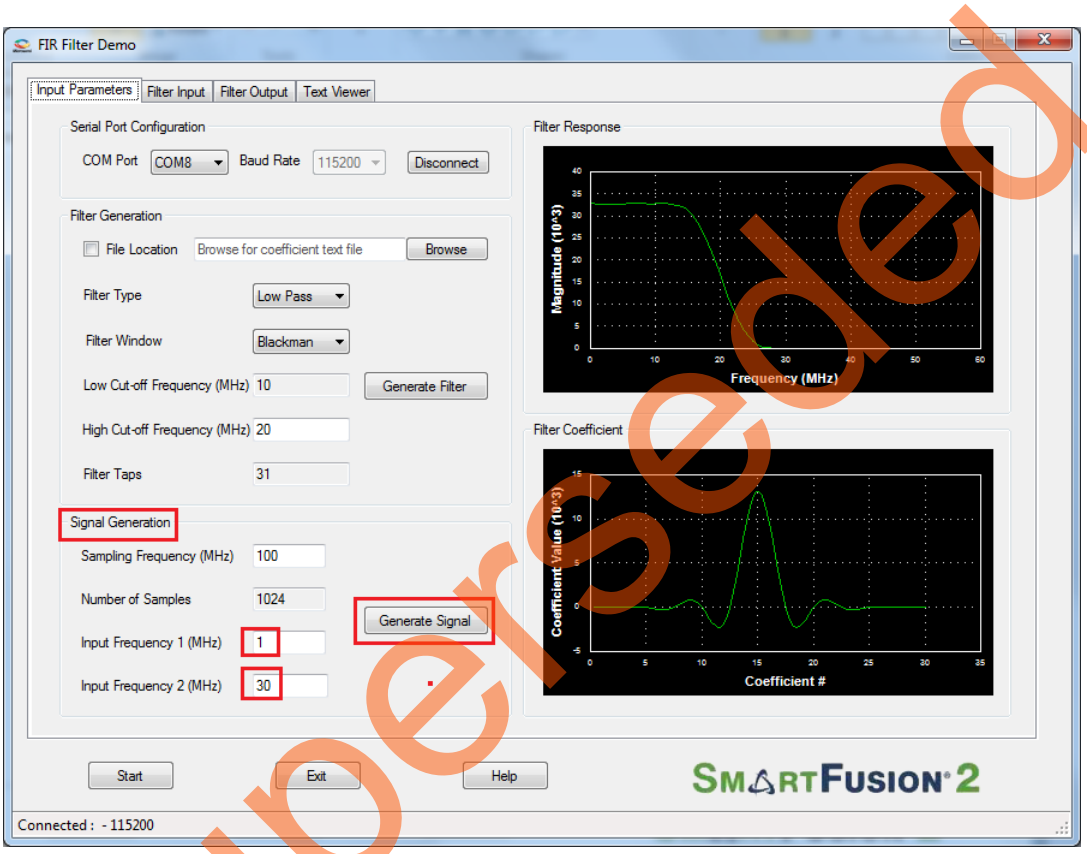

Figure 14 • **Signal Generation**

6. Input signal and the frequency spectrum of the specified signal are displayed as shown in Figure 15.

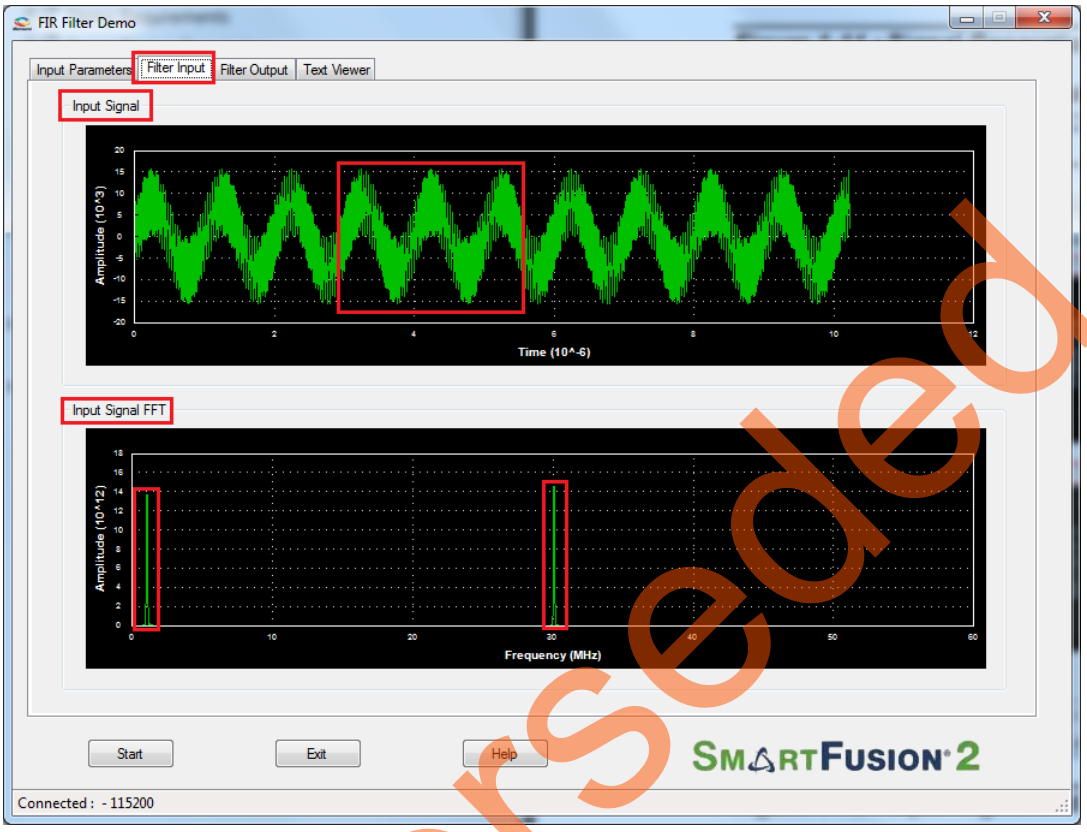

***Figure 15* • Input Signal and Input Signal FFT Plot**

7. To configure the input frequencies and coefficients click **Start**. Refer to Figure 16 on page 21. It sends the input data (1K samples) and filter coefficients to the SmartFusion2 device for processing the filtering operation.

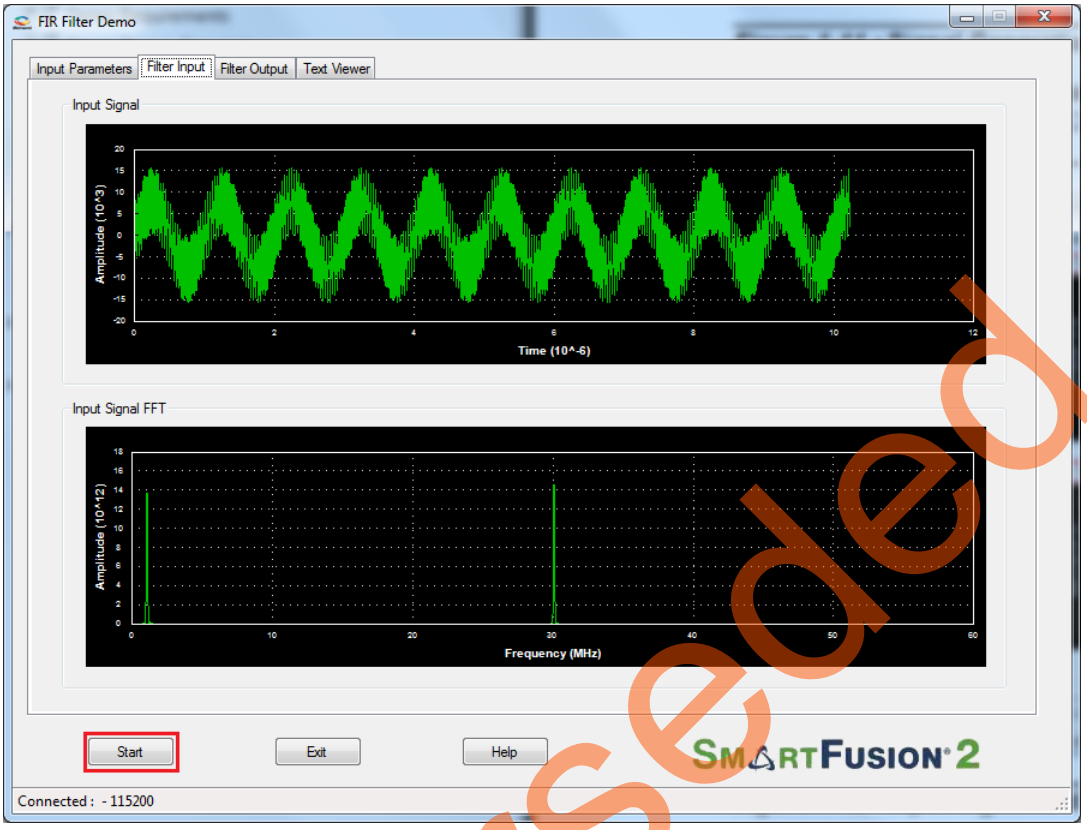

***Figure 16* • DSP FIR Filter Demo Start**

8. After completing the filter operation by SmartFusion2, the GUI plots the filtered data and FFT data on filter output window, refer to Figure 17. Since Low-pass filter option was selected, the High frequency component is suppressed while the Low frequency signal is preserved. This can be observed in the frequency spectrum of the output signal.

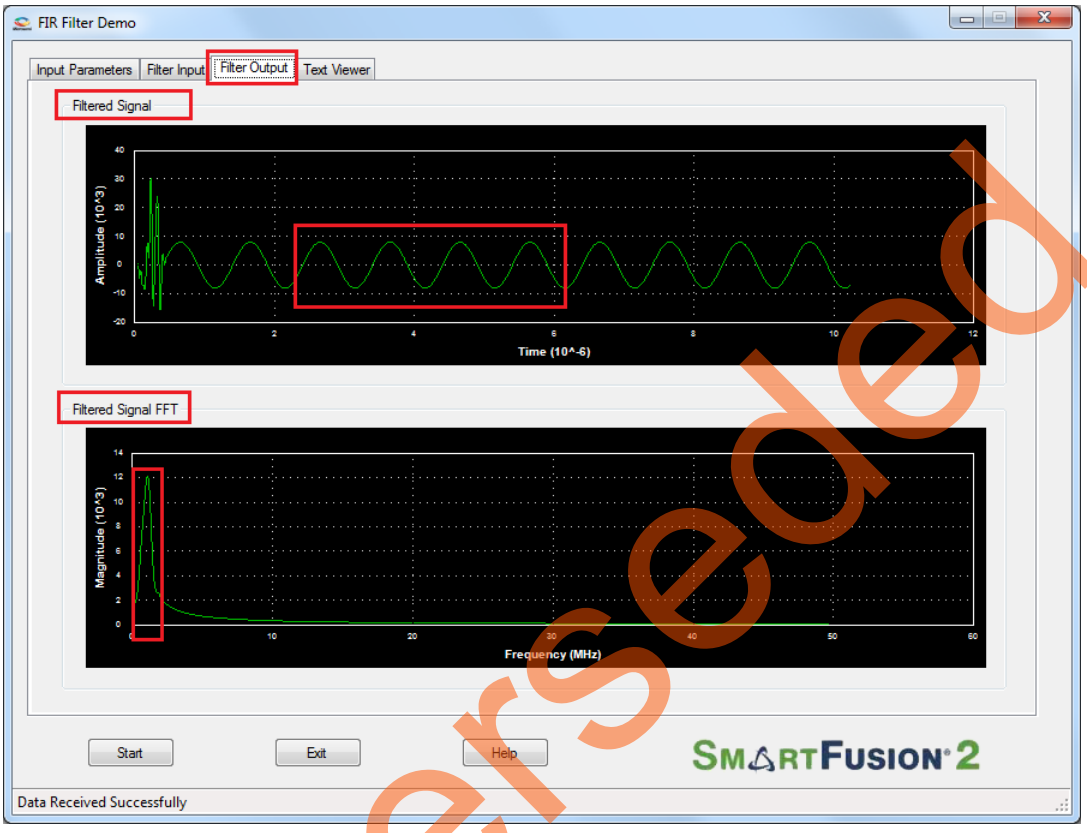

***Figure 17* • Filtered Signal: Time and Frequency Plot**

9. Right-click on the window, it shows different options. Refer to Figure 18. The data can be copied, saved, and exported to the CSV plot for analysis purpose. Page setup, print, show point values, zoom, and set scale are set to default.

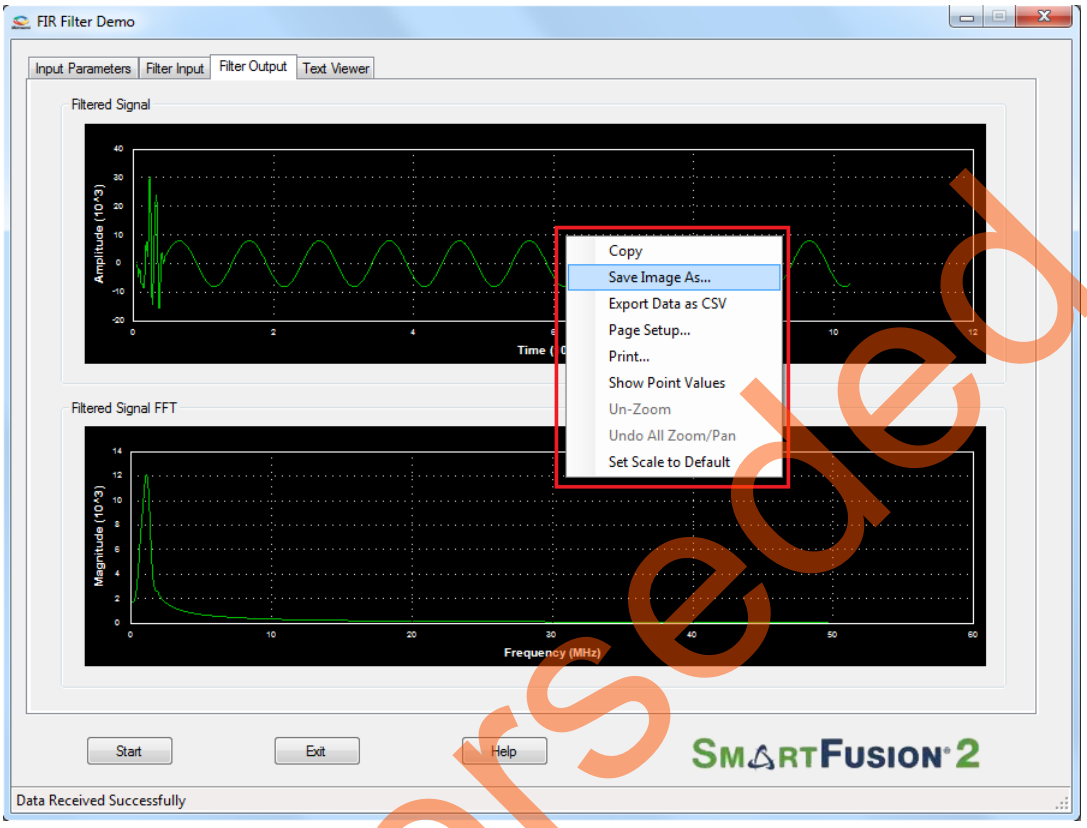

***Figure 18* • Filtered Signal: GUI options**

10. The filter coefficients, input signal, output signal, and FFT output data values can be viewed in **Text viewer**. Click on the **Text Viewer** tab and then click on the corresponding **View** button as shown in Figure 19.

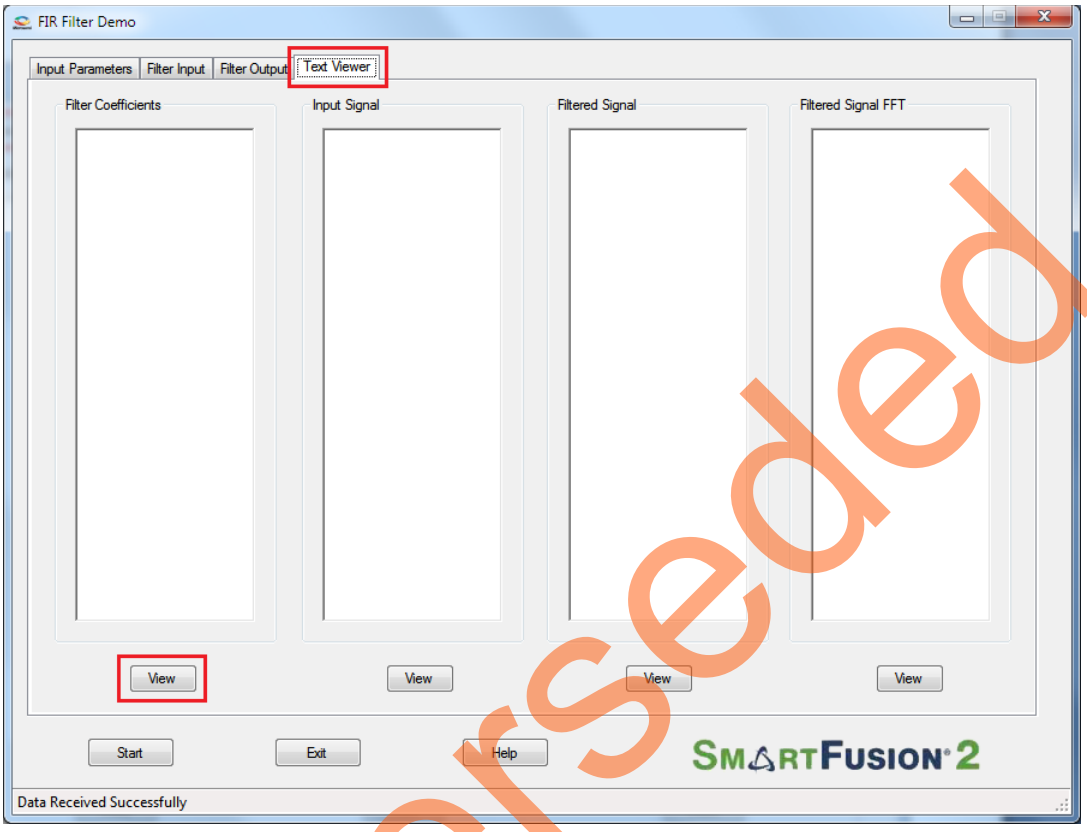

Figure 19 • **Text Viewer**

11. The values can be observed as shown in Figure 20.

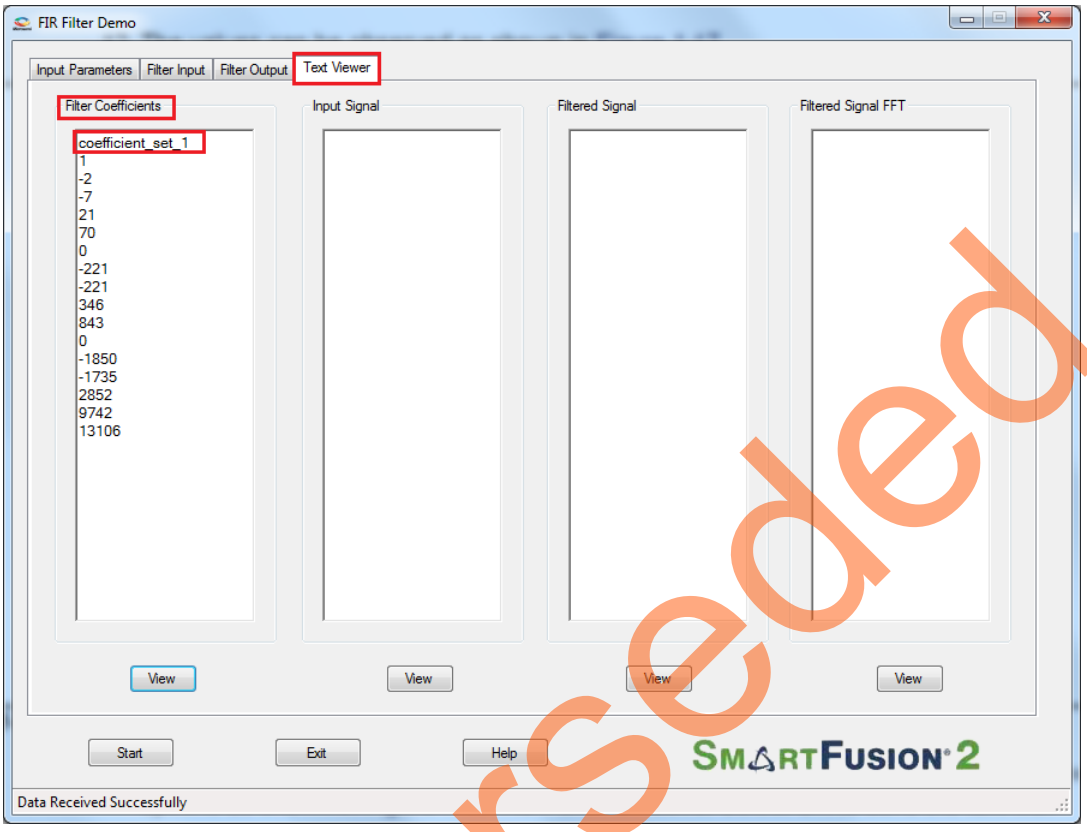

***Figure 20* • Text Viewer: Filter Coefficient Values**

12. To save the coefficients as a text file, right-click on the **Filter Coefficients** window, it shows different options, as shown in Figure 21. Now click on **Save**. Select **OK** to save the text file.

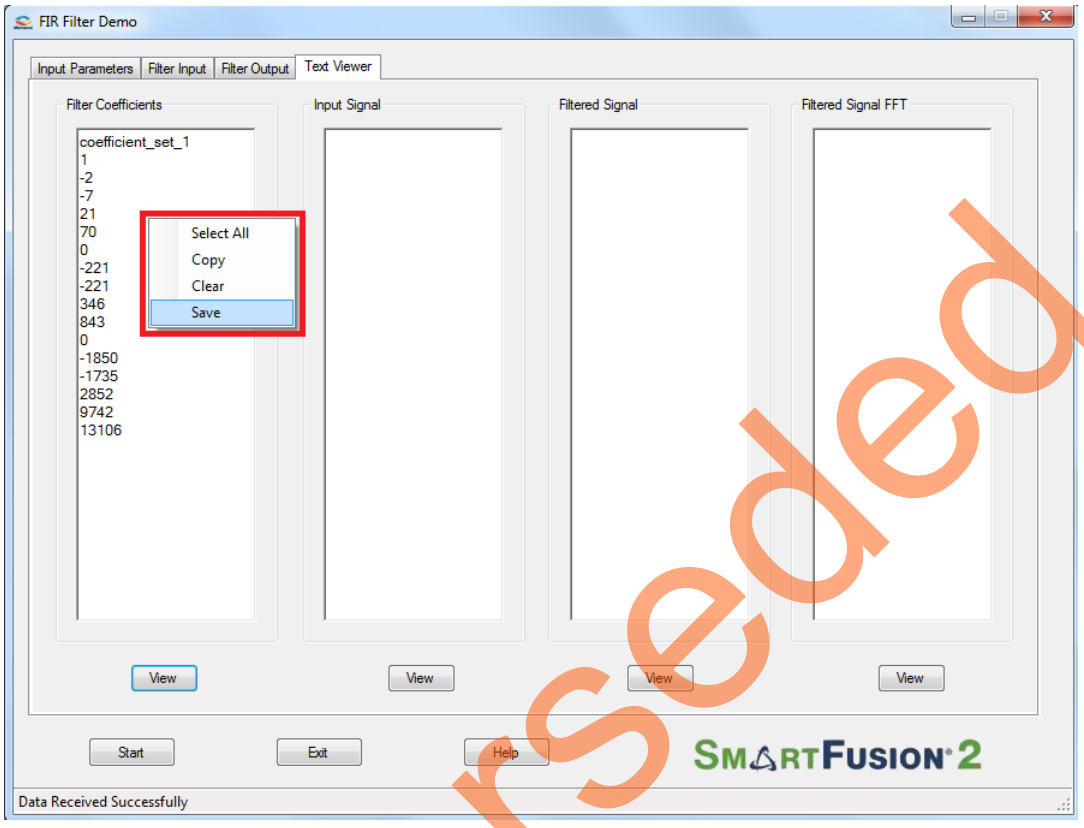

Figure 21 • **Text Viewer: Coefficients Save Options**

13. Click **Exit** to stop the demo. Refer to Figure 22.

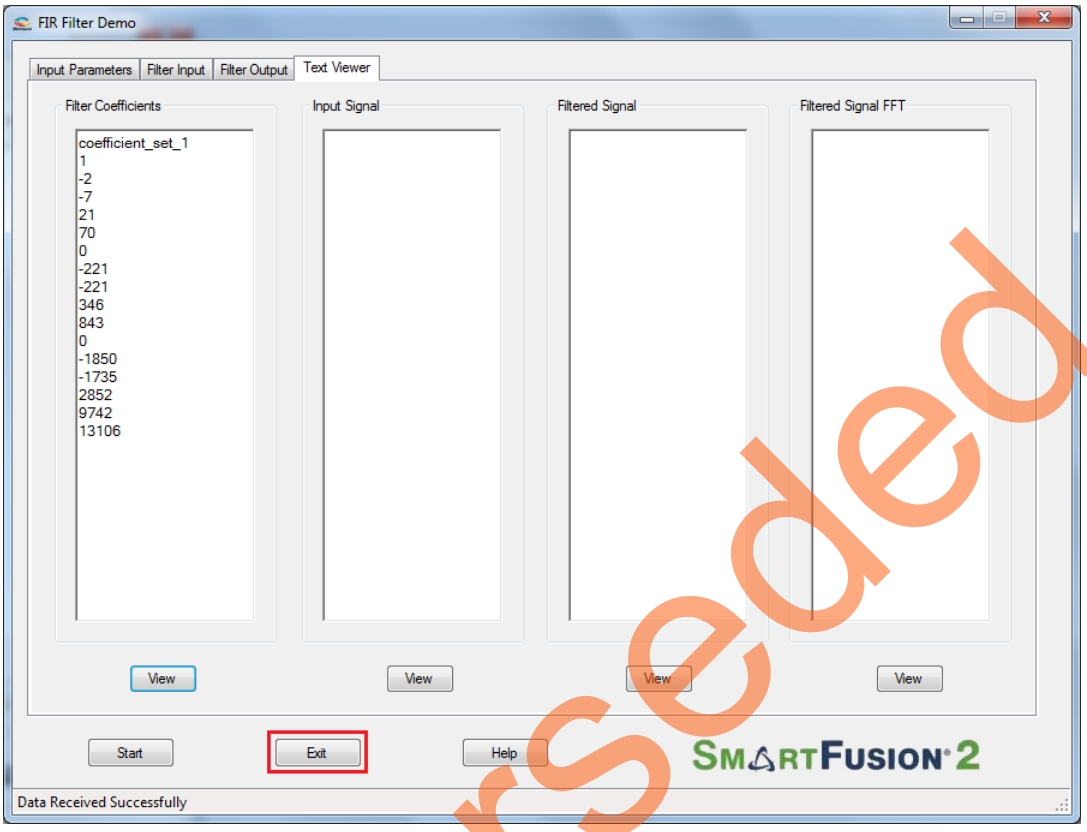

***Figure 22* • Exit Demo**

Conclusion

This demo shows the features of the SmartFusion2 device including MSS, Mathblocks, and LSRAMS for DSP specific applications. Also provides information about how to use the Microsemi DSP IP cores (CoreFIR, CoreFFT). This GUI-based demo is very easy to use and provides many options to understand and implement DSP filters on the SmartFusion2 device.

Appendix 1 - Smart Design Implementation

DSP FIR filter SmartDesign is shown in Figure 1.

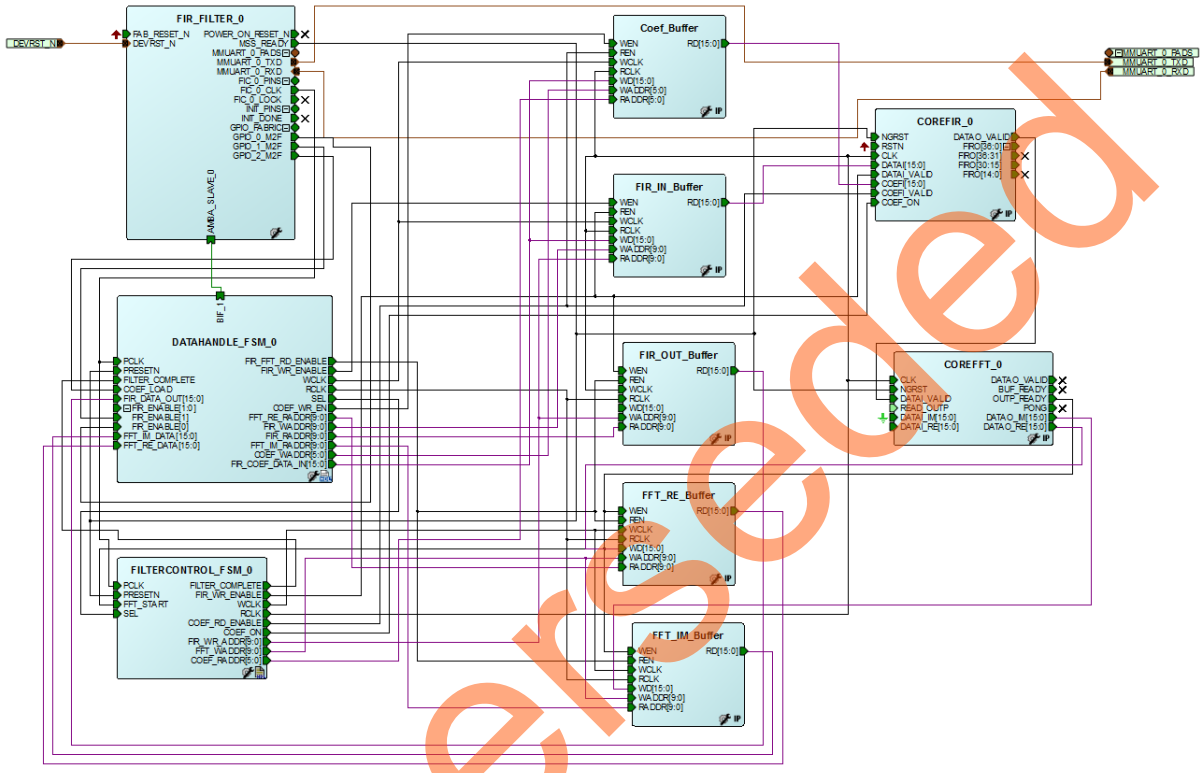

Figure 1 • **DSP FIR Filter Smart Design**

Table 1 describes SmartDesign blocks in DSP FIR Filter.

Table 1 • **DSP FIR Filter Demo Smart Design Blocks and Description**

S.No	Block Name	Description
1	FIR_FILTER_0	FIR_FILTER_0 is a System Builder generated component, in which MMUART is configured to handle the communication between the host PC and fabric logic. To generate a System Builder component, refer to the *SmartFusion2 System Builder User Guide*.
2	DATAHANDLE_FSM	Control logic to send/receive the data between MSS and data buffers.
3	FILTERCONTROL_FSM	Control logic to generate the control signals for FIR and FFT operations.
4	Coef_Buffer	TPSRAM IP for filter coefficient buffer
	FIR_IN_Buffer	TPSRAM IP for FIR input signal data buffer
	FIR_Out_Buffer	TPSRAM IP for FIR output signal buffer
	FFT_Im_Buffer	TPSRAM IP for FFT output imaginary data buffer
	FFT_Re_Buffer	TPSRAM IP for FFT output real data buffer

Table 1 • **DSP FIR Filter Demo Smart Design Blocks and Description (continued)**

S.No	Block Name	Description
5	COREFIR	COREFIR IP
6	COREFFT	COREFFT IP

Appendix 2 - Resource Usage Summary

Table 1 shows DSP FIR filter resource usage summary.

Device: SmartFusion2 device

Die: M2S010

Package: 484 FBGA

Table 1 • **DSP FIR Filter Demo Resource Usage Summary**

Type	Used	Total	Percentage
COMB	2651	12084	3.22
SEQ	3575	12084	5.49
RAM64x18	0	22	0.00
RAM1Kx18	12	21	17.39
MACC	20	22	50.00

Table 2 shows MACC blocks usage summary.

Table 2 • **MACC Blocks Usage Summary**

CoreFIR	CoreFFT	Total
16	04	20

Table 3 shows RAM1Kx18 blocks usage summary.

Table 3 • **RAM1Kx18 Blocks Usage Summary**

CoreFIR	CoreFFT	Fabric Buffers	Total
0	7	5	12

Appendix 3 - Coefficient Text File Format

The FIR filter coefficients can be loaded from an ASCII text file (*.txt). Create the coefficient file using a text editor. The format of text file should be as shown in Figure 1. Coefficient values must be entered as integer numbers. For a symmetric or anti-symmetric filter, only half of the coefficients must be listed in the file (applies to the Fully Enumerated type only). Only one coefficient value per line is permitted. An extra empty line must be placed after the last coefficient of the last set.

```
coefficient_set_1
5
6
10
25
63
- 1
- 11
- 32
- 63
```

***Figure 1* • Coefficient File Example - 9 Taps, Decimal Values**

A – List of Changes

The following table lists critical changes that were made in each revision of the chapter in the demo guide.

Date	Changes	Page
Revision 2 (July 2014)	Updated the document for Libero v11.3 software release (SAR 58923).	NA
	Updated the "Demo Design" section (SAR 58923).	6
	Updated the "Setting Up the Demo Design" section (SAR 58923).	9
Revision 1 (November 2013)	Updated the document for Libero v11.2 software release (SAR 52985).	NA
Revision 0 (April 2013)	Initial release	NA

B – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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