SmartFusion2 SoC FPGA Adaptive FIR Filter

Demo Guide

July 2014

Microsemi®

Revision History

Date	Revision	Change
1 July 2014	2	Third release
30 November 2013	1	Second release
22 May 2013	0	First release

Confidentiality Status

This is a non-confidential document.

Table of Contents

Preface

About this document

This demo is for SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) devices. It provides instructions on how to use the corresponding reference design.

Intended Audience

SmartFusion2 devices are used by:

- FPGA designers
- Embedded designers
- System-level designers

References

Microsemi Publications

- SmartFusion2 Programming User Guide
- SmartFusion2 System Controller User Guide
- SmartFusion2 Microcontroller Subsystem User Guide
- SmartFusion2/IGLOO2 Digital Signal Processing Reference Guide

See the following web page for a complete and up-to-date listing of SmartFusion2 device documentation: http://www.microsemi.com/products/fpga-soc/soc-fpga/sf2docs

SmartFusion2 SoC FPGA - Adaptive FIR Filter Demo

Introduction

The SmartFusion2 SoC FPGA devices integrate a fourth generation flash-based FPGA fabric and an ARM® Cortex™-M3 processor. The SmartFusion2 SoC FPGA fabric includes embedded mathblocks, which are optimized specifically for digital signal processing (DSP) applications such as, finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast fourier transform (FFT) functions.

Adaptive filter automatically adjusts the filter coefficients according to the underlying adaptive algorithm and the input signal characteristics. Due to its self adjustment of transfer function of an unknown system and computational requirements, adaptive filters are widely used in different areas of DSP application such as communication, biomedical instrumentation, audio processing, and video processing.

The least mean square (LMS) is a basic adaptive algorithm used in adaptive filters to update the filter coefficients. The LMS algorithm has advantages over other algorithms because of its simplicity, less computations and best performance in terms of the number of iterations required for convergence.

In this demo, an adaptive FIR filter application, the suppression of a narrow band signal interference on a wide band signal is implemented using an SmartFusion2 device. Refer to Figure 1.

The LMS algorithm is implemented in the FPGA fabric to adjust the filter weights/coefficients based on mean square error (MSE) approach. CoreFIR IP is used to perform the filtering operation and CoreFFT IP is used to generate the output spectrum to observe that the narrow band interfering signal component is suppressed. The host interface is implemented in microcontroller subsystem (MSS) to communicate with the Host PC. A user friendly `SF2_Adaptive_FIR_Filter.exe` generates input signals (narrow band signal and wide band signal), and also plots the input/output waveforms and the required spectrum.

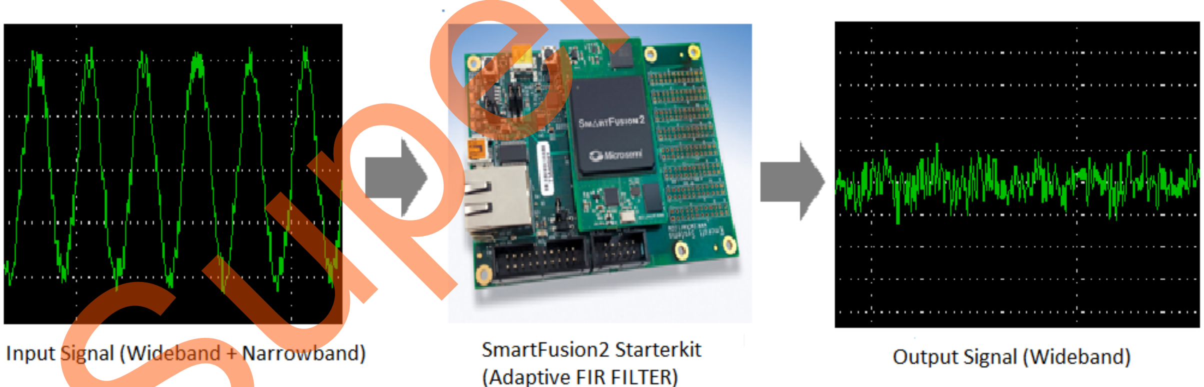

***Figure 1* • Narrowband Interference Cancellation**

Theory of Operation

Adaptive filters are mainly categorized into four basic architectures:

- System identification
- Noise cancellation
- Linear prediction
- Inverse modeling

In this demo, linear prediction architecture is used to implement adaptive filter. The LMS algorithm uses a gradient search technique to determine the filter coefficients that minimize the mean square prediction error. The estimate of the gradient is based on the sample values of the tap-input vector and the error signal. The algorithm iterates over each coefficient in the filter, moving it in the direction of the approximated gradient. After reaching the optimal filter coefficients, the error signal e(n) consists of the Wideband signal. Figure 2 shows the linear prediction based adaptive filter architecture.

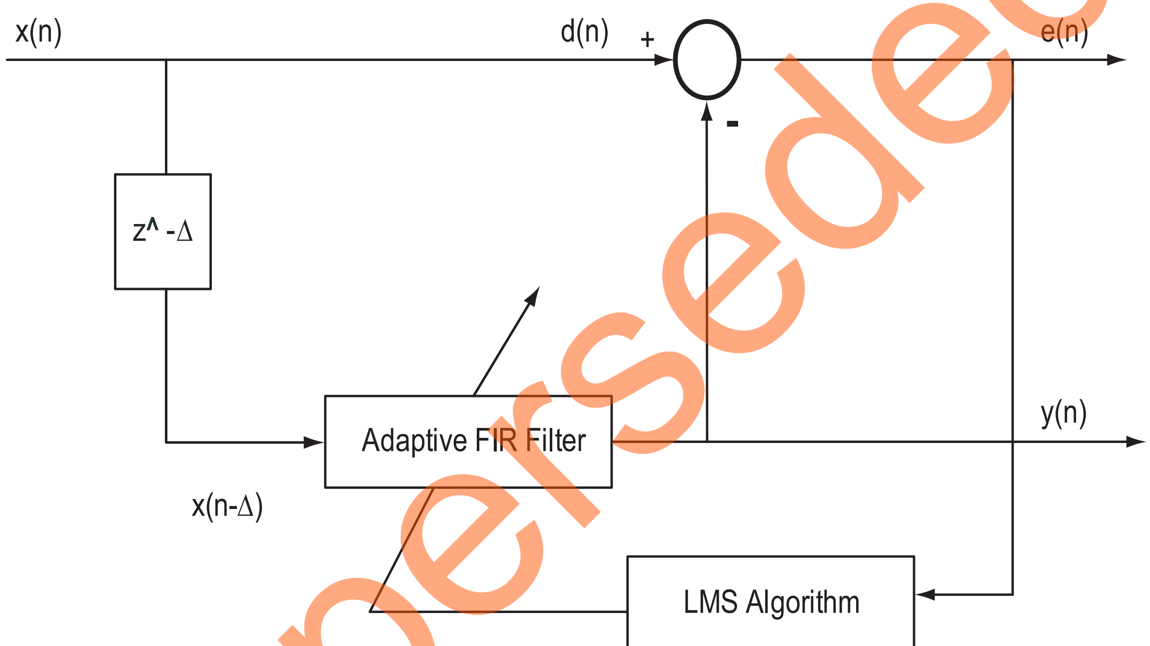

***Figure 2* • Linear Prediction Adaptive Filter Architecture**

The input signal x(n) consists of a desired wideband signal corrupted by a narrow band signals that are not required, refer to Figure 3 on page 8. In a linear prediction architecture, the desired signal d(n) is same as the input signal x(n) and delayed input x(n-Δ) is fed to the adaptive filter as shown in Figure 2. The delay factor Δ (delta) de-correlates the wideband component and correlates the narrow band component of the desired signal d(n) with the delayed input signal x(n-Δ).

The adaptive filter tries to estimate the narrow band component y(n), and forms an equivalent transfer function, which is similar to that of narrow band filters centered at the frequencies of the narrow band components of the input signal. At the summing junction, the filtered input signal subtracting with delayed input signal produces an error signal. The error signal is used by the LMS algorithm to adjust the filter coefficients. After some iterations, the Error signal converges to a wide band component. The following equations describe computing the coefficients using LMS algorithm.

$$y(n) = \sum_{k=0}^{k=l-1} h(n) \times x(n - \Delta - k)$$

EQ 1-1

where,

According to EQ 1-1, narrowband component y(n), is the adaptive filter output

h(n) is the filter weights/coefficients

x(n-Δ) is the input signal to adaptive filter

l is length of the filter (number of taps)

k is the index variable.

The error is computed using the following equation:

$$e(n) = d(n) - y(n)$$

EQ 1-2

where,

e(n) is the error signal

d(n) is desired signal

The filter weights/coefficients are updated using the following equation:

$$h(n+1) = h(n) + \mu * e(n) * x(n-\Delta)$$

EQ 1-3

where,

h(n+1) is the estimated filter weights

h(n) is present filter weights

μ is the step size factor

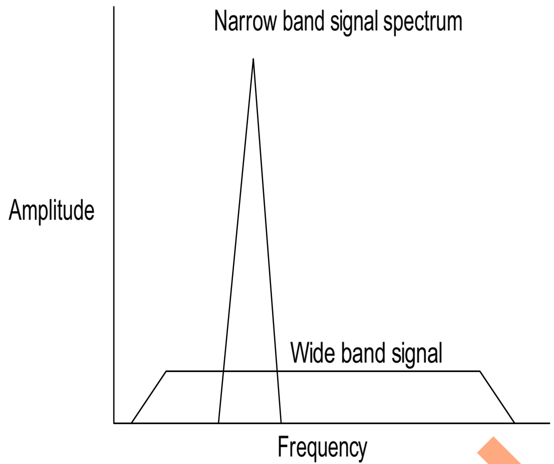

***Figure 3* • Input Spectrum of Narrow Band Signal + Wide Band Signal**

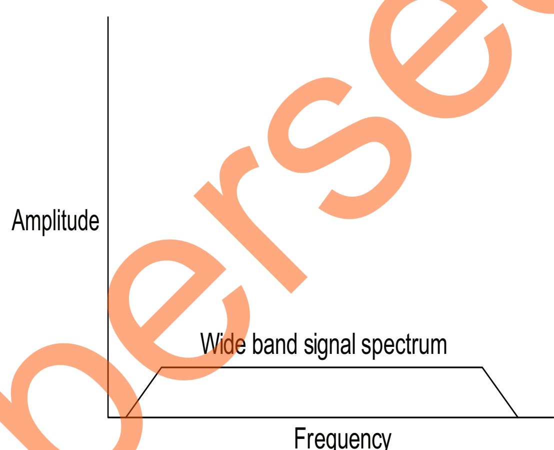

***Figure 4* • Output Spectrum of Wide Band Signal**

Design Requirements

Table 1 • **Design Requirements**

Design Requirements	Description
Hardware Requirements	
SmartFusion2 Starter Kit • FlashPro4 programmer • USB A to Mini-B cable	SF2-484-STARTER-KIT
Host PC or Laptop	Windows 7 64-bit Operating System
Software Requirements	
Libero® System-on-Chip (SoC)	11.3
FlashPro Programming Software	11.3
Host PC Drivers	USB to UART drivers
Framework	Microsoft .NET Framework 4 Client for launching demo GUI

Demo Design

Introduction

The design files are available for download from the following path in the Microsemi® website:
http://soc.microsemi.com/download/rsc/?f=SmartFusion2_Adaptive_FIR_Filter_Demo_DF

Design files include:

1. Design files
2. Programming files
3. GUI executable
4. Readme file

Figure 5 shows the top-level structure of the design files. For further details, refer to the `readme.txt` file.

```
<download_folder>
  |
  └── sf2_adaptive_fir_filter_demo_df
        ├── Design_files
        ├── GUI
        ├── programming_file
        └── readme.txt
```

Figure 5 **• Demo Design Files Top-Level Structure**

Demo Design Description

This demo design uses the following blocks:

- MSS block
- Control logic (user RTL)
- LMS_FIR_TOP (Smart Design)
- TPSRAM (IPcore)
- CoreFFT (IPcore)

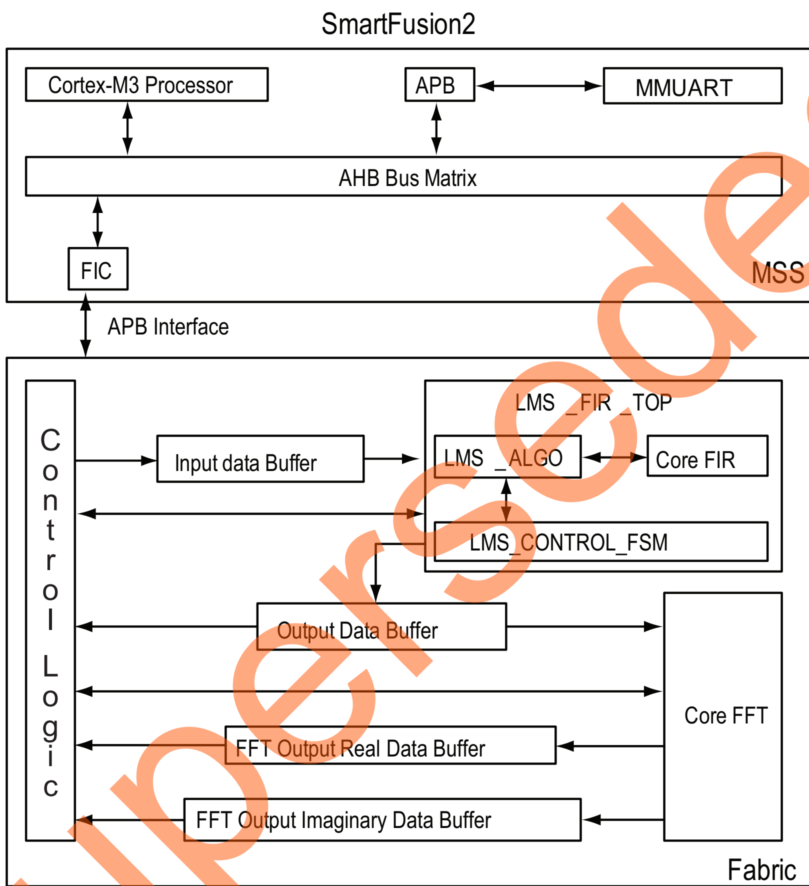

Figure 6 • **Adaptive FIR Filter Demo Block Diagram**

MSS Block

The MSS block sends and receives the data between the Host PC (GUI interface) and FPGA fabric logic. The MMUART interface is used to communicate with the Host PC. FIC_0 interface (APB master) is used to communicate with the fabric user logic.

Control Logic

This is the user logic that is implemented in the fabric and consists of the following two finite-state machines (FSM)s:

- **Data Handling**: Implements and controls operations like loading the filter input data to the corresponding input data buffer, reading of processed data, and FFT data values. An APB bus slave is implemented to communicate with the MSS APB master.
- **Filter Control**: Controls the FIR filter and FFT operations. Loads the filtered data to the corresponding output buffer and moves the FFT output data to the corresponding output data buffer.

LMS_FIR_TOP

This is a SmartDesign block implemented in the fabric.It consists of the following blocks:

- **LMS_CONTROL_FSM**: This FSM is implemented in the RTL to provide the control signals to the LMS_ALGO block.
- **LMS_ALGO**: This LMS algorithm is implemented in the RTL to compute the error signal, correction factor, filter coefficients, and to send the filter coefficients to the Core FIR filter.
- **CoreFIR**: CoreFIR IP is used in the Reloadable Coefficient mode to configure its coefficients on the fly. CoreFIR IP configuration is as follows:
  – Version: 8.5.104
  – Filter Type: Single rate fully enumerated
  – No of taps: 16
  – Coefficients type: Reloadable
  – Coefficients bit width: 16 (signed)
  – Data bit width: 16 (signed)
  – Filter structure: Transposed with no symmetry

TPSRAM IP

TPSRAM IP uses the following configurations:

- Input signal data buffer (depth: 1024, width: 16)
- Output signal buffer (depth: 1024, width: 16)
- Output signal FFT real data buffer (depth: 1024, width: 16)
- Output signal FFT imaginary data buffer (depth: 1024, width: 16)

CoreFFT

CoreFFT IP is used to generate the frequency spectrum of the filtered data. CoreFFT IP configuration is as follows:

- Version: 6.3.102
- FFT Architecture: In place
- FFT type: Forward
- FFT Scaling: Conditional
- FFT Transform Size: 256
- Width: 16

For detailed SmartDesign implementation and resource usage summary, refer to "Appendix 1: SmartDesign Implementation" on page 28.

Setting Up the Demo Design

The following steps describe how to setup the hardware demo:

1. Connect the jumpers on the SmartFusion Starter Kit board as shown in Table 2.

Table 2 • **SmartFusion2 Starter Kit Jumper Settings**

Jumper	Configuration	Comments
JP1	1-2 Closed, 3-4 Open	Enable power on the M2S-FG484 SOM (VCC3)
JP2	1-2 Open, 3-4 Closed	Select appropriate JTAG mode and enable power to the SmartFusion2 JTAG controller.
JP3	1-3 Open, 2-4 Closed	Use the mini-USB port as the power source

2. Connect the FlashPro4 programmer to the P5 connector of the SmartFusion2 Starter Kit board.
3. Connect the Host PC USB port to the P1 Mini USB connector on the SmartFusion2 Starter Kit board using the USB Mini-B cable.

   Figure 7 shows the board setup for running the Adaptive FIR filter demo on the SmartFusion2 Starter Kit.

Figure 7 • **SmartFusion2 SoC FPGA Starter Kit Setup**

4. Ensure that the USB to UART bridge drivers are automatically detected. This can be verified in the **Device Manager** of the Host PC.

Figure 8 shows the USB Serial port.

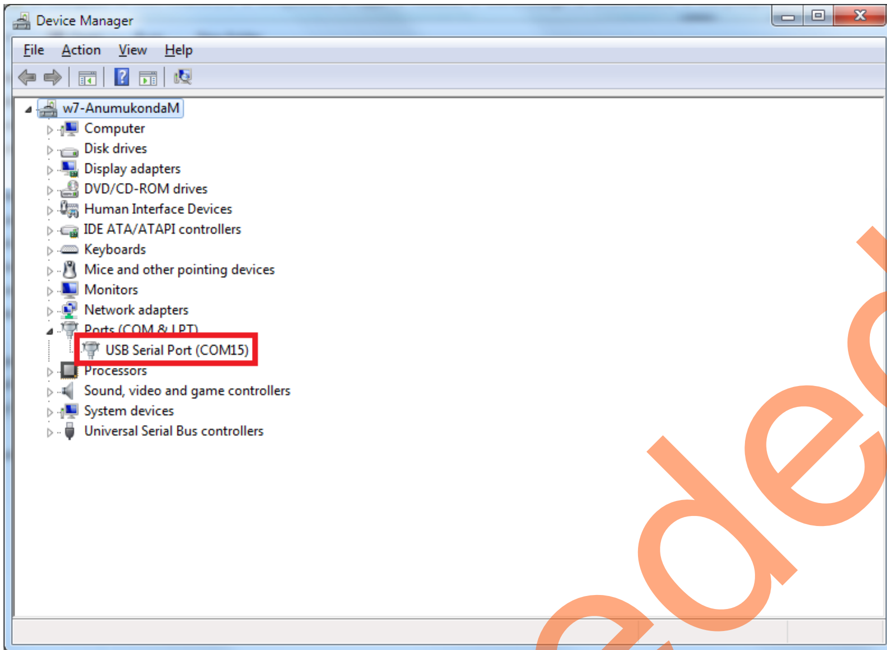

***Figure 8* • USB to UART Bridge Drivers**

5. If USB to UART bridge drivers are not installed, download and install the drivers from: www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip.

Programming the Demo Design

The following steps describe how to program the demo design:

1. Download the demo design from: http://soc.microsemi.com/download/rsc/?f=SmartFusion2_Adaptive_FIR_Filter_Demo_DF
2. Launch the FlashPro software.
3. Click **New Project**.

4. In the **New Project** window, type the project name as SF2_Adaptive_Filter.

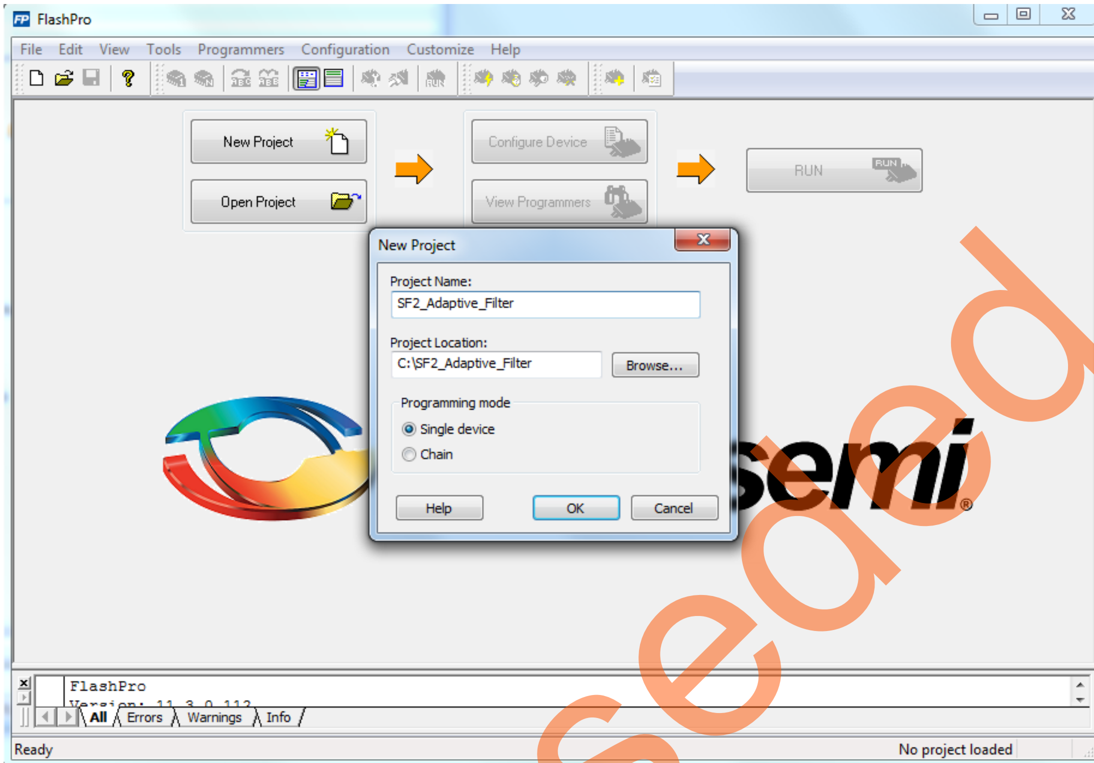

Figure 9 **• FlashPro - New Project**

5. Click **Browse** and navigate to the location where you want to save the project.
6. Select **Single device** as the **Programming mode**.
7. Click **OK** to save the project.

Setting Up the Device

The following steps describe how to configure the device:

1. Click **Configure Device** on the FlashPro GUI.
2. Click **Browse** and navigate to the location where the `Adaptive_FIR_top.stp` file is located and select the file. The default location is: *<download_folder>\Adaptive_FIR_filter_Demo_DF\ProgrammingFiiles\Adaptive_FIR_top.stp*.
3. Click **Open**. The required programming file is selected and is ready to be programmed in the device.

Programming the Device

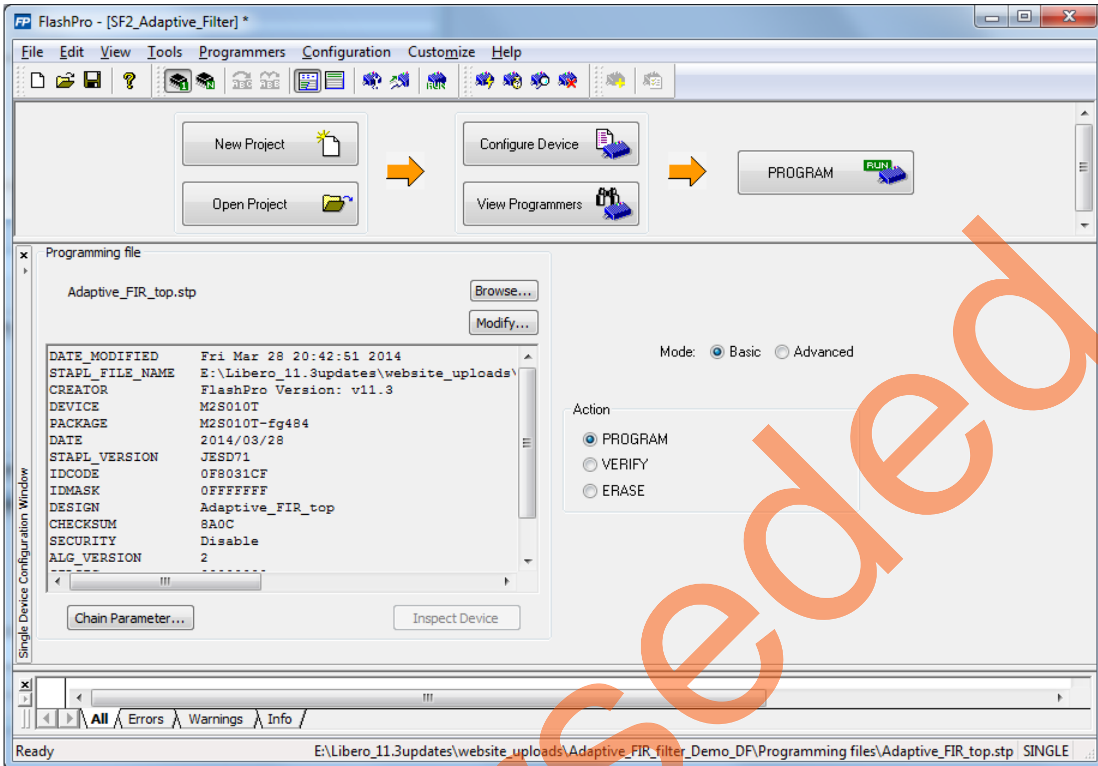

***Figure 10* • FlashPro Project Configured**

The following steps describe how to program the device:

1. Click **PROGRAM** to start programming the device. Wait until you get a message indicating that the **RUN PASSED**.

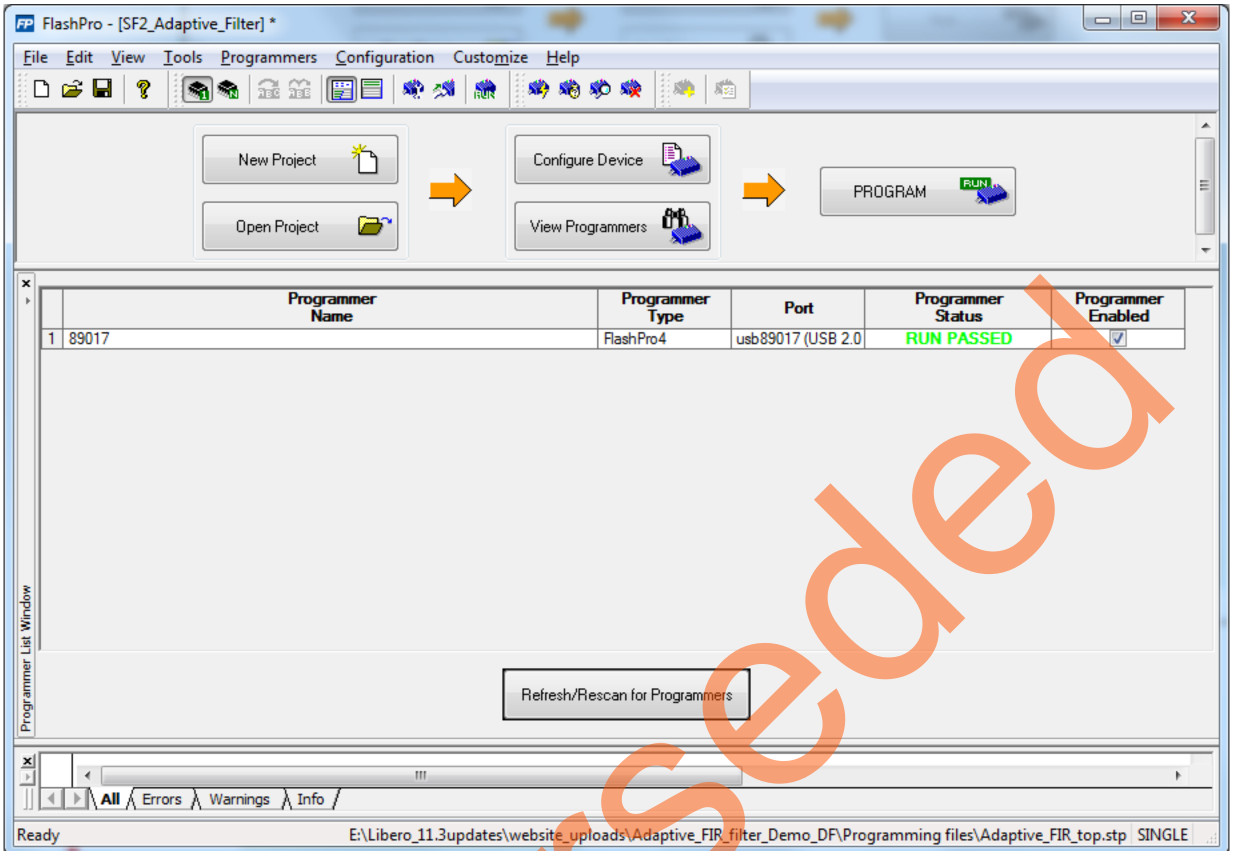

Figure 11 **• FlashPro Project RUN Passed**

Adaptive FIR Filter Demo GUI

The adaptive FIR filter demo is provided with a user-friendly GUI that runs on the Host PC and communicates with the SmartFusion2 Starter Kit. The UART is used as the underlying communication protocol between the Host PC and the SmartFusion2 Starter Kit. Figure 12 shows the Adaptive FIR Filter demo GUI.

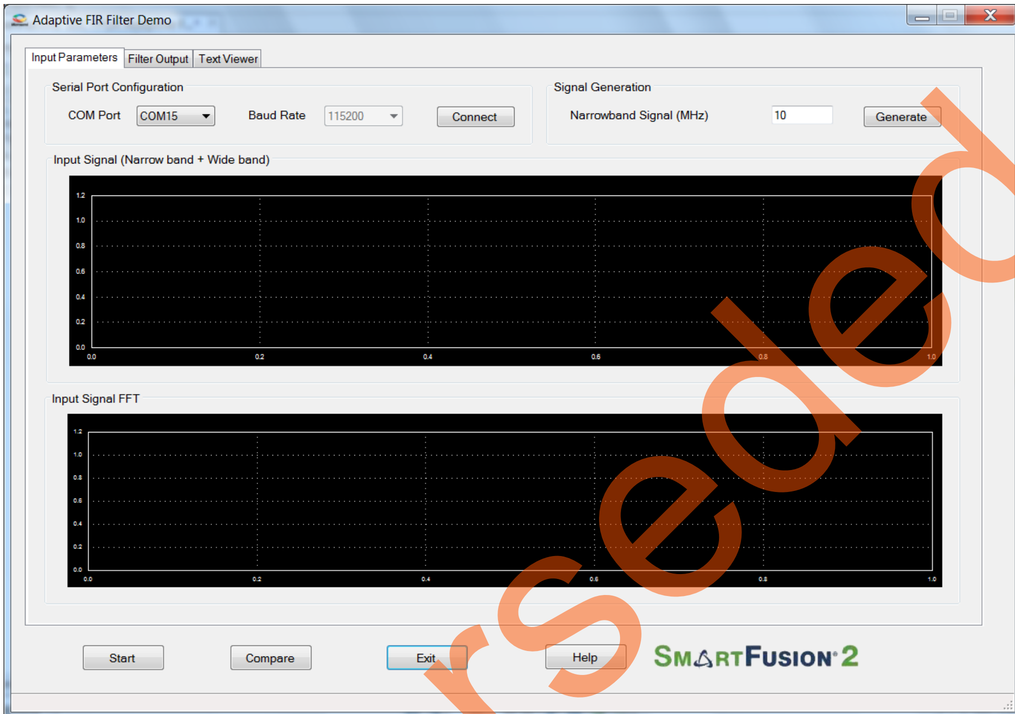

***Figure 12* • Adaptive FIR Filter Demo GUI**

The Adaptive FIR filter demo window consists of the following tabs:

- **Input Parameters**: Configures the serial COM port, filter generation, and signal generation.
- **Filter Output**: Plots Error signal and its frequency spectrum
- **Text Viewer**: Shows the coefficients, input signal, output signal, and FFT data values

Click **Help** for more information on the GUI.

Running the Design

1. Launch the adaptive FIR filter demo GUI, install and invoke the executable file provided with the design files. (*\\SF2_Adaptive_FIR_Filter_Demo\GUI\SF2_Adaptive_FIR_Filter.exe*). The Adaptive FIR Filter Demo window is displayed, refer to Figure 13 on page 18.

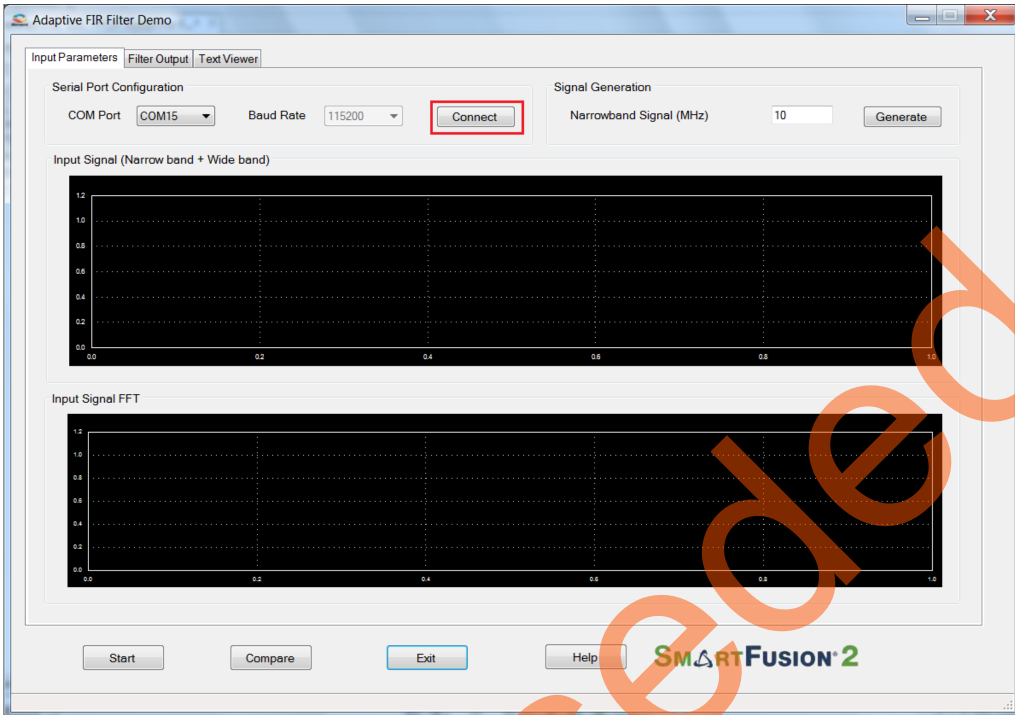

Figure 13 **• Serial Port Configuration**

2. **Serial Port Configuration**: The COM port number is automatically detected and baud rate is fixed at 115200. Press **Connect**. Refer to Figure 13.
3. **Signal Generation**: Enter the narrowband signal frequency as 2 MHz (supported range is 1 MHz to 20 MHz), and click **Generate**. Refer to Figure 14 on page 19.

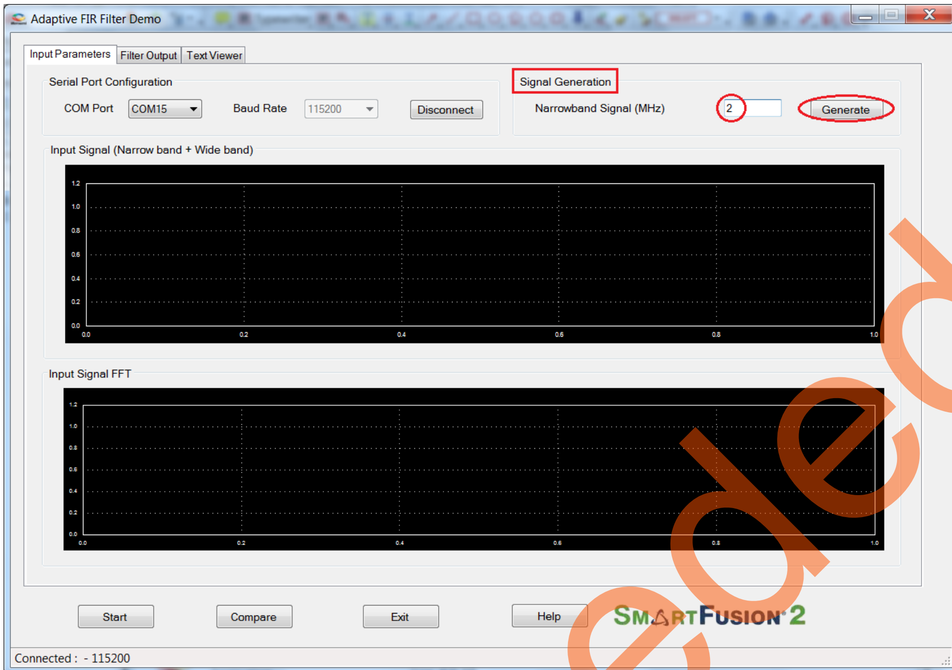

Figure 14 **• Signal Generation**

Adaptive FIR Filter Demo adds the wide band signal (generated inside the Adaptive FIR Filter Demo window) to the narrow band signal component and plots the combined signal (Narrowband and Wide band), FFT spectrum. Refer to Figure 15.

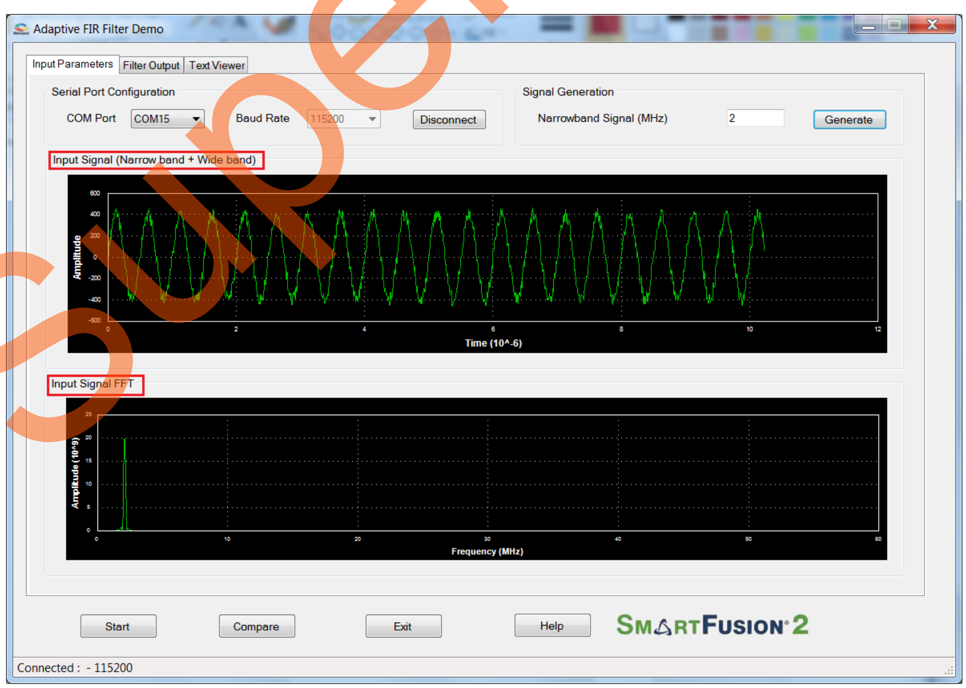

Figure 15 **• Signal Generation**

4. Click **Start**(, to load the input data (1K samples) to the SmartFusion2 device for processing the filtering operation, refer to Figure 16.

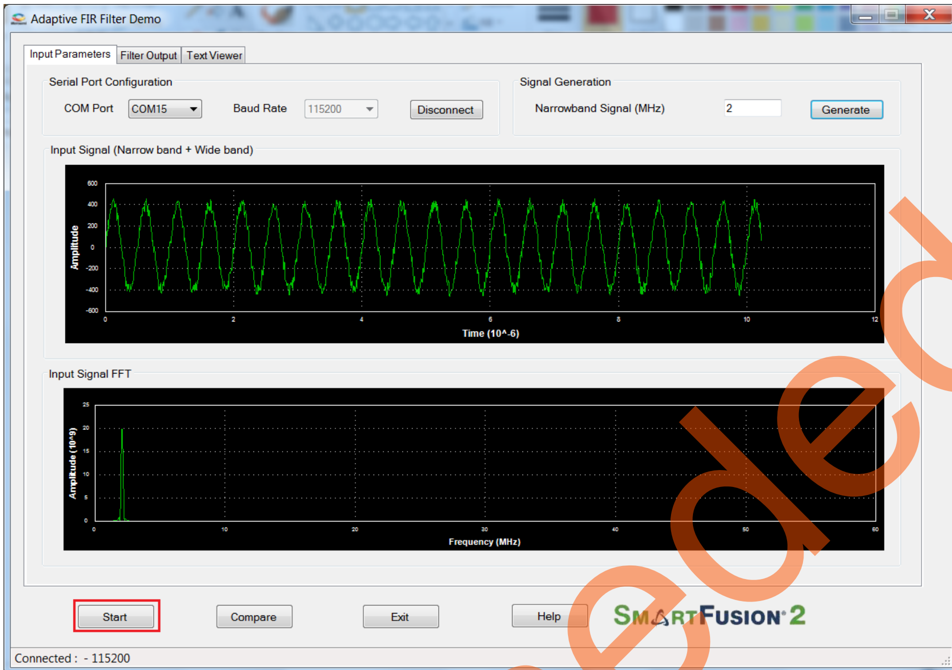

Figure 16 **• Adaptive FIR Filter Demo Start**

5. After completing the filter operation, the GUI receives the error data and its FFT data from the SmartFusion2 device and plots as shown in Figure 17 on page 21. The error signal plot shows the suppression of narrow band component from the wide band signal only after the required number of iterations.

Figure 17 **• Error Signal: Time and Frequency Plot**

The narrow band signal component is suppressed gradually in the Error signal frequency spectrum. This can be observed in the Error signal FFT plot as shown in Figure 18.

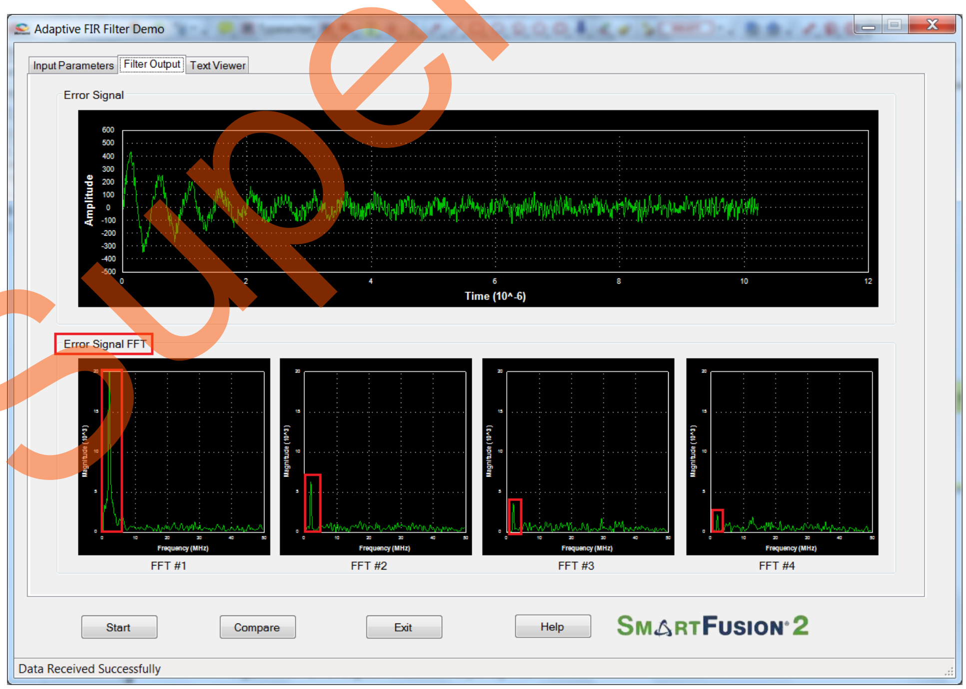

Figure 18 **• Error Signal: Time and Frequency Plot**

6. You can compare the input wide band and the output wide band signals. Click **Compare** to analyze the Input wide band data with the Output wide band data.

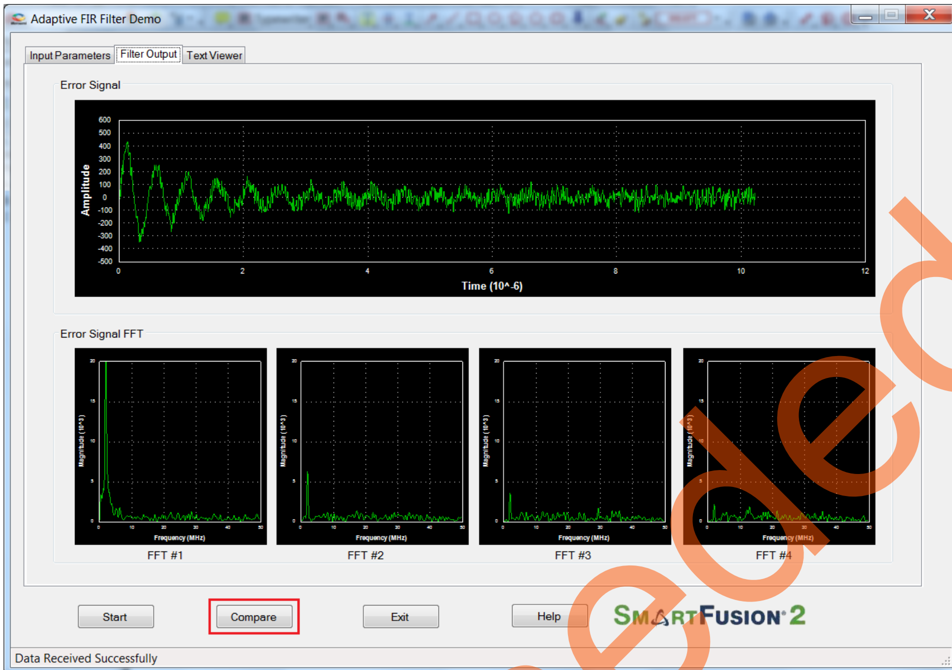

***Figure 19* • Compare Error Signal: Time and Frequency Plot**

7. A window displaying the comparison between the Input wide band and Output wide band is displayed, refer to Figure 20.

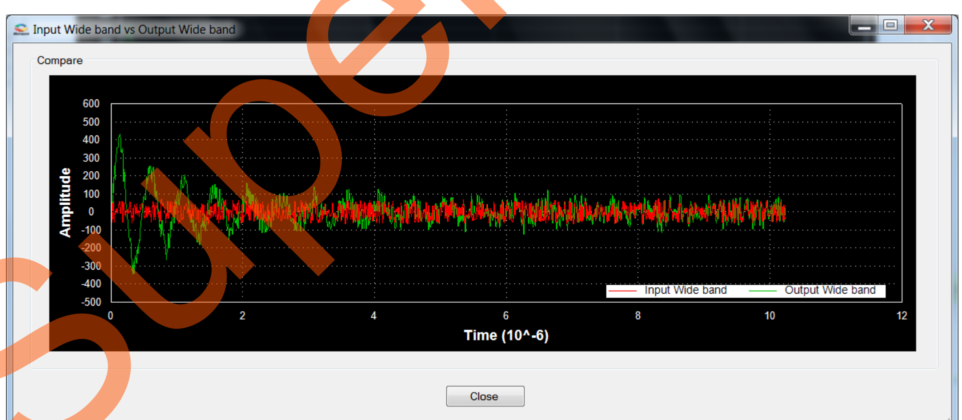

***Figure 20* • Comparison of Input Wide Band and Output Wide Band**

8. The plot can be zoomed in for comparison, refer to Figure 21.

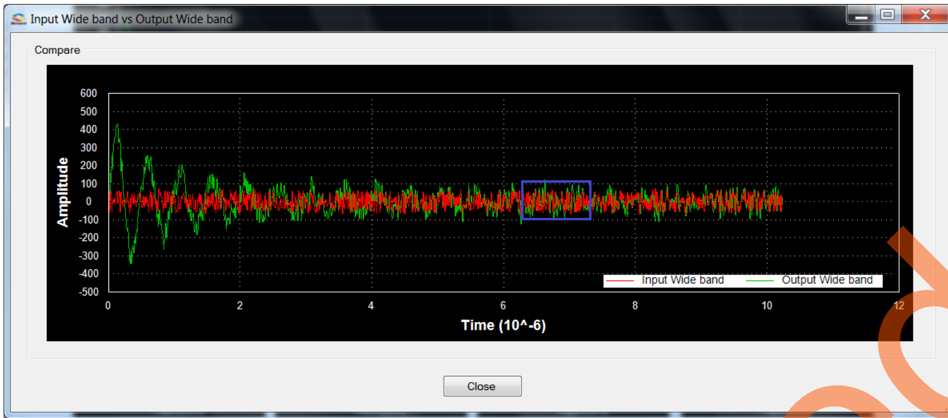

Figure 21 **• Input Wide Band vs Output Wide Band**

9. Compare the Error signal (output wide band signal) with the input wide band signal, refer to Figure 22. You can see that the narrow band interfering component is eliminated and the wide band signal is preserved in Error signal.

Figure 22 **• Comparison of Input Wide Band and Output Wide Band**

10. Click **Close**, refer to Figure 23.

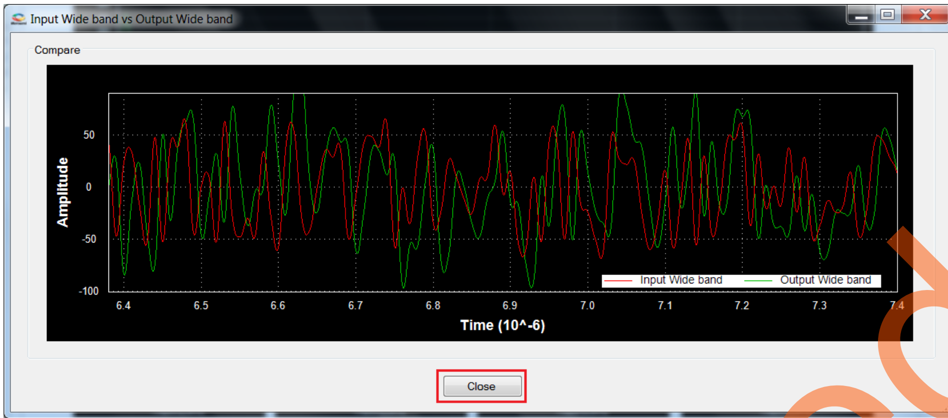

Figure 23 **• Closing Input Wide Band vs Output Wide Band**

11. You can copy, save, export and customize page and configure print setup the Error Signal plot. Right-click on the **Error Signal** plot.
12. From the context sensitive pop-up select the required option.
13. It shows the different options as shown in Figure 24. The data can be copied, saved, and exported to CSV plot for analysis purpose. Page setup, print, show point values, Zoom, and set scale to default.

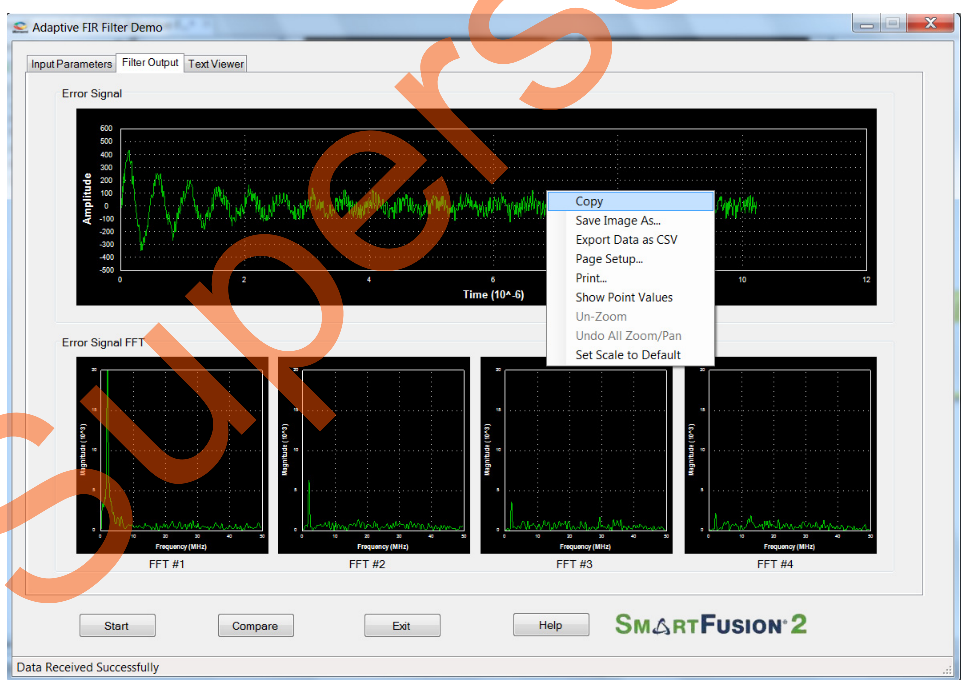

Figure 24 **• Error Signal - GUI Options**

14. The input signal and error signal values can be viewed in the **Text Viewer** tab. Click on the **Text Viewer** tab and then click on the corresponding **View** shown in Figure 25.

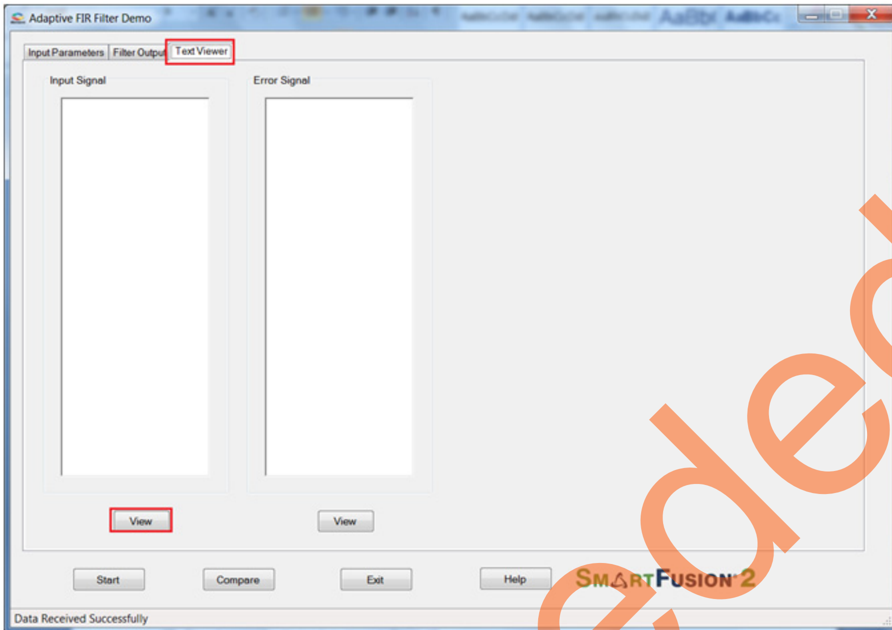

Figure 25 **• Text Viewer**

15. Figure 26 shows the **Text Viewer** tab showing the **Input Signal** values.

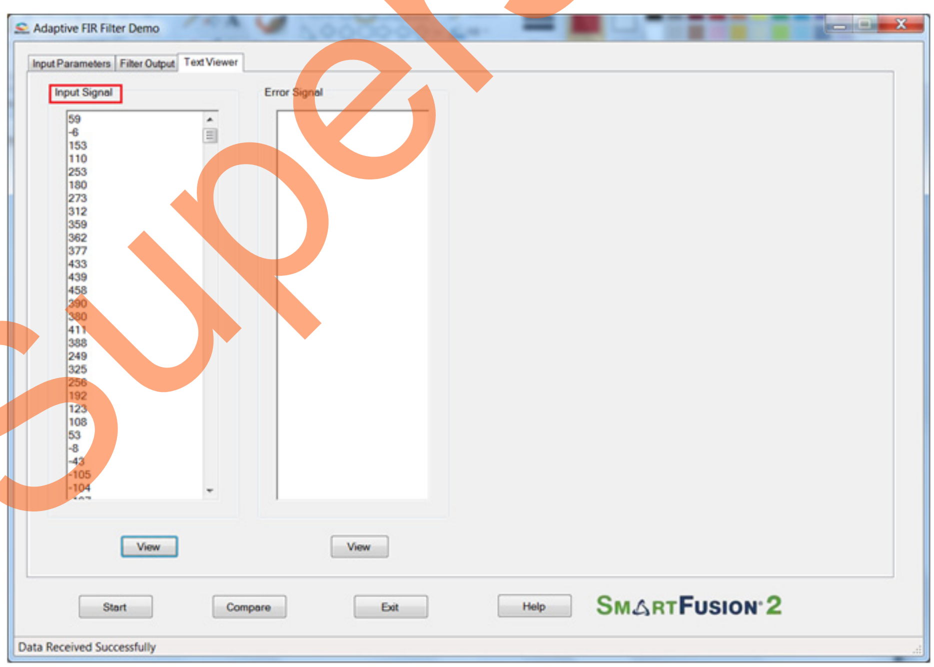

Figure 26 **• Text Viewer: Input Signal Values**

16. To save the Input Signal as a text file, right-click on the Input Signal window. The Input Signal window displays different options as shown in Figure 27.
17. Click **Save**. Select **OK** to save the text file.

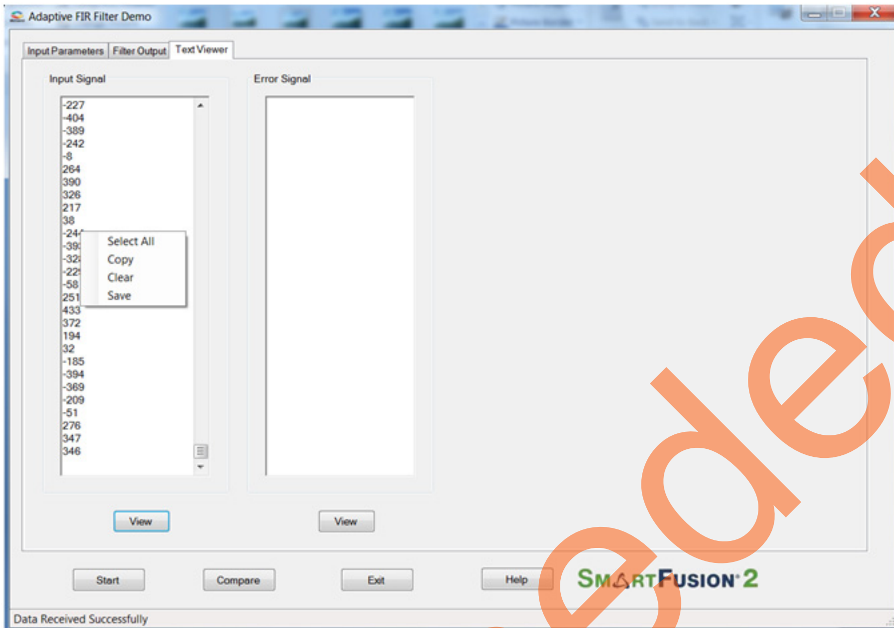

***Figure 27* • Text Viewer - Coefficients Save Options**

18. Click **Exit** to stop the demo, refer to Figure 28.

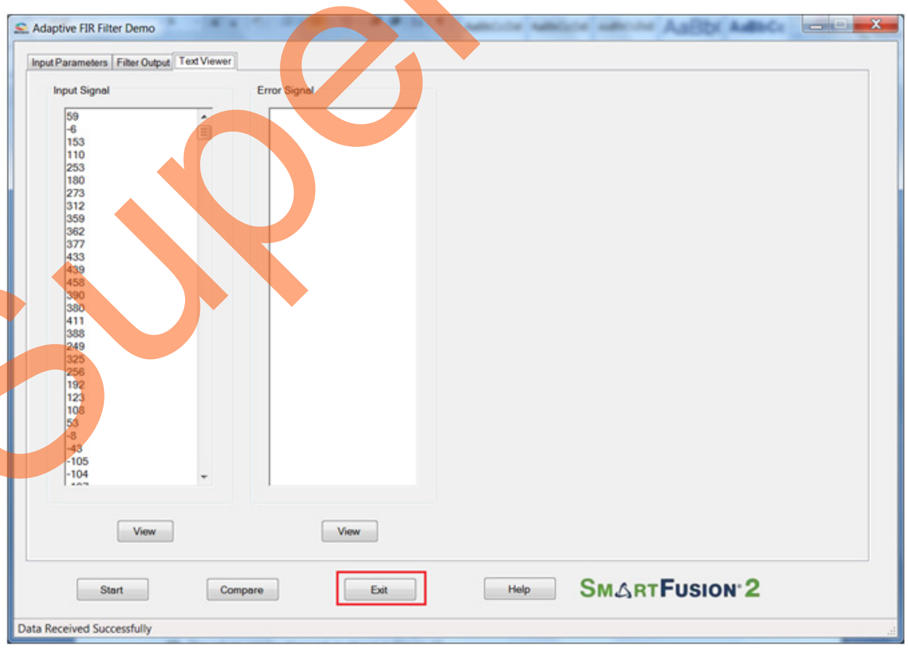

***Figure 28* • Exit Demo**

Conclusion

This demo provides information about the features of the SmartFusion2 device including mathblocks and how to use Microsemi IPs (CoreFIR and CoreFFT) or narrow band interference cancellation application using Adaptive filters. This Adaptive FIR Filter based-demo is easy to use and provides many options to understand and implement DSP filters on the SmartFusion2 device.

Appendix 1: SmartDesign Implementation

Adaptive FIR filter SmartDesign is shown in Figure 1.

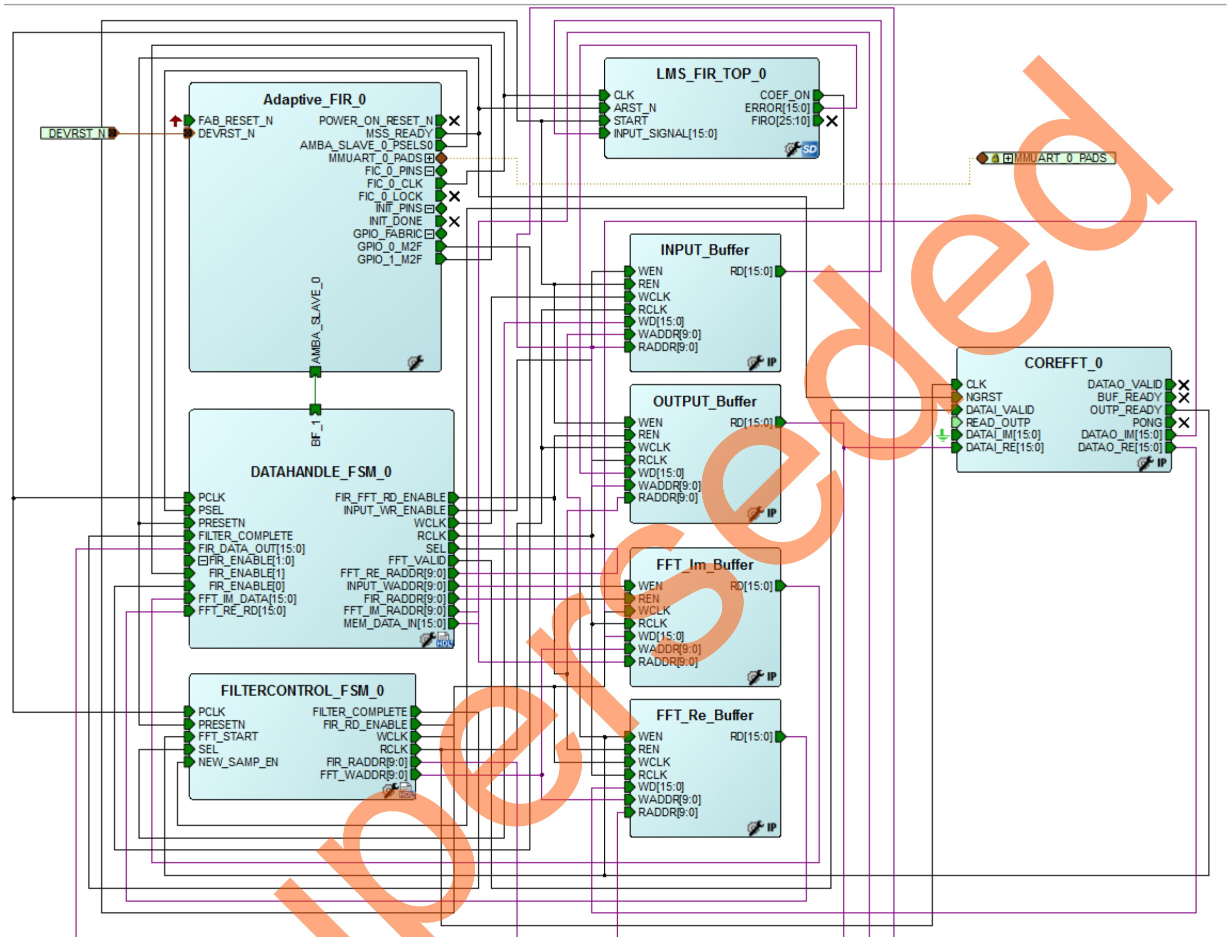

***Figure 1 •* Adaptive FIR Filter SmartDesign**

SmartDesign LMS_FIR_TOP is shown in Figure 2.

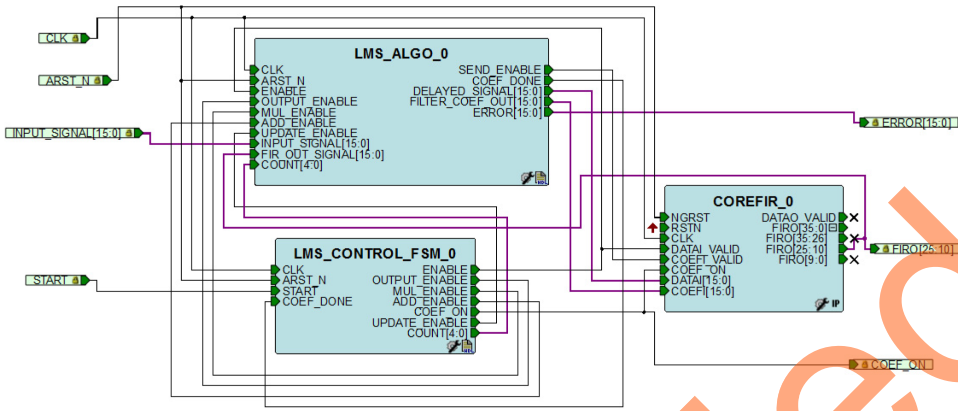

Figure 2 • **LMS_FIR_TOP Smart Design**

Table 1 describes SmartDesign blocks in Adaptive FIR Filter.

Table 1 • **Adaptive FIR Filter Demo Smart Design Blocks and Description**

S.No	Block Name	Description
1	Adaptive_FIR	FIR_FILTER_0 is a System Builder generated component, in which MMUART is configured to handle the communication between the host PC and fabric logic. To generate a System Builder component, refer to the *SmartFusion2 System Builder User Guide*.
2	DATAHANDLE_FSM	Control logic to send/receive the data between MSS and data buffers
3	FILTERCONTROL_FSM	Control logic to generate the control signals for FIR and FFT operations
4	LMS_FIR_TOP	SmartDesign
5	INPUT_Buffer	FIR input signal data buffer
	OUTPUT_Buffer	FIR output signal buffer
	FFT_Im_Buffer	FFT output imaginary data buffer
	FFT_Re_Buffer	FFT output real data buffer
6	COREFFT	COREFFT IP

Table 2 describes SmartDesign blocks in LMS_FIR_TOP.

Table 2 • **LMS_FIR_TOP Smart Design Blocks and Description**

S.No	Block Name	Description
1	LMS_ALGO	LMS algorithm implemented in RTL to compute error, correction factor, and filter coefficients.
2	LMS_CONTROL_FSM	FSM implemented in RTL to control LMS_ALGO block
3	COREFIR	COREFIR IP

Appendix 2: Resource Usage Summary

Table 1 shows adaptive FIR filter demo resource usage summary.

Device: SmartFusion2 device

Die: M2S010

Package: 484 FBGA

Table 1 • **Adaptive FIR Filter Demo Resource Usage Summary**

Type	Used	Total	Percentage
COMB	2727	12084	4.87
SEQ	2832	12084	5.38
RAM64x18	0	22	2.78
RAM1Kx18	11	21	17.39
MACC	13	22	29.17

Table 2 shows MACC blocks usage summary.

Table 2 • **MACC Blocks Usage Summary**

CoreFIR	CoreFFT	LMS_ALGO	Total
8	04	1	13

A – List of Changes

The following table lists critical changes that were made in each revision of the chapter in the demo guide.

Date	Changes	Page
Revision 2 (July 2014)	Updated the document for Libero v11.3 software release (SAR 58924).	NA
	The "Theory of Operation" section updated (SAR 58924).	6
Revision 1 (November 2013)	Updated the document for Libero v11.2 software release (SAR 52986).	NA
Revision 0 (May 2013)	Initial release.	NA

B – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com

50200441-2/07.14