ZL30151, ZL30169, ZL3025x, ZL30281, ZL30622, and ZL30722 Series Recommended Power Supply Decoupling and Layout Practices

Introduction

This document details the recommended power supply decoupling and layout practices for the ZL30151, ZL30169, ZL30250, ZL30251, ZL30252, ZL30253, ZL30622, and ZL30722 series of any-to-any clock multipliers, jitter attenuators, and telecom timing integrated circuits (ICs). This document also applies to the ZL30281 Three Output PCIe Clock Generator.

Power Supply Decoupling and Layout Practices

The following common design practices are recommended for improving device power supply noise rejection.

- Allocate one low-ESR 0.1 µF to 1 µF decoupling capacitor for each power pin. Example recommended capacitor types are ceramic X5R and X7R. Each capacitor should be located as close as possible to its respective device power pin. Each capacitor should be connected directly to the power pin and should not share vias to power or ground planes with other decoupling capacitors. Adjacent power pins 12 and 13 can share a single decoupling capacitor to reduce component count.
- Allocate one low-ESR 10 µF bulk capacitor for each device power domain. The power domains consist of the device's 1.8 V and 3.3V power supplies and any optional power islands used with the device's analog supplies. Example recommended capacitor types are ceramic X5R and X7R. Tantalum capacitors can also be used. These capacitors filter low frequency noise (up to several hundred kHz) that originates from switching power supplies. If a ferrite bead is used to connect a power island to a main board power plane, the associated bulk capacitor should be located close to the ferrite bead. Bulk decoupling capacitors can be shared with nearby devices powered by common power domains to reduce component count.
- Allocate one low-ESR 100 µF capacitor to pin VDDXO33 when using a crystal resonator reference connected to pins XA and XB. Example recommended capacitor types are ceramic X5R and X7R. Tantalum capacitors can also be used.
- Connect the device's exposed ground pad (E-PAD) directly to the board's ground plane through a 4x4 array of vias spaced evenly across the pad.
- Power islands can be optionally used on the device's analog supplies to provide improved power rail noise rejection. A power island is a local copper area, separated from the main power plane by a series passive component such as a ferrite bead or low ohm resistor. When a ferrite bead is used, it should have a resistance of several hundred Ohms at 100 MHz. Additionally, it should have a current rating at least double the maximum current required by the associated device power pins to avoid core saturation and degraded performance. Finally, the combination of the ferrite bead inductance and supply decoupling capacitance should be chosen to avoid creating a resonant frequency which could cause gain peaking of a board noise source such as a switching power supply. For both the ferrite bead and low ohm resistor options, the voltage drop across this component must be taken into account in the board's power supply design to ensure the device's power rail specifications are met.

- Each of the ZL30151/169/250/251/252/253/281/622/722 output clocks has an independent power pin for signal format flexibility: VDDO1 for OC1, VDDO2 for OC2, and VDDO3 for OC3. When implementing the above guidelines, any output clock requiring a 3.3 V or 1.8 V supply can share a power island with the corresponding device core analog supply voltage to reduce component count. Additionally, output clock supplies of the same voltage can share a power island.

Figure 1 shows the application of these guidelines to a design which has all output clock signals configured as current-mode logic (CML) which requires a 3.3 V supply.

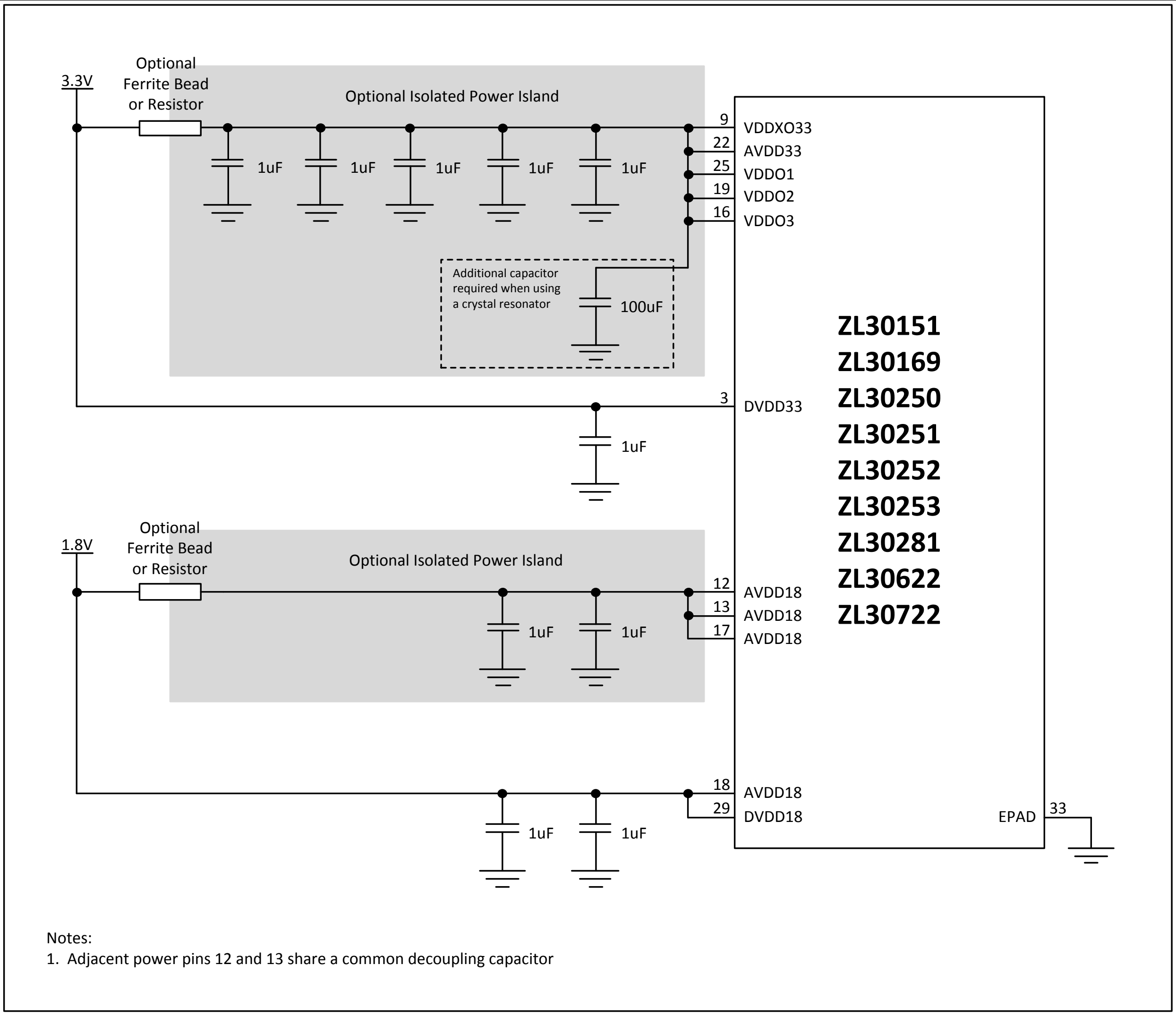

Figure 1 Example ZL30151/169/250/251/252/253/281/622/722 Power Supply Decoupling Scheme

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