IGLOO2

System Builder Port/BIF Name Changes

Microsemi®

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Introduction

Between the Libero 11.1 SP3 (or earlier) and Libero 11.2 releases, names of some System Builder Pins, Pin Groups, and Bus Interfaces for System Builder Blocks have changed. In addition to some port name changes, some extraneous reset ports have been removed, and other ports have been added. These name changes were made in Libero SoC 11.2 (December 2013) or earlier releases to optimize the System Builder Interface for clarity and to support new features. The changes are:

- Remove Pins and Pin Groups (Table 1-1 on page 4)
- Rename Pins and Pin Groups (Table 1-2 on page 5)
- Rename Bus Interfaces (Table 1-3 on page 5)
- Add new Pin names (Table 1-4 on page 6)

If you are migrating from a pre-Libero 11.2 release and your design contains a System Builder Block, read this document to become familiar with the changes before you continue with your System Builder design in Libero SoC 11.2. or subsequent releases.

1 – Migrating from Libero v11.1 SP3 or Earlier Releases to Libero v11.2 or Subsequent Releases

When you use Libero SoC to open a System Builder block created with Libero SoC Release 11.1 SP3 or older, your System Builder block will display the old names. If you want to use the new System Builder interface, or if you are using a SERDES block in your design, you must migrate your designs using the following steps:

1. Click the **Configuration** icon on the System Builder block in the SmartDesign canvas, or double-click the System Builder block to open System Builder.

   Regenerate the System Builder block with the same features and options you chose in the selection pages.

2. In the SmartDesign Canvas, right-click the System Builder block and choose **Update Instances with Latest Component**.

   The System Builder block displays the name changes. The names may be new, changed, or dropped.

   Regenerating your System Builder block results in the following:

   – System Builder ports whose names have changed will be disconnected from other components in the SmartDesign Canvas. Use Table 1-2 to determine the new names for System Builder ports. **You must reconnect System Builder ports to these components manually.**

   – If a component in the SmartDesign Canvas was connected to a System Builder port which was removed, it will be disconnected. **You must reconnect affected pins (as per Table 1-1) or mark them unused.**

   – For new features, new ports appear in the System Builder block. **Connect these to SmartDesign components as needed.**

Table 1-1 • Removed Pins / Pin Groups

Old Names	New Names	Pin Group or Input/Output
FIC32_0_RESET_OUT_N	Removed, use HPMS_READY	Output
FIC32_0_RESET_IN_N	Removed	Input
FIC32_1_RESET_OUT_N	Removed, use HPMS_READY	Output
FIC32_1_RESET_IN_N	Removed	Input
FDDR_Subsystem_RESET_OUT_N	Removed, use INIT_DONE	Output
HPMS_DDR_FIC_Subsystem_RESET_OUT_N	Removed, use INIT_DONE	Output
CORERESETP_0_PINS	Removed	Pin Group
USER_FAB_RESET_N	Removed, use INIT_DONE	Output
EXT_RESET_IN_N	Removed	Input
CoreAHBLite_(0-n)_PINS	Removed	Pin Group
REMAP_M0 or REMAP_M0_(0-n)	Removed	Input

Note: If, in your design, a System Builder output pin that drives a SmartDesign component is removed, you can use the alternate pin mentioned in the New Names column to drive the SmartDesign component. If a System Builder input pin is removed, you can mark the pin driving it as unused.

Table 1-2 • **Renamed Pins / Pin Groups / Bus Interfaces**

Old Name	New Name	Pin Group or Input/Output
FIC32_0_PINS	**FIC_0_PINS**	**Pin Group**
FIC32_0_CLK	FIC_0_CLK	Output
FIC32_0_LOCK	FIC_0_LOCK	Output
FIC32_1_PINS	**FIC_1_PINS**	**Pin Group**
FIC32_1_CLK	FIC_1_CLK	Output
FIC32_1_LOCK	FIC_1_LOCK	Output
FDDR_Subsystem_PINS	**FDDR_SUBSYSTEMS_PINS**	**Pin Group**
CLK_BASE_PLL_LOCK (used to be under the FABDDR_0_PINS group)	FDDR_SUBSYSTEM_CLK_PLL_LOCK	Input
FDDR_Subsystem_CLK	FDDR_SUBSYSTEM_CLK	Input
AXI_S_RMW (used to be under the FABDDR_0_PINS group)	FDDR_AXI_S_RMW	Input
HPMS_DDR_FIC_Subsystem_PINS	**HPMS_DDR_FIC_SUBSYSTEM_PINS**	**Pin Group**
HPMS_DDR_FIC_Subsystem_CLK	HPMS_DDR_FIC_SUBSYSTEM_CLK	Output
HPMS_DDR_FIC_Subsystem_LOCK	HPMS_DDR_FIC_SUBSYSTEM_LOCK	Output
MDDR_DDR_AXI_S_RMW (used to be under <design_name>_HPMS_0_PINS group)	MDDR_AXI_S_RMW	Input
CORECONFIGP_0_PINS	**INIT_PINS**	**Pin Group**
APB_S_PCLK	INIT_APB_S_PCLK	Output
APB_S_PRESETN	INIT_APB_S_PRESET_N	Output
Individual Pins (Not grouped)		
HPMS_FAB_RESET_N	HPMS_READY	Output
USER_FAB_RESET_IN_N (used to be under CORERESETP_0_PINS)	FAB_RESET_N	Input

Table 1-3 • **Renamed Bus Interfaces**

Old Name	New Name
SDIF(0-3)_APBmslave	SDIF(0-3)_INIT_APB
<User_Fabric_Slave_Name>_<AHB/APB/AXI>mslave<n>	*<User_Fabric_Slave_Name>*
<User_Fabric_Master_Name>_<AHB/APB/AXI>mmaster<n>	*<User_Fabric_Master_Name>*
HPMS_FIC_0_USER_MASTER_M1_AHBmmaster (in the case when System Services are used)	HPMS_FIC_0_SYS_SERVICES_MASTER

Table 1-4 • **New Pins / Pin Groups**

Old Name	New Name	Input/Output
N/A	SDIF(0-3)_PERST_N (under SDIF<0-3>_PINS Pin Group)	Input
N/A	POWER_ON_RESET_N (Not under any Pin Group)	Output
N/A	DDR_READY (Not under any Pin Group), added in Libero 11.4	Output
N/A	SDIF_READY (Not under any Pin Group), added in Libero 11.4	Output
N/A	**FAB_CCC_PINS**, added in Libero 11.3	**Pin Group**
N/A	FAB_CCC_GL<0-3> (under the Pin Group - FAB_CCC_PINS), added in Libero 11.3	Output
N/A	**SPI_PADS**	**Pin Group**
N/A	SPI_0_DI	Input
N/A	SPI_0_DO	Output
N/A	SPI_0_CLK	Inout
N/A	SPI_0_SSO	Inout

Note: Refer to the IGLOO2 System Builder User's Guide for details about these new ports.

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A – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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5-02-00520-1/08.14