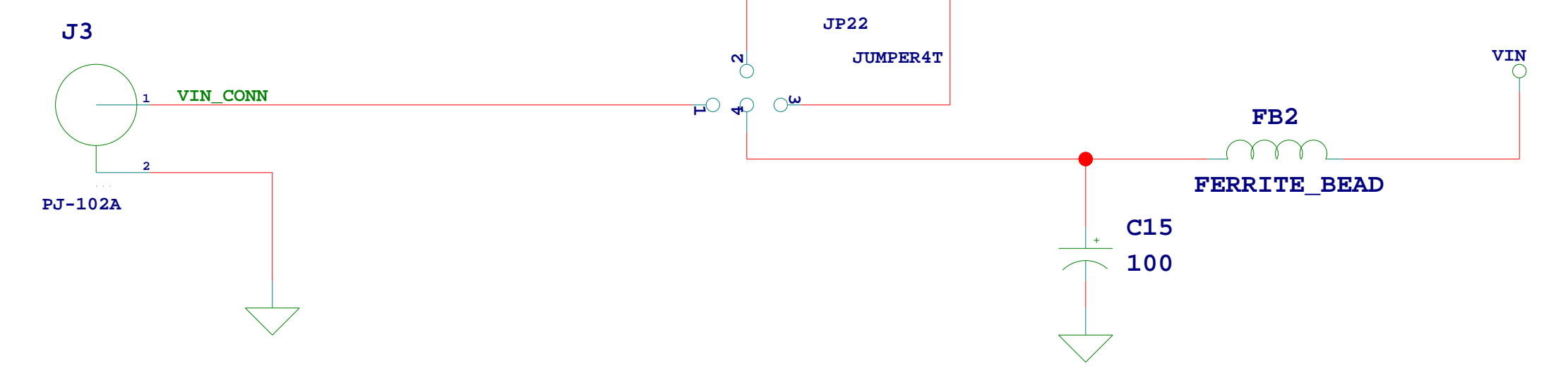
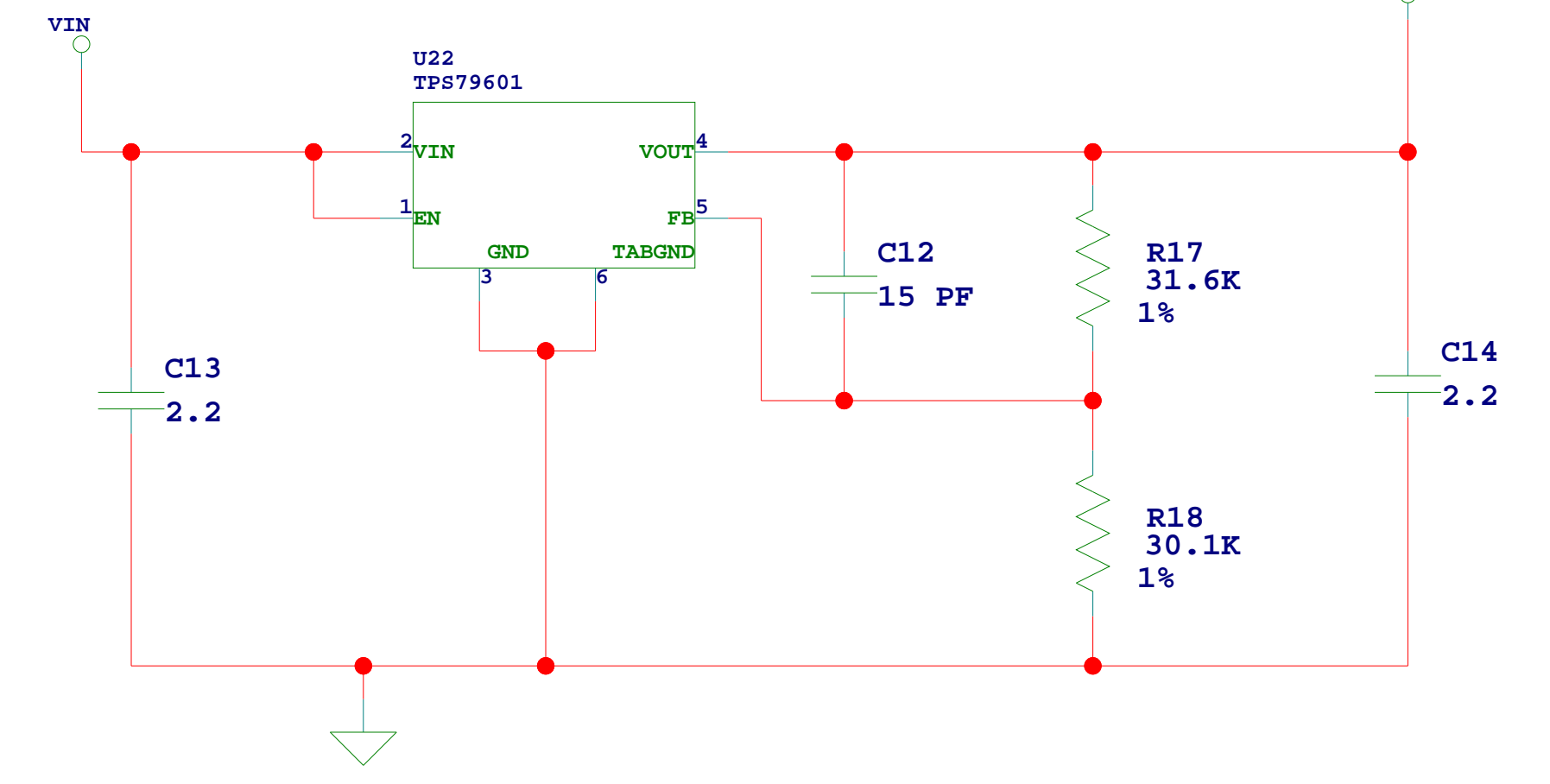


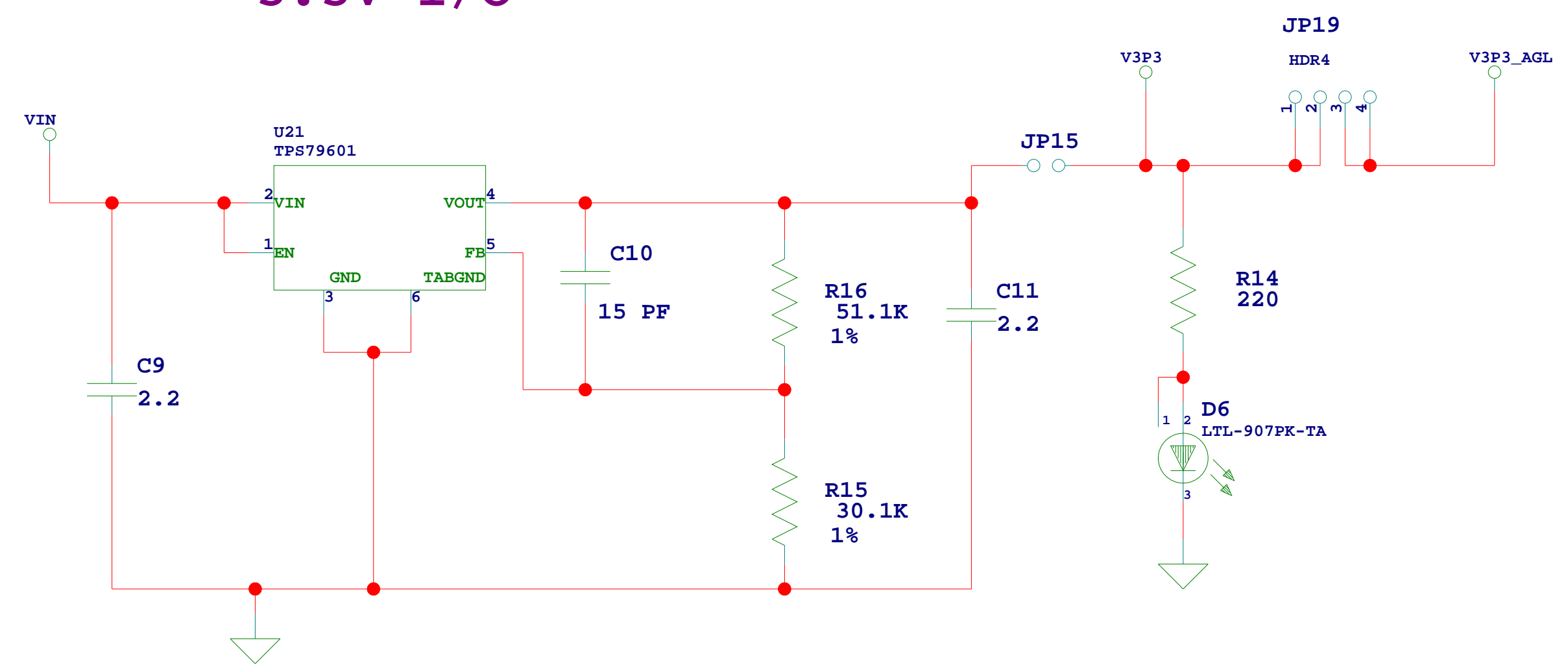
+5.0V DC IN



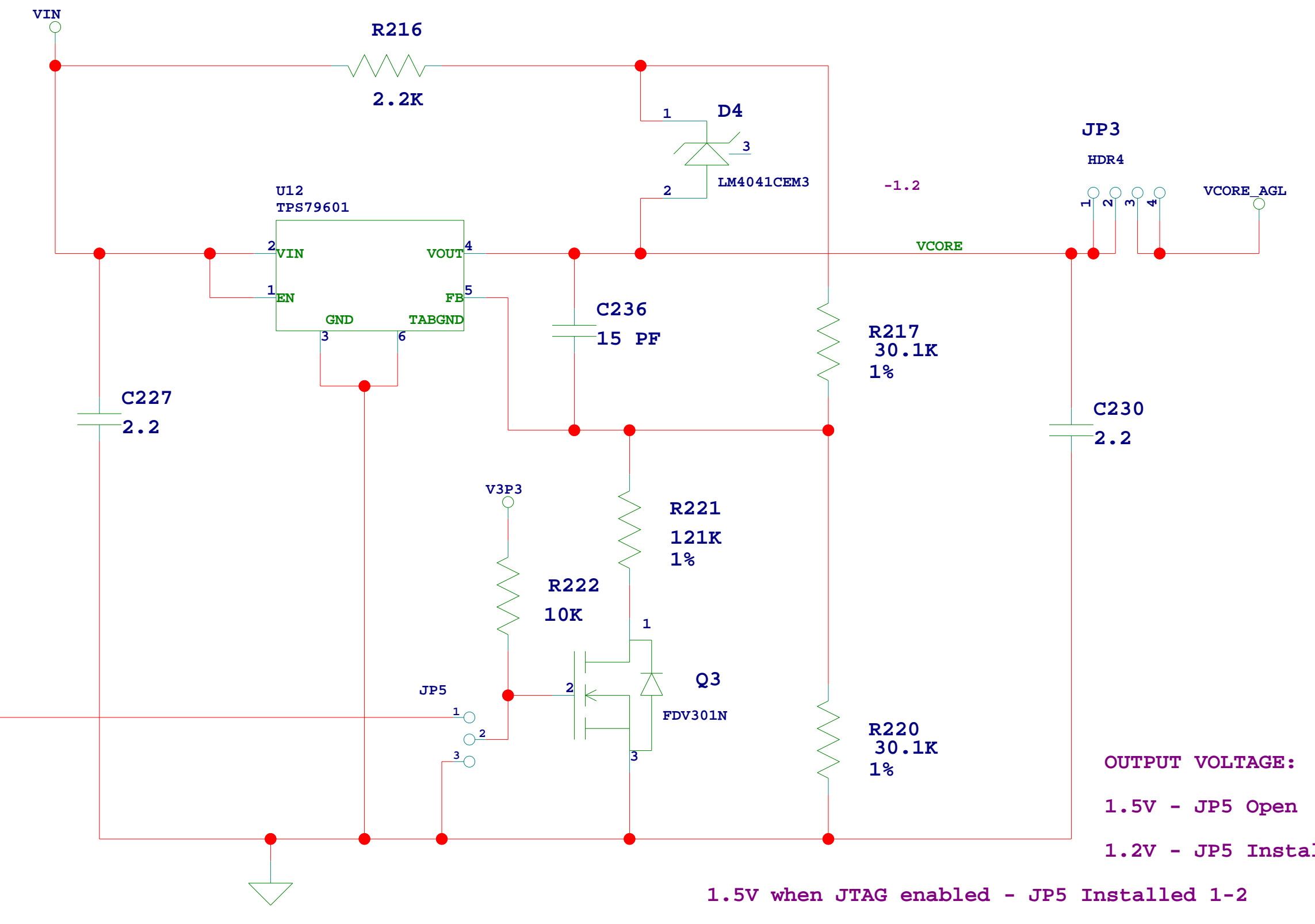
2.5V



3.3V I/O



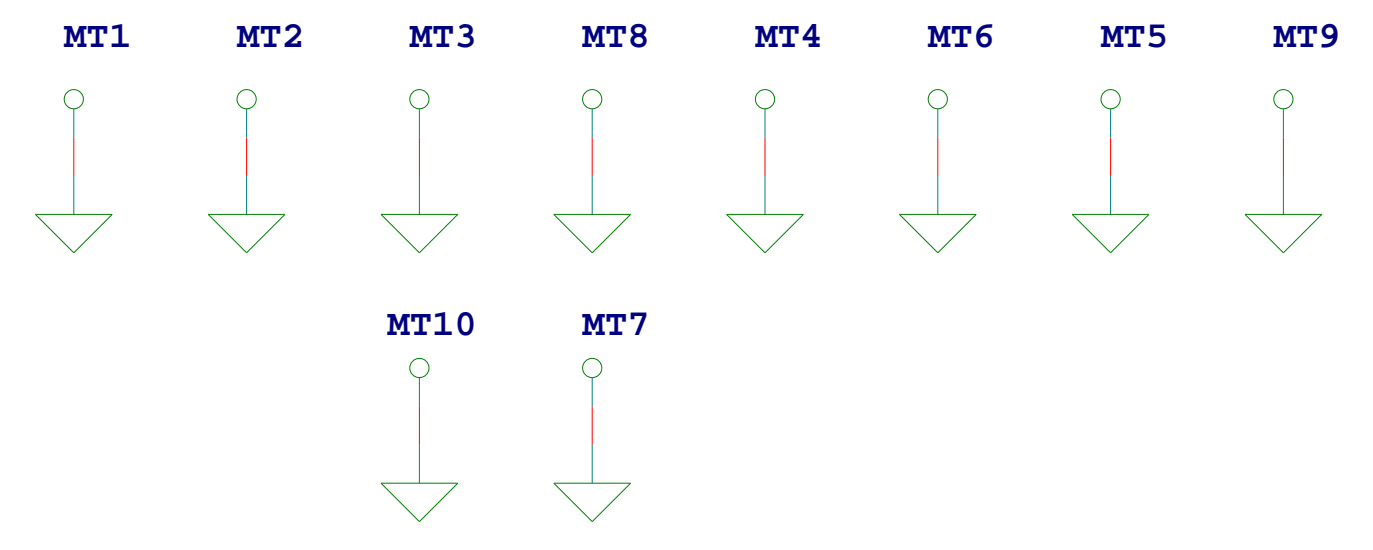
1.2V / 1.5V CORE



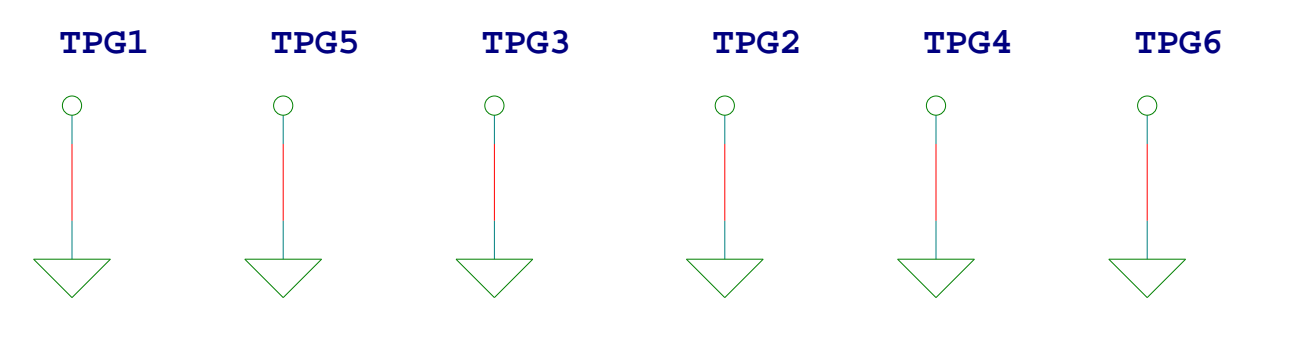
OUTPUT VOLTAGE:
 1.5V - JP5 Open
 1.2V - JP5 Installed 2-3

1.5V when JTAG enabled - JP5 Installed 1-2

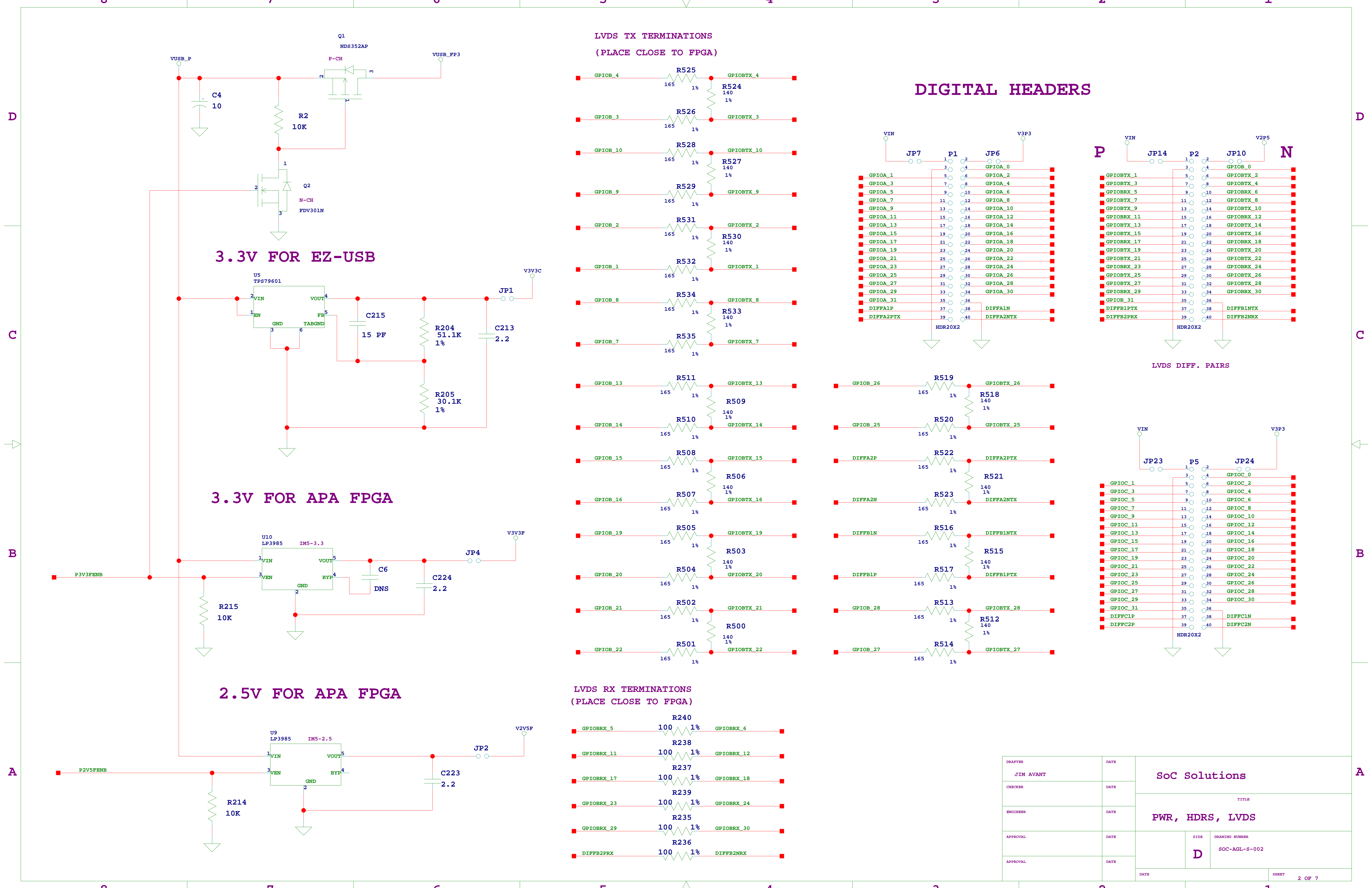
MOUNTING HOLES



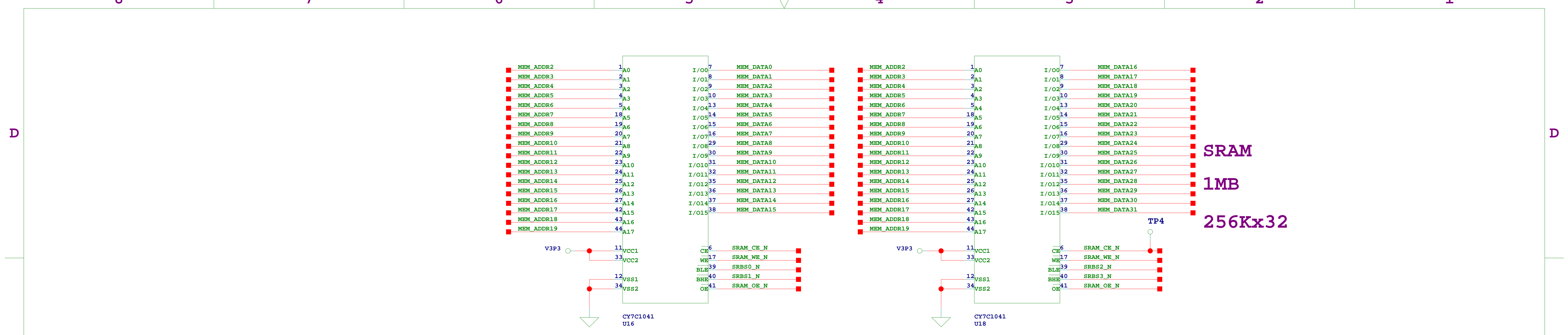
GROUND TESTPOINTS



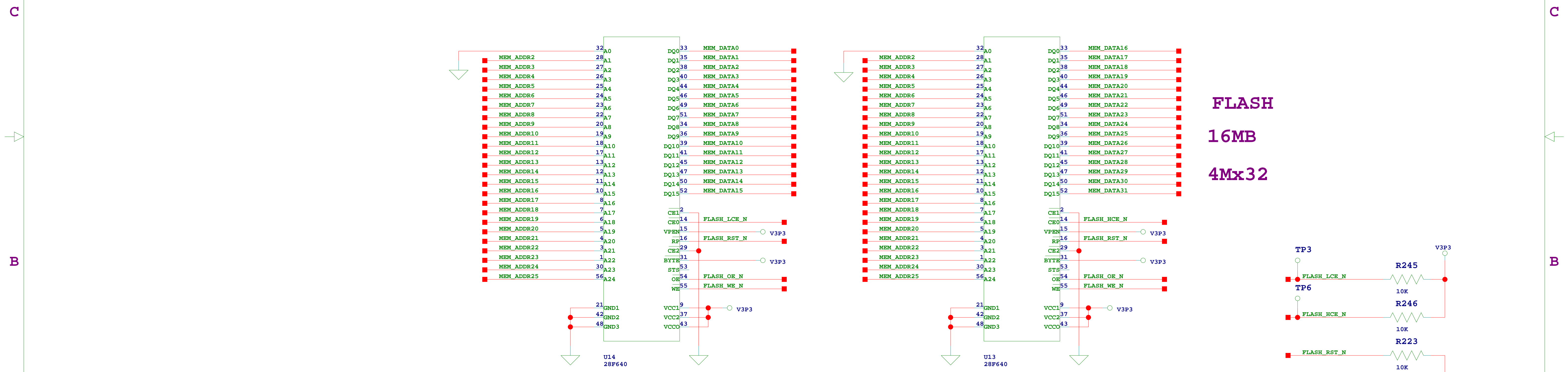
DRAFTER	DATE	SoC Solutions	
JIM AVANT		TITLE	
CHECKER	DATE	POWER SUPPLIES	
ENGINEER	DATE	SIZE	DRAWING NUMBER
APPROVAL	DATE	D	SOC-AGL-S-002
APPROVAL	DATE	DATE	SHEET 1 OF 7



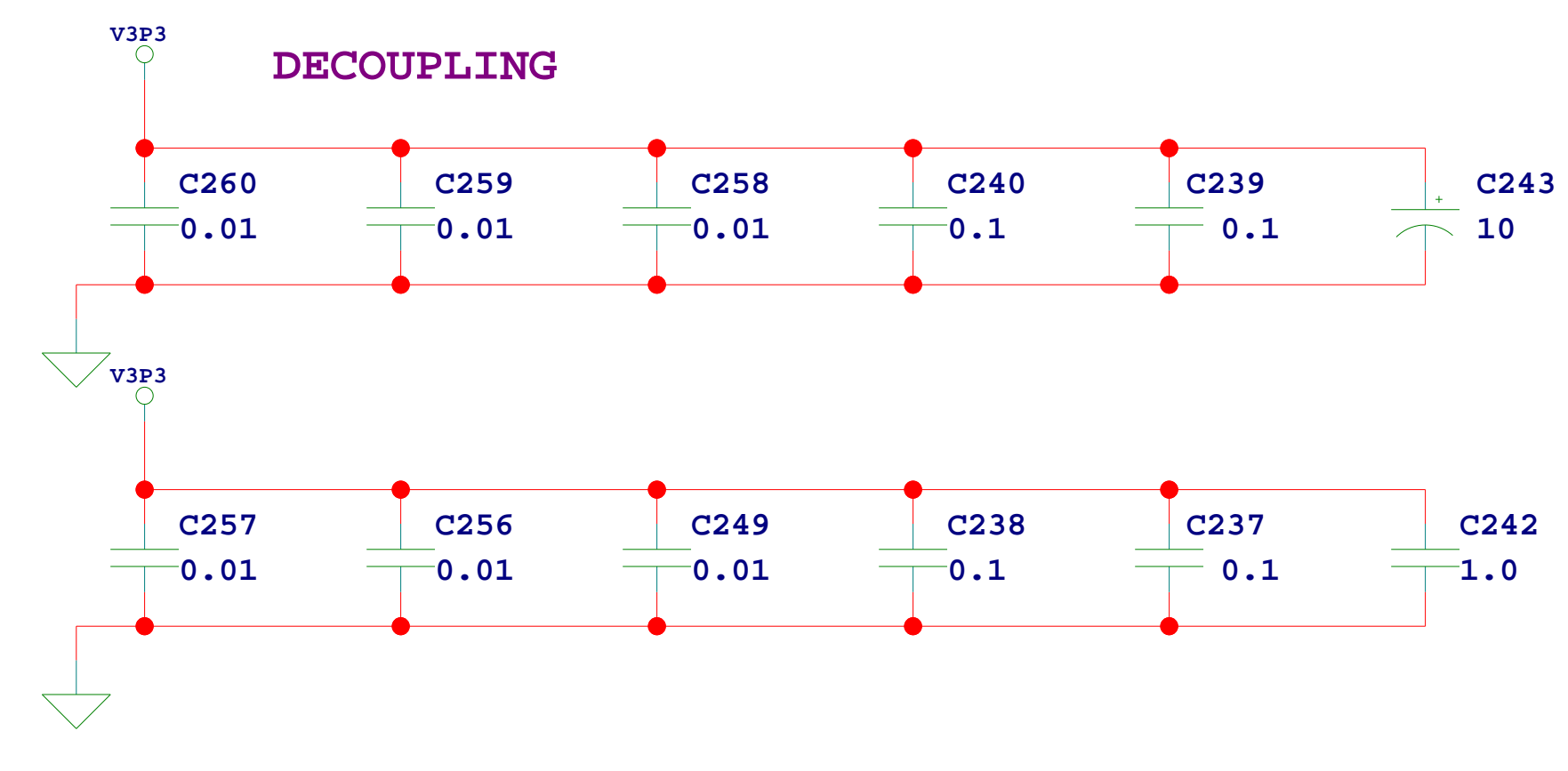
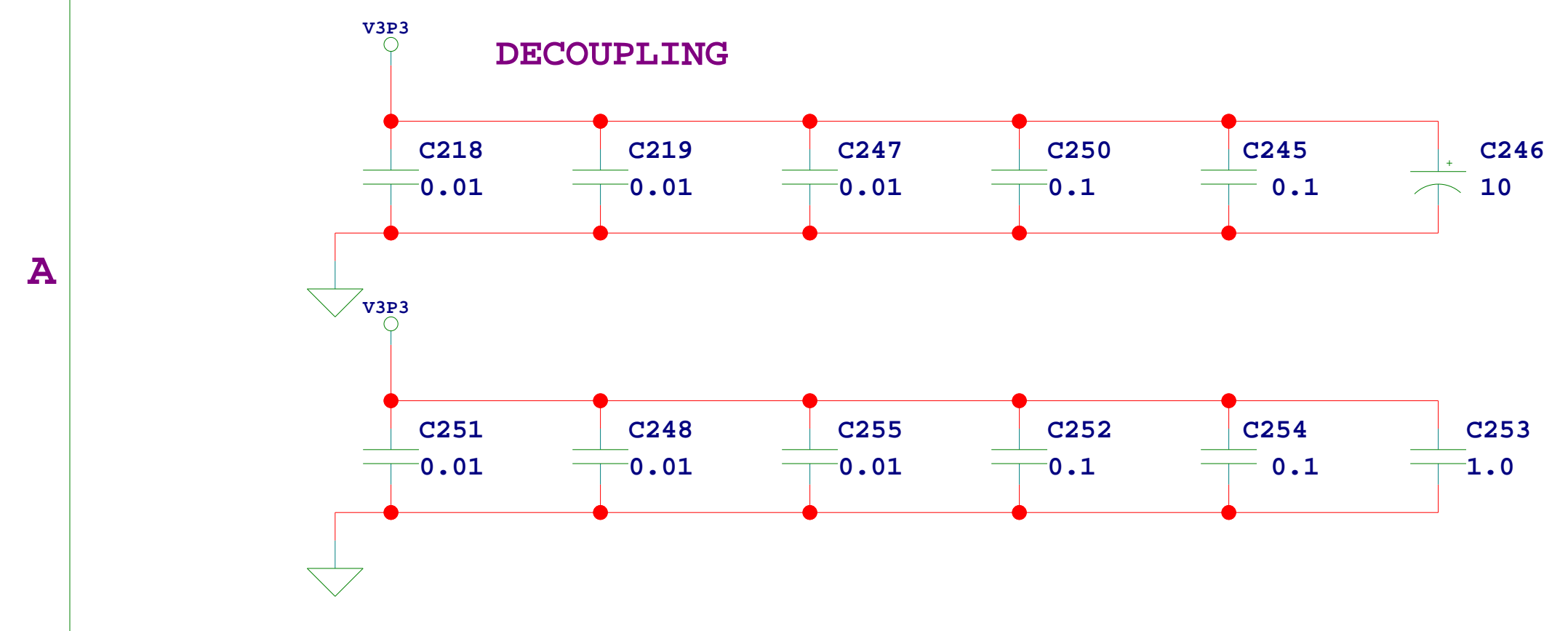
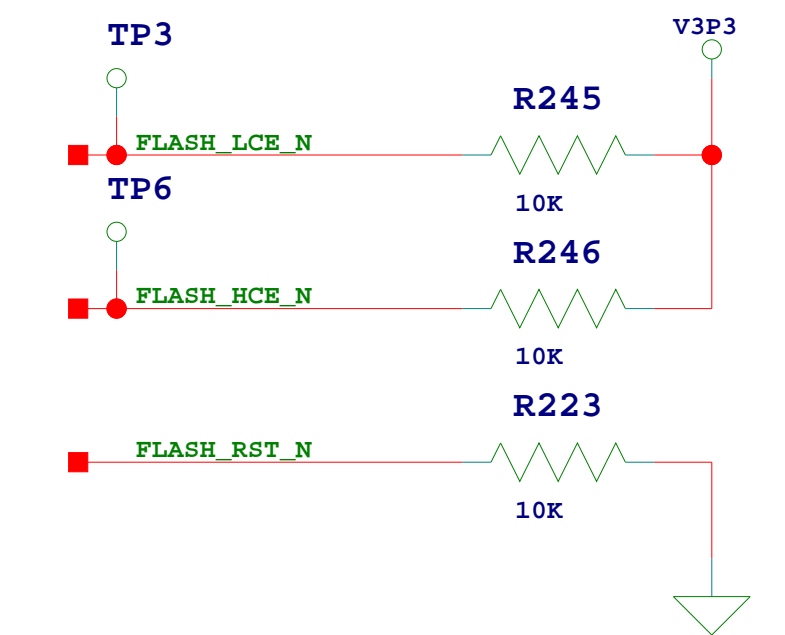
DRAFTER	DATE	SoC Solutions		
JIM AVANT				
CHECKER	DATE	TITLE		
ENGINEER	DATE	PWR, HDRS, LVDS		
APPROVAL	DATE	SIZE	DRAWING NUMBER	
			D	SOC-AGL-S-002
APPROVAL	DATE	DATE	SHEET	2 OF 7



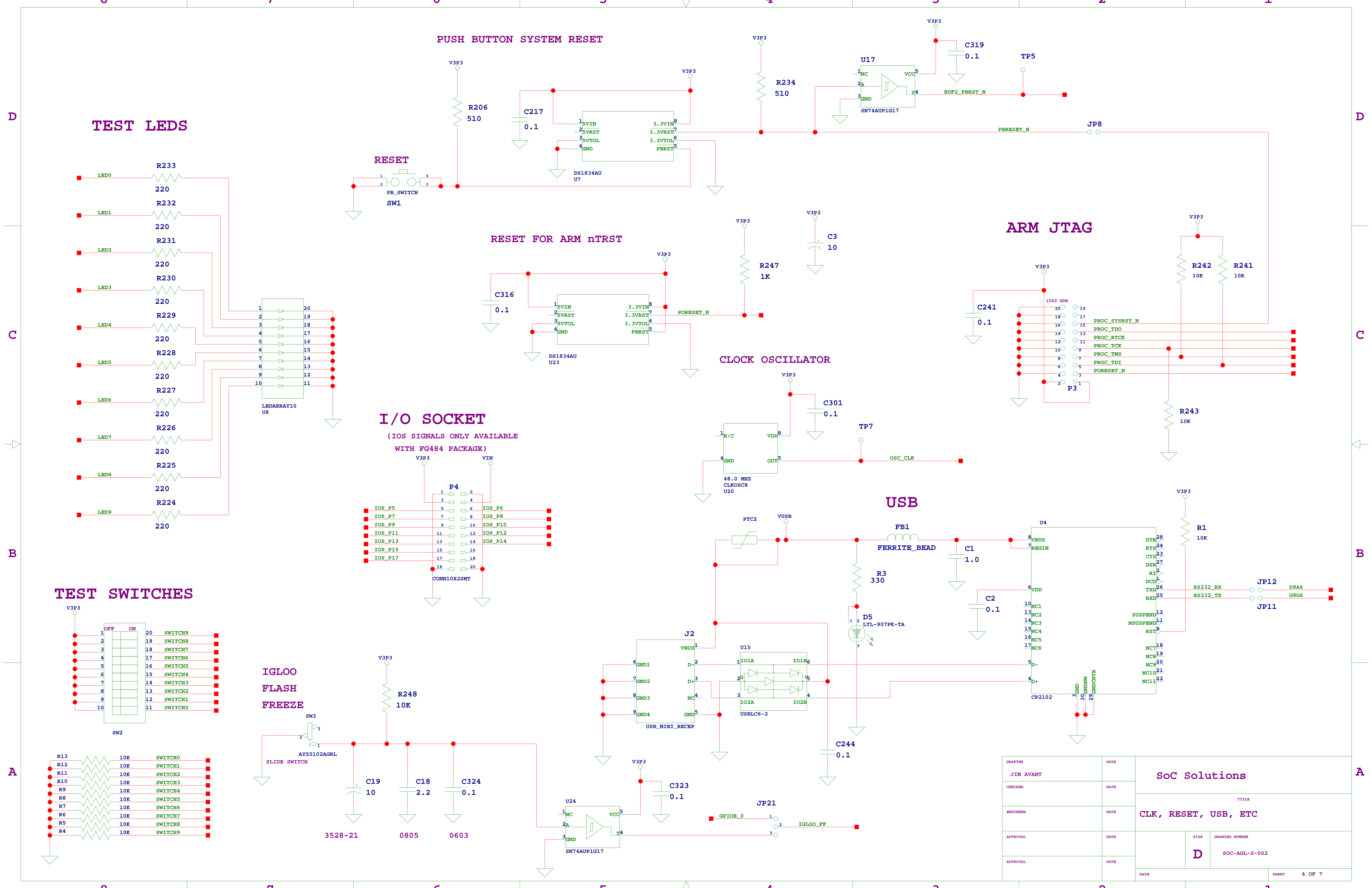
SRAM
1MB
256Kx32



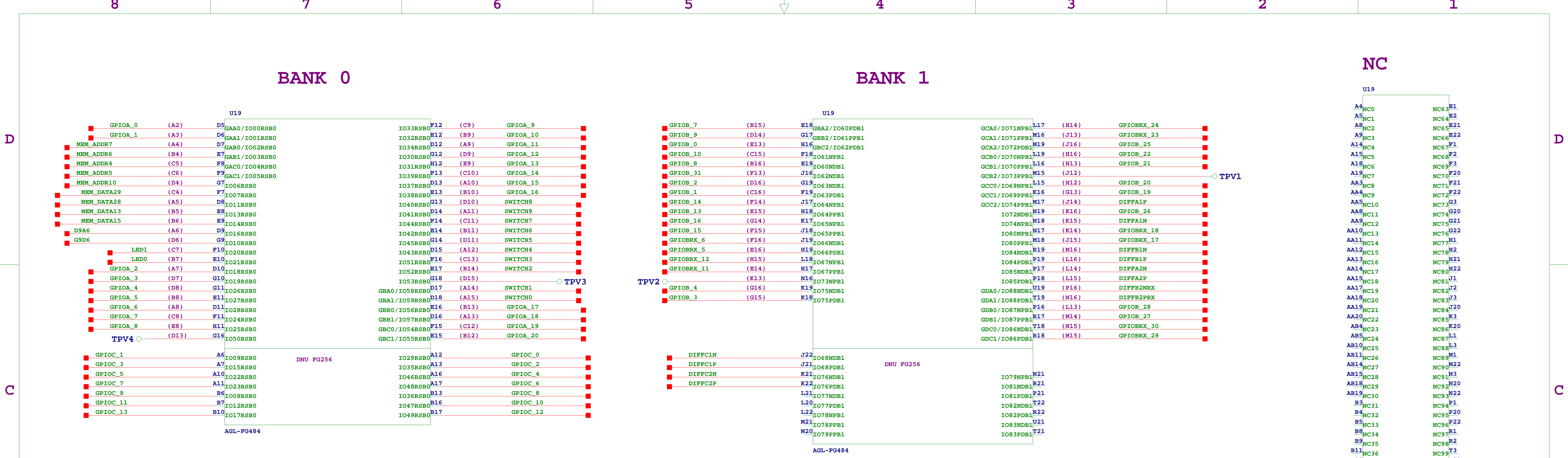
FLASH
16MB
4Mx32



DRAFTER	DATE	SoC Solutions	
JIM AVANT			
CHECKER	DATE	TITLE	
ENGINEER	DATE	SRAM & FLASH	
APPROVAL	DATE	SIZE	DRAWING NUMBER
APPROVAL	DATE	D	SOC-AGL-S-002
	DATE		SHEET 3 OF 7

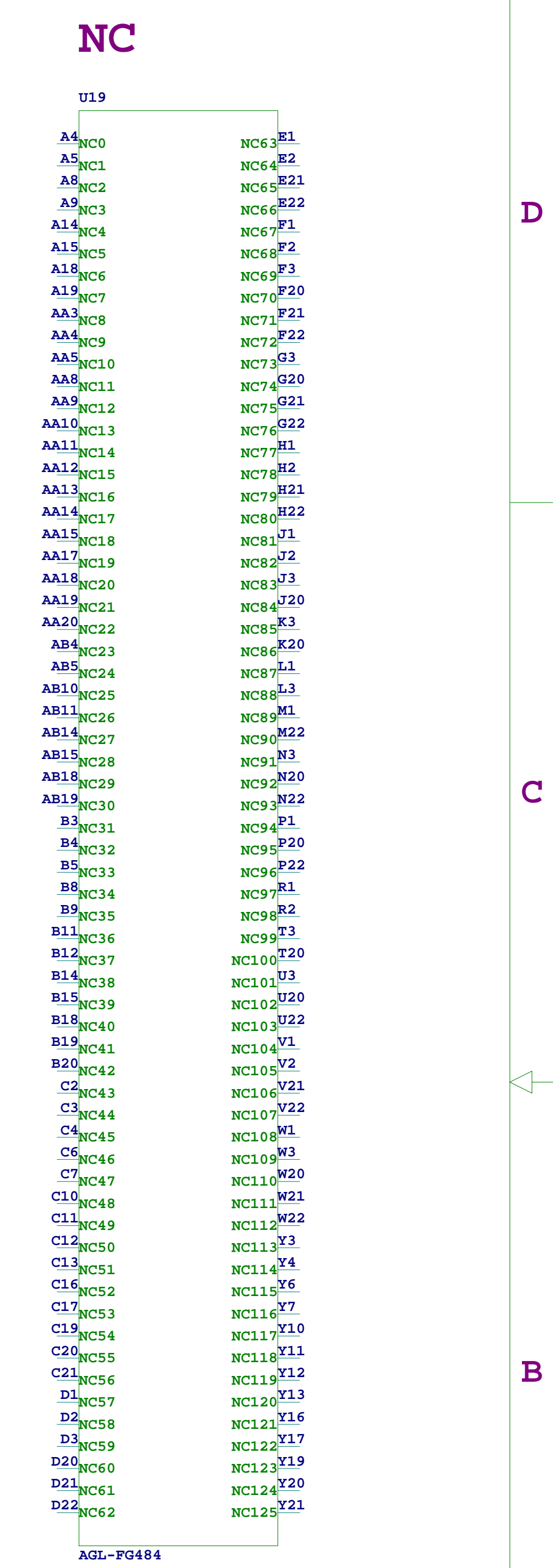
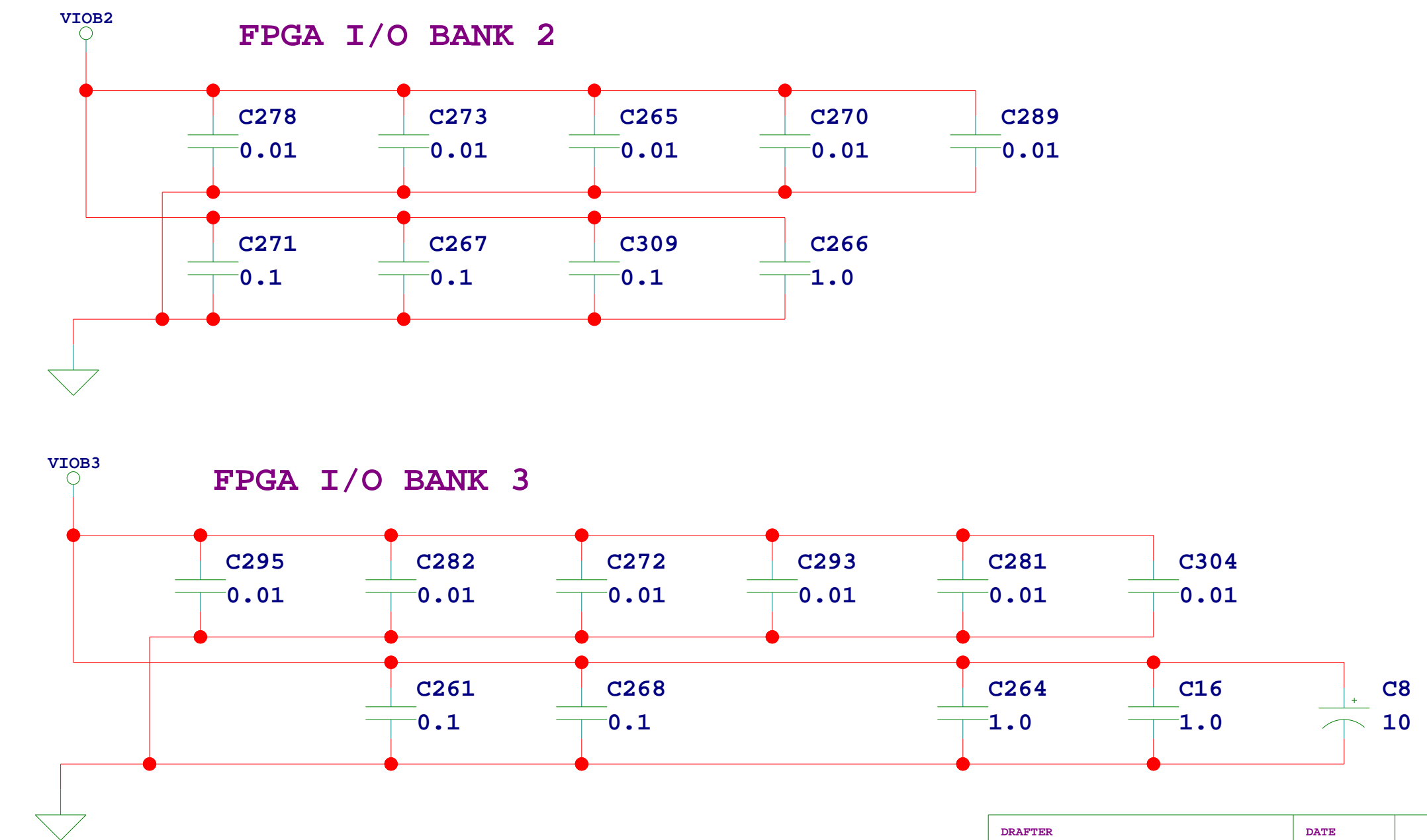
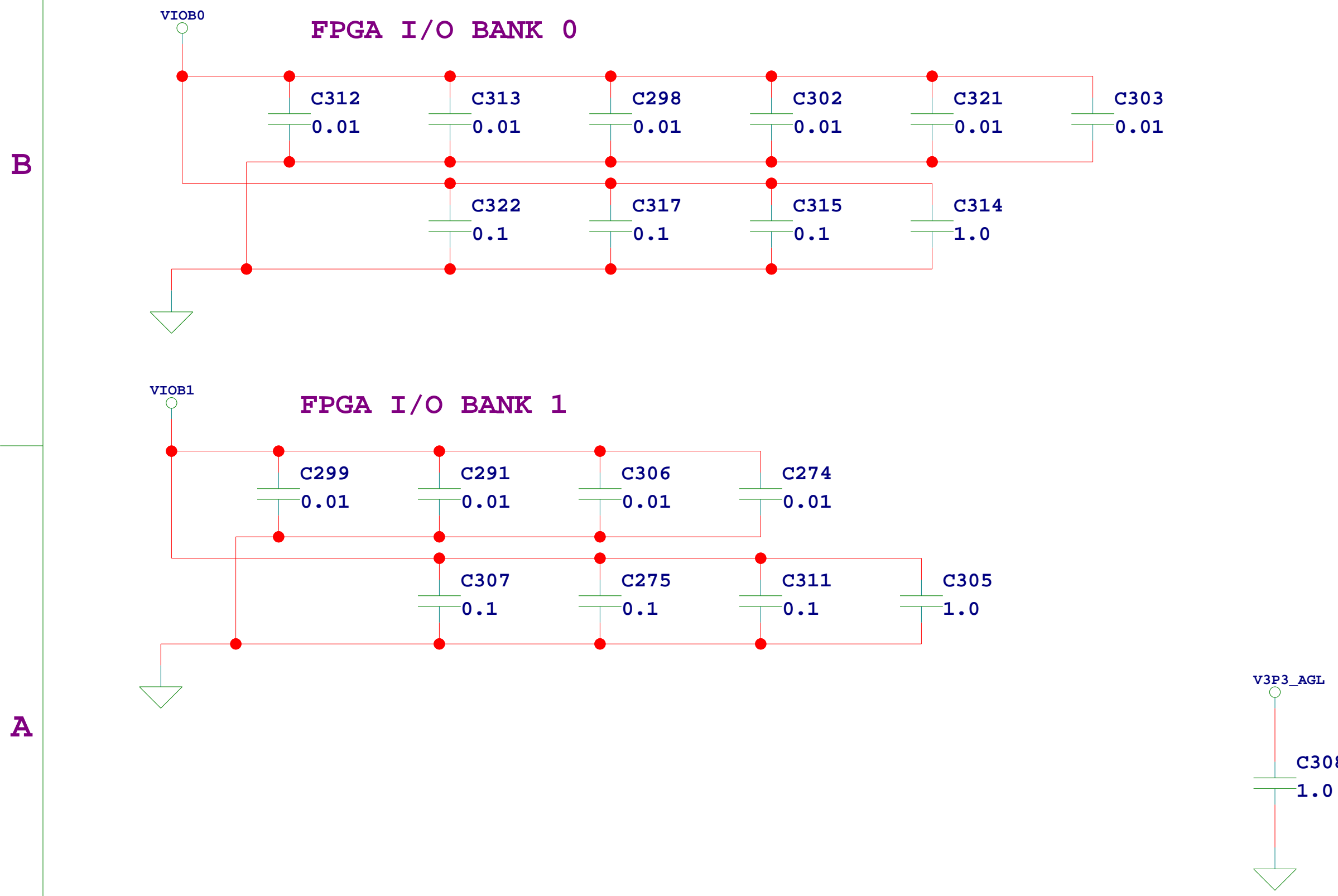


DRAFTER	DATE	SoC Solutions	
JIM AVANT			
CHECKER	DATE	TITLE	
ENGINEER	DATE	CLK, RESET, USB, ETC	
APPROVAL	DATE	SIZE	DRAWING NUMBER
		D	SOC-AGL-S-002
APPROVAL	DATE	DATE	SHEET 4 OF 7

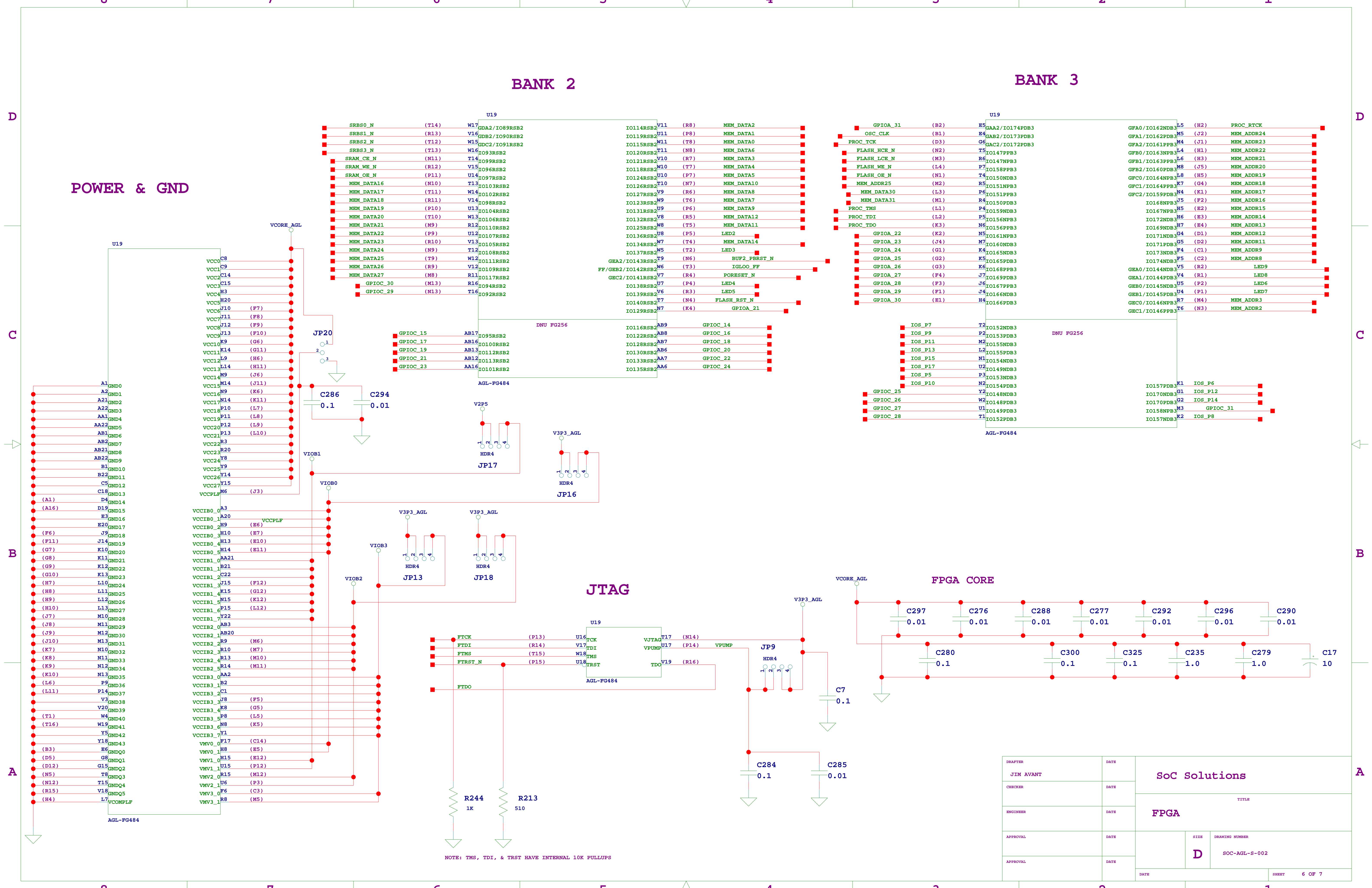


NOTE: BGA BALL NUMBERS SHOWN FOR FG484 PACKAGE WITH FG256 BALL NUMBERS IN PARENTHESES.

NOTE: BOTTOM PORTION OF FPGA SYMBOLS MARKED "DNU FG256" SHOWS BALLS THAT ARE NOT AVAILABLE WHEN THE FG256 PACKAGE IS USED.



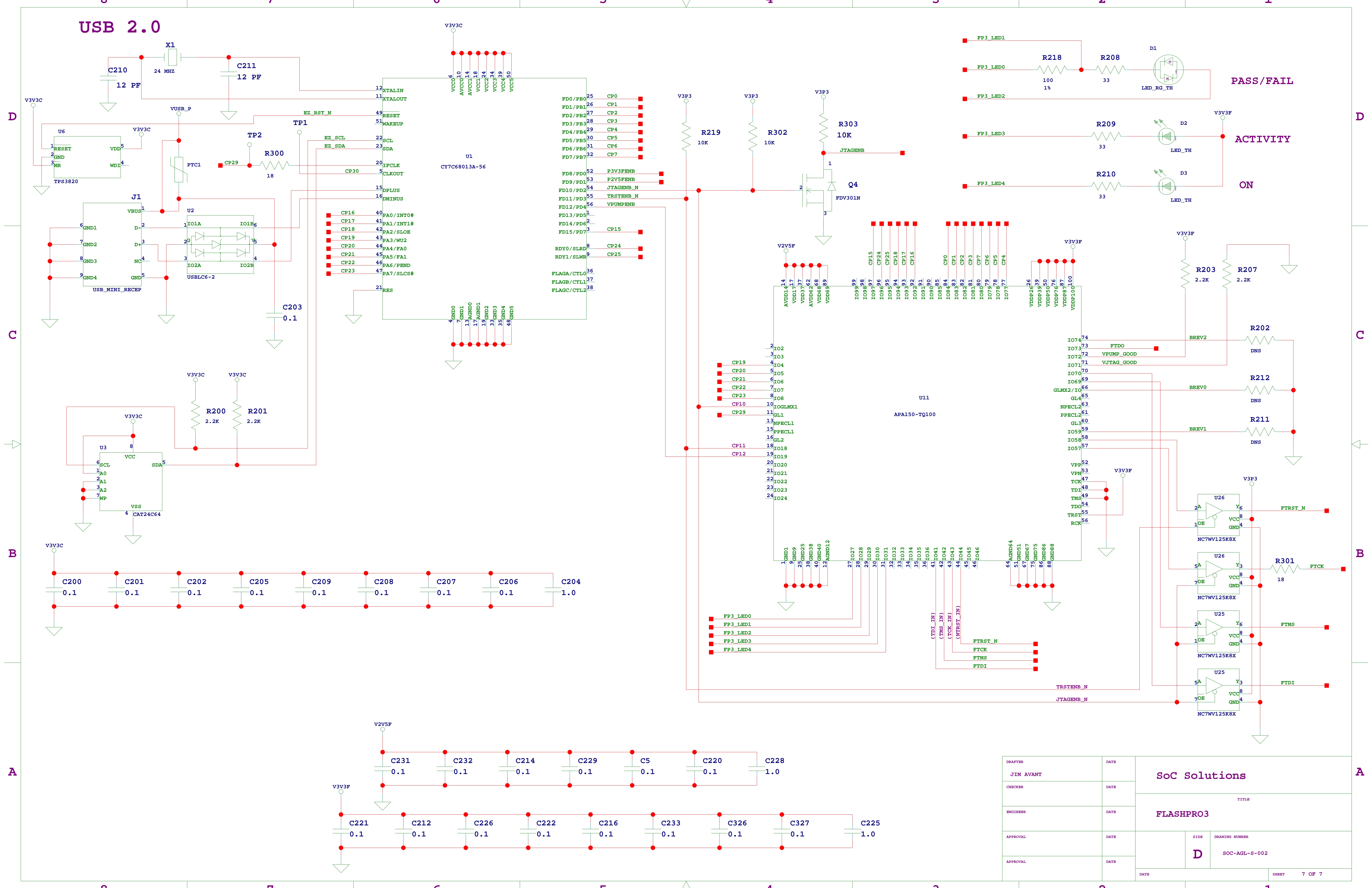
DRAFTER	DATE	SoC Solutions	
JIM AVANT			
CHECKER	DATE	FPGA	
ENGINEER	DATE	D	DRAWING NUMBER
APPROVAL	DATE	DATE	SHEET



NOTE: TMS, TDI, & TRST HAVE INTERNAL 10K PULLUPS

DRAFTER	DATE	SoC Solutions	
JIM AVANT			
CHECKER	DATE	FPGA	
ENGINEER	DATE	SIZE	DRAWING NUMBER
APPROVAL	DATE	D	SOC-AGL-S-002
APPROVAL	DATE		
	DATE		SHEET 6 OF 7

USB 2.0



DRAFTER	DATE	SoC Solutions	
JIM AVANT			
CHECKER	DATE	FLASHPRO3	
ENGINEER	DATE	SIZE	DRAWING NUMBER
APPROVAL	DATE	D	SOC-AGL-S-002
APPROVAL	DATE		
			SHEET 7 OF 7