SmartFusion2 PCIe Data Plane Demo using MSS HPDMA and SMC_FIC

Demo Guide

March 2014

Microsemi

Revision History

Date	Revision	Change
19th March, 2014	1	First release

Confidentiality Status

This is a non-confidential document.

Table of Contents

Preface

About this document

This demo is for SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) devices. It provides instructions on how to use the corresponding reference design.

Intended Audience

SmartFusion2 devices are used by:

- FPGA designers
- Embedded designers
- System-level designers

References

Microsemi® Publications

The following references are used in this document:

- SmartFusion2 and IGLOO2 High Speed Serial Interface Configuration
- SmartFusion2 Microcontroller Subsystem User Guide
- SmartFusion2 SoC FPGA High Speed Serial Interfaces User Guide
- SmartFusion2 PCIe Control Plane Demo User Guide

Refer to the following web page for a complete and up-to-date listing of SmartFusion2 device documentation: www.microsemi.com/soc/products/smartfusion2/docs.aspx.

SmartFusion2 Data Plane Demo using MSS HPDMA and SMC_FIC

Introduction

This demo describes the usage of the embedded features of the SmartFusion2 devices such as peripheral component interconnect express (PCIe) controller, microcontroller subsystem (MSS) high-performance direct memory access (HPDMA) controller and soft memory controller - fabric interface controller (SMC_FIC). The demo uses all of these embedded features and limited FPGA resources. The objective of this demo is to show ease-of-use, optimized resource utilization and low power. In this demo, the PCIe advanced extensible interface (AXI) is accessed through the SMC_FIC AXI interface. This demo shows the performance of the PCIe and HPDMA through SMC_FIC of SmartFusion2 device.

An application, **PCIe_Demo** that runs in the Host PC is provided for setting up and initiating the DMA transactions from the SmartFusion2 PCIe endpoint to the Host PC device. Drivers for connecting the Host PC to the SmartFusion2 PCIe endpoint are provided as part of the demo deliverables.

Microsemi provides three different PCIe data plane demos for SmartFusion2 devices:

- ***PCIe data plane demo using MSS HPDMA Demo Guide*:** This demo shows the low throughput data transfers between PCIe and double data rate (DDR).
- **PCIe data plane demo using MSS HPDMA and SMC_FIC** (current demo)**:** This demo shows the medium throughput data transfers between PCIe and embedded static random access memory (eSRAM).
- ***PCIe data plane demo using 2 channel fabric DMA Demo Guide*:** This demo shows the high throughput data transfers between PCIe and large SRAM (LSRAM).

The high-speed serial interface (SERDESIF) available in the SmartFusion2 devices provides a fully hardened PCIe endpoint implementation and is compliant to the PCIe Base Specification Revision 2.0 and 1.1. For more information, refer to the *SmartFusion2 SoC FPGA High Speed Serial Interfaces User Guide*.

For a tutorial design on how to develop and use the PCIe endpoint including the tools flow and simulation, refer to the *SmartFusion2 PCIe Control Plane Demo Users Guide*.

Table 1 • **Reference Design Requirements and Details**

Reference Design Requirements and Details	Description
Hardware Requirements	
• SmartFusion2 Development Kit that has: – FlashPro4 programmer – 12 V adapter – PCI Edge Card Ribbon Cable	Rev D or later
Host PC or Laptop	Any 64-bit Windows Operating System
Software Requirements	
Libero® System-on-Chip (SoC) software	v11.3
FlashPro programming software	v11.3
PCIe_Demo application	-

Demo Design

Introduction

The demo design files are available for download from the following path in the Microsemi website:
www.microsemi.com/download/rsc/?f=M2S_PCIe_MSSHPDMA_SMCFIC_DF

The demo design files include:

- Drivers_64bit OS
- GUI
- Libero project
- Programming files
- Readme.txt file

Figure 1 shows the top-level structure of the design files. For more details, refer to the readme.txt file.

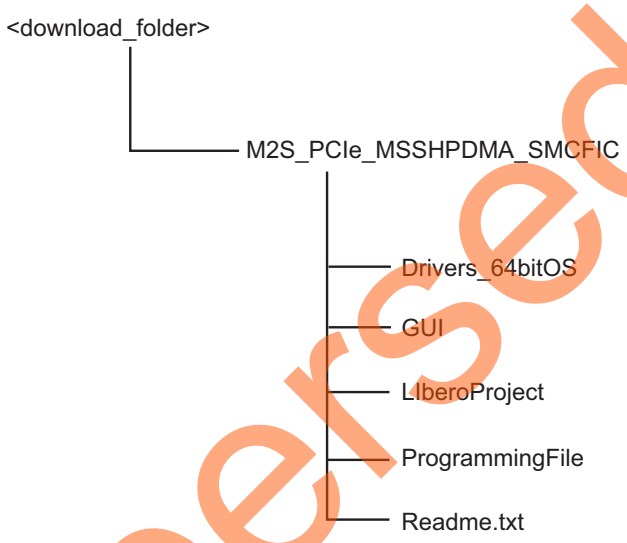

Figure 1 • **Demo Design Files Top-Level Structure**

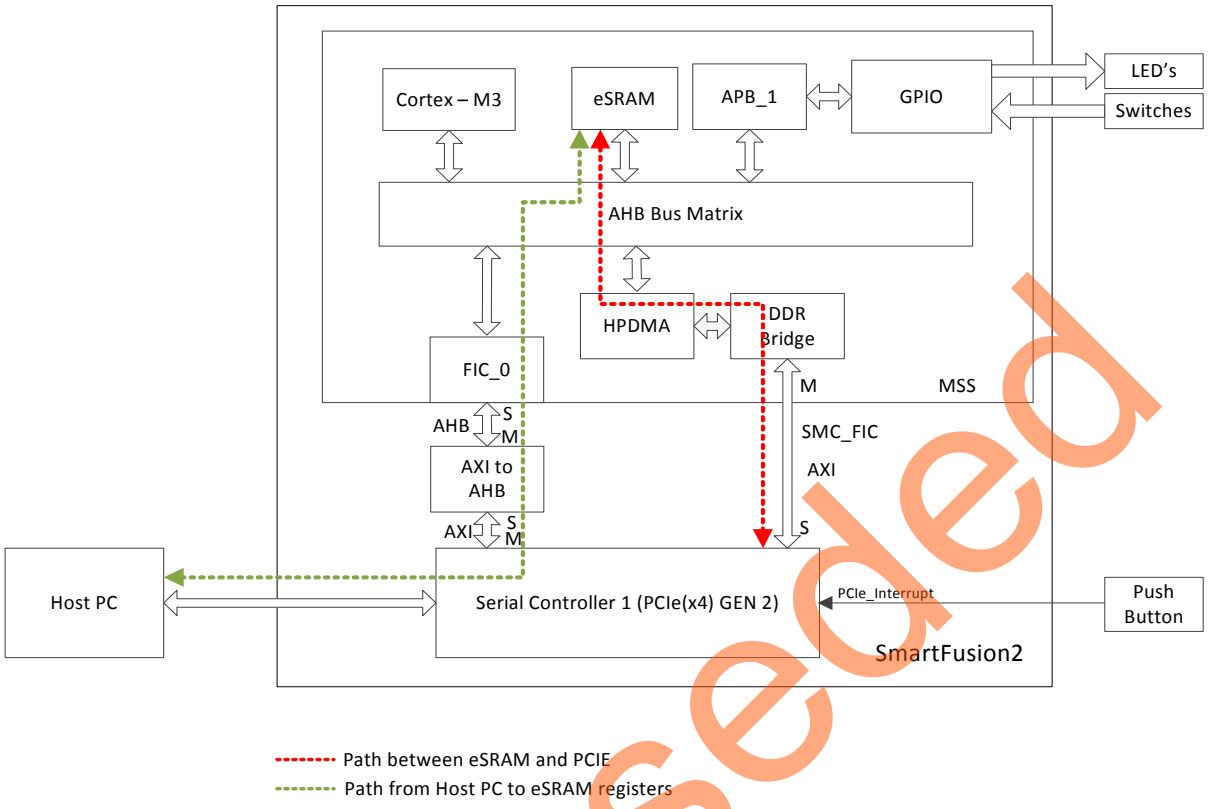

Figure 2 • **PCIe Data Plane Demo Block Diagram**

Figure 2 describes the demo-design. The PCIe core in the SmartFusion2 devices supports both AXI and AMBA® high-performance bus (AHB) master and slave interfaces. This demo design uses the AXI master and slave interfaces to achieve maximum bandwidth.

The PCIe_Demo application on the Host PC initiates the DMA transfers and the embedded PCIe core in the SmartFusion2 device initiates the AXI transactions through the AXI master interface to the AXI to AHB logic in the FPGA fabric. The AXI to AHB logic initiates AHB transactions to eSRAM through FIC_0 (the green line in Figure 2 shows this path). The firmware running on the Cortex-M3 processor reads the registers in eSRAM and initializes the HPDMA depending on the type of DMA transfer. In this demo, FIC_0 interface is used only for configuring registers in eSRAM for initiating HPDMA.

The PCIe AXI slave interface is connected to SMC_FIC AXI interface. The HPDMA accesses PCIe through the SMC_FIC and performs the DMA transactions to eSRAM (the red line in Figure 2 shows this path). In this demo, all data transfers occur through the AXI based SMC_FIC interface.

Note: The SMC_FIC AXI interface supports only WRAP type of Read burst transactions. The fabric logic converts these WRAP type transactions into INCR type transactions as the PCIe AXI interface supports only INCR type of burst transfers.

In this demo design, the following configurations are done:

- The SERDES_IF_1 in the SmartFusion2 device is configured for PCIe 2.0, x4 lanes and Gen2 rate.
- BAR0 and BAR1 are configured in 32-bit memory mapped memory mode. The AXI master window 0 is enabled and configured to map the BAR0 memory address space to MSS general purpose input output (GPIO) address space to control the MSS GPIOs. The AXI master window 1 is enabled and configured to map the BAR1 memory address space to eSRAM address space to perform read and write operations from the PCIe interface. The AXI slave window 0 is enabled and configured to map the SmartFusion2 local address space to the Host PC address space.

- MSS GPIO block is enabled and configured as:
  - GPIO_0 to GPIO_7 as outputs and connected to LEDs
  - GPIO_8 to GPIO_11 as inputs and connected to DIP switches

The PCIe AXI interface clock and ARM® Cortex™-M3 processor clock are configured to run at 166 MHz.

Demo Design Features

- DMA data transfers between the Host PC memory and the eSRAM.
- Throughput for every DMA data transfer.
- Enables continuous DMA transfers for observing throughput variations.
- Displays the PCIe link enable/disable, negotiated link width, and the link speed on the PCIe_Demo application.
- Displays the position of DIP Switches on SmartFusion2 Development Kit on the PCIe_Demo application.
- Displays the PCIe configuration space on the PCIe_Demo application.
- Controls LEDs on the board according to the command from the PCIe_Demo application.
- Enables read and write operations to scratchpad register in the FPGA fabric.
- Interrupts the Host PC, when the Push button is pressed. The PCIe_Demo application displays the count value of the number of interrupts sent from the board.

Demo Design Description

Following are two types of data transfers supported by this demo design.

- Host PC Memory to eSRAM
- eSRAM to Host PC Memory

Host PC Memory to eSRAM

A data transfer from PC memory to the eSRAM happens in the following sequence:

1. HPDMA is setup over the PCIe link based on the settings in the GUI.
2. HPDMA initiates AHB read transactions to the DDR bridge.
3. The DDR bridge converts these AHB read transactions into AXI read transactions (32-byte burst) to the PCIe AXI interface.
4. The PCIe core sends a memory read (MRd) transaction layer packets (TLP) to the Host PC.
5. The Host PC returns with a completion with data (CplD) TLP to the PCIe link.
6. This return data completes the AXI read initiated by DDR bridge. The DDR bridge stores this data into read buffer.
7. The DDR bridge returns this buffered data to HPDMA. The return data completes the AHB read initiated by HPDMA controller.
8. HPDMA writes the return data to eSRAM.
9. HPDMA repeats this process until the transfer size set in the Host PC GUI is completed.

eSRAM to Host PC Memory

A data transfer from the eSRAM to PC memory happens in the following sequence:

1. HPDMA is setup over the PCIe link based on the settings in the GUI.
2. HPDMA reads the data from eSRAM by initiating an AHB read transaction to eSRAM.
3. The data is written to the PCIe core as an AHB write transaction through the DDR bridge. The DDR bridge buffers up to 32 bytes of these write transactions.
4. The DDR bridge initiates an AXI write transaction (32 byte burst) to the PCIe AXI interface.
5. The PCIe core sends a memory write (MWr) TLP to the Host PC.
6. HPDMA repeats this process until the transfer size set in the Host PC GUI is completed.

Throughput Calculation

This demo uses MSS timer to measure the throughput of DMA transfers.The throughput measured includes all of the overhead of the AXI, PCIe, and DMA controller transactions. The procedure for measuring throughput is:

1. Setup the DMA controller for the data transfer.
2. Start the MSS timer and the DMA controller.
3. Initiate data transfer for the requested number of bytes.
4. Wait until DMA transfer is completed.
5. Record the number of clock cycles consumed for steps 2-4.

To arrive at a realistic system performance, the throughput calculation takes into account all the overheads during a transfer. The Throughput formula is as shown below:

Throughput = Transfer Size (Bytes) / (Number of clock cycles taken for a transfer * Clock Period)

Setting Up the Demo Design

Jumper Settings for Smart Fusion2 Development Kit

1. Connect the jumpers on the SmartFusion2 SoC FPGA Development Kit, as shown in Table 2.

   CAUTION: While making the jumper connections, the power supply switch SW7 must be switched off.

Table 2 • **SmartFusion2 SoC FPGA Development Kit Jumper Settings**

Jumper	Pin (from)	Pin (to)	Comments
J70, J93, J94, J117, J123, J142, J157, J160, J167, J225, J226, J227	1	2	default
J2	1	3	default
J23	2	3	default

2. Connect the FlashPro4 programmer to the J59 connector of SmartFusion2 SoC FPGA Development Kit.
3. Connect the power supply to the J18 connector.
4. Switch on the power supply switch, SW7.

Programming the Device

Download the demo design from:
www.microsemi.com/soc/download/rsc/?f=M2S_PCIe_MSSHPDMA_SMCFIC_DF

1. Launch the FlashPro software.
2. Click **New Project**. Figure 3 shows the **FlashPro - New Project** dialog.
3. In the **New Project** dialog, type the project name.

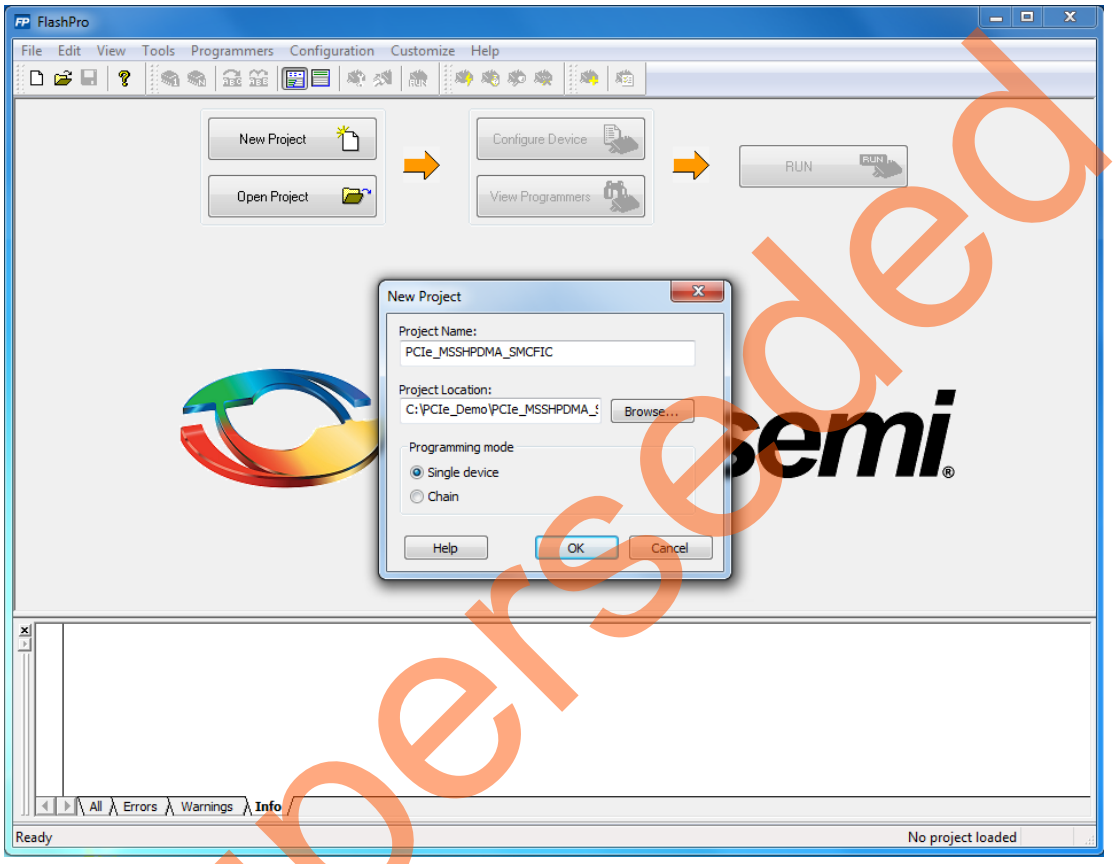

Figure 3 • **FlashPro- New Project Dialog**

4. Click **Browse** and navigate to the location where it is required to save the project.
5. Select **Single Device** as the **Programming Mode**.
6. Click **OK** to save the project.
7. Click **Configure Device**.
8. Click **Browse** and navigate to the location where the `PCIe_HPDMA_SMCFIC_top.stp` file is located and select the file. The default location is: <download_folder>\M2S_PCIe_MSSHPDMA_SMCFIC_DF\ProgrammingFile\

9. Click **Open**. The required programming file is selected and is ready to be programmed in the device.

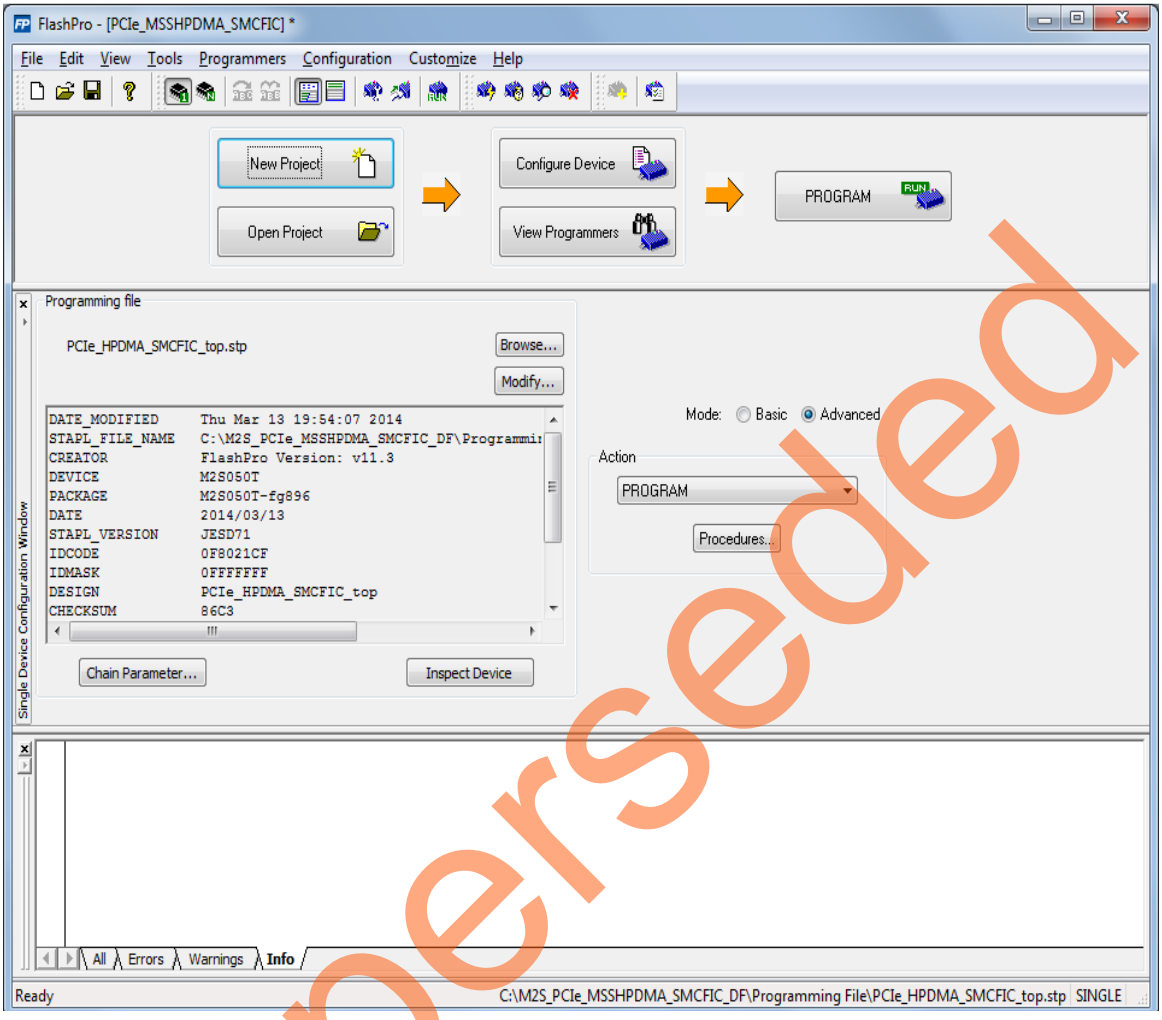

Figure 4 • **FlashPro Project Configured**

10. Click **PROGRAM** to start programming the device. Wait until you get a message indicating that the program passed.

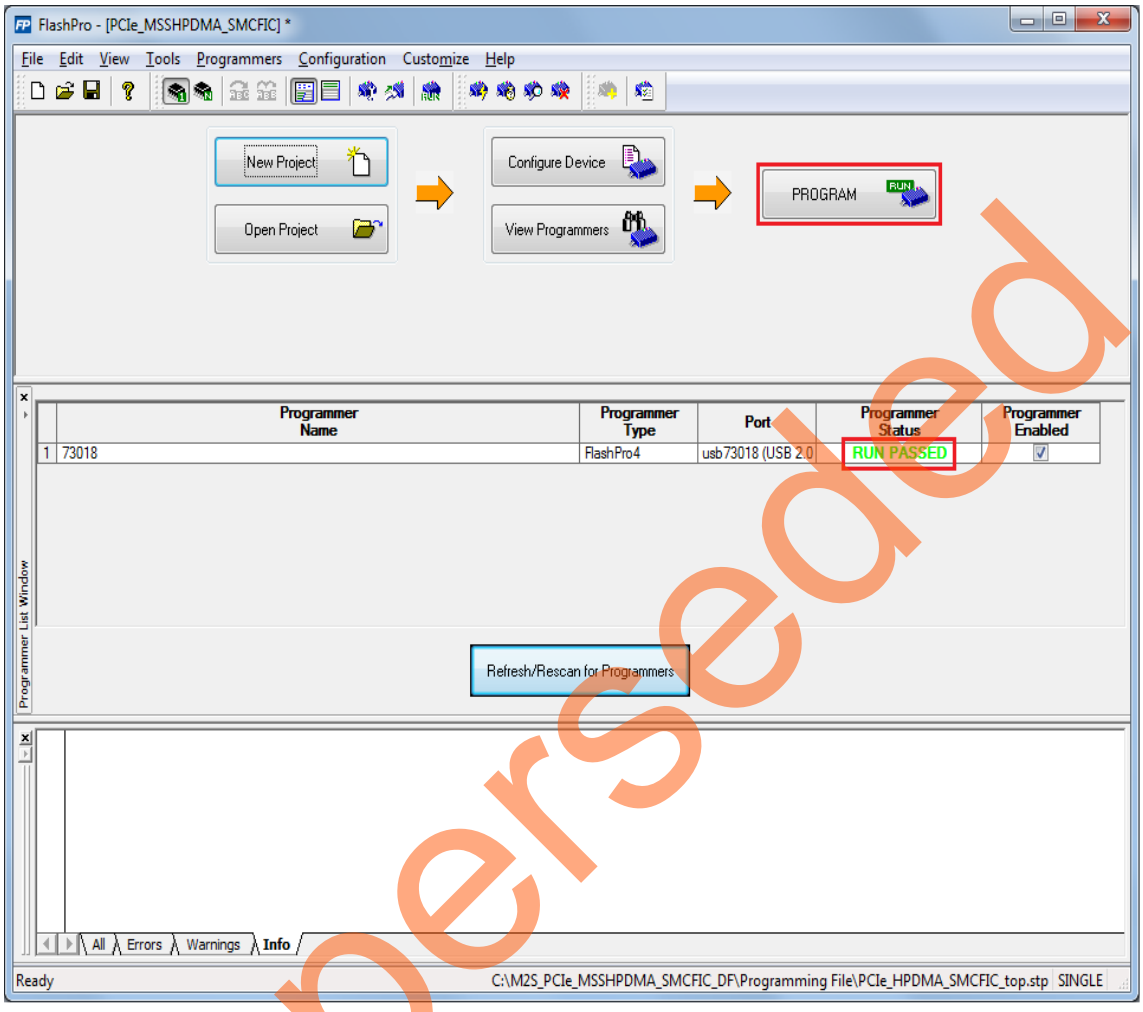

Figure 5 • **FlashPro Programming Passed**

Connecting the Kit to the Host PC PCIe Slot

1. After successful programming, **power off** the SmartFusion2 Development Kit and **shut down** the Host PC.
2. Connect the J230 - PCIe Edge connector of SmartFusion2 Development Kit to Host PC's PCIe slot through the PCI Edge Card Ribbon Cable.

Note: Ensure that the Host PC is switched off when plugging the PCIe connector cable to PCIe slot.

3. Figure 6 shows the board setup for the Host PC in which SmartFusion2 Development Kit is connected to the Host PC PCIe slot.

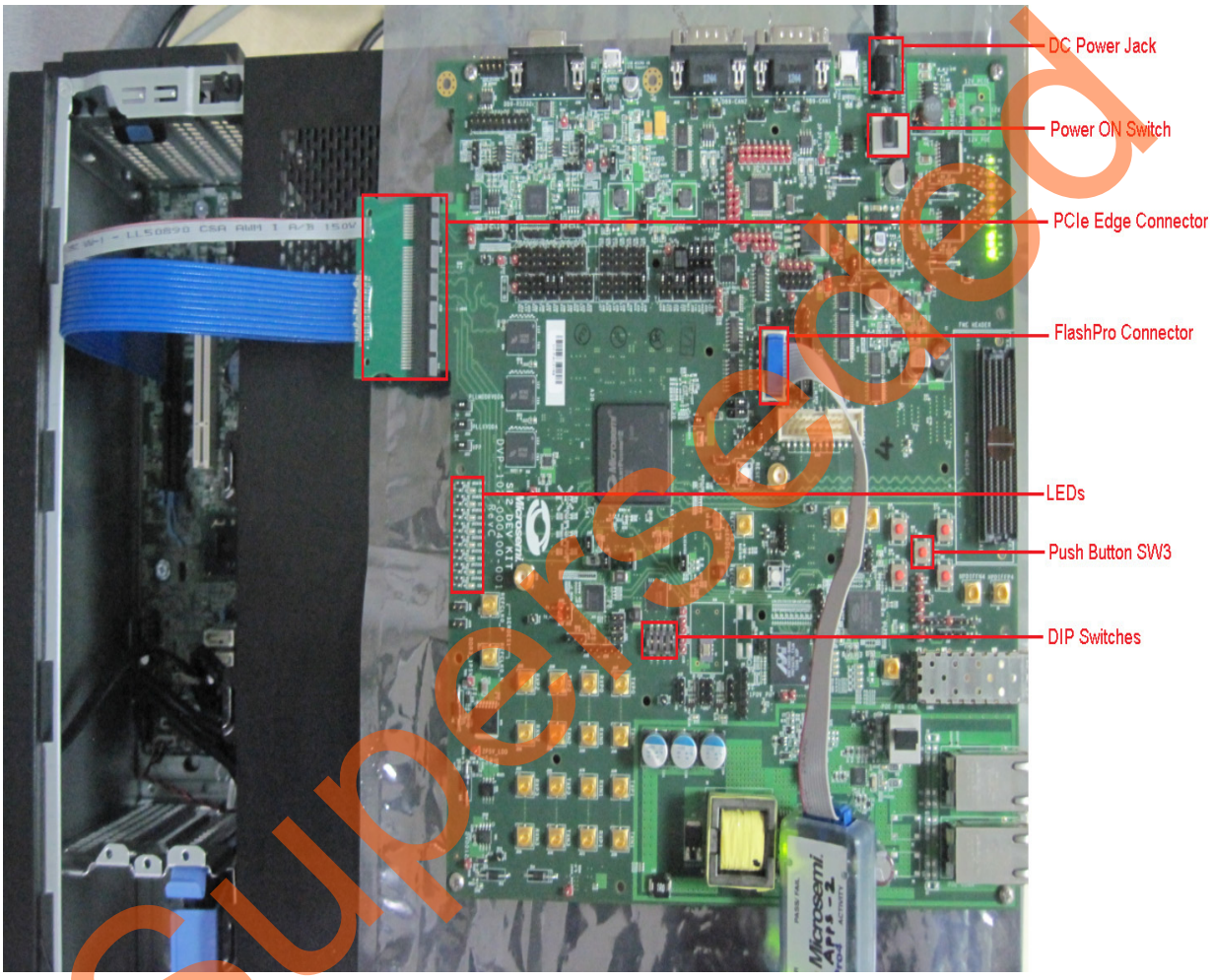

Figure 6 • **SmartFusion2 Development Kit Setup**

4. Switch on the power supply switch, SW7.

5. Power on the Host PC and check the **Device Manager** of the Host PC for **PCIe Device**. Figure 7 shows the **Device Manager** window.

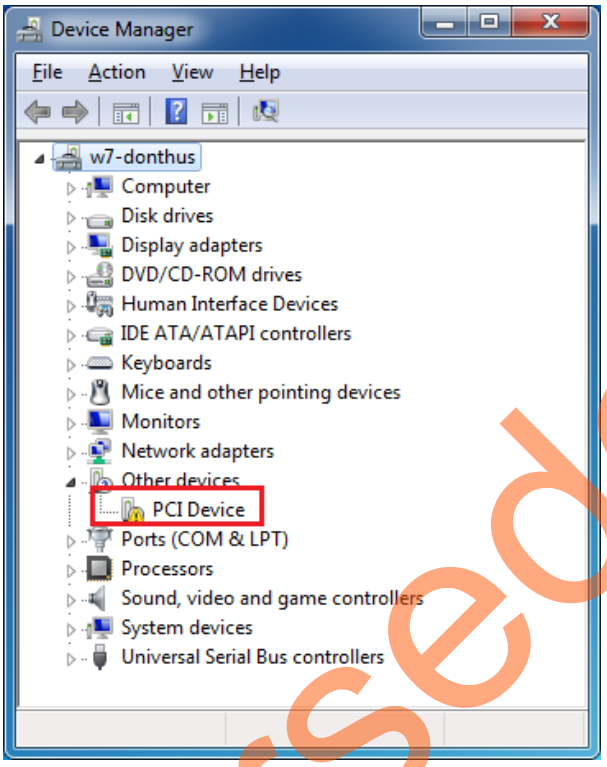

Figure 7 • **Device Manager - PCIe Device Detection**

6. If the device is not detected, power cycle the SmartFusion2 Development Kit and click **scan for hardware changes** option in the **Device Manager** window. Figure 8 shows the **scan for hardware changes** option in the **Device Manager.**

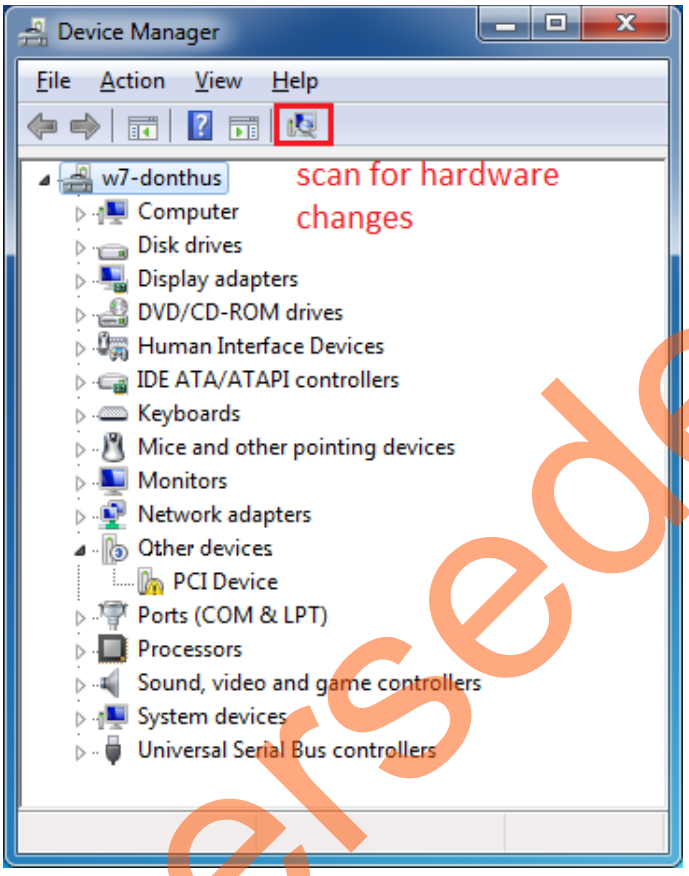

Figure 8 • **Scan for Hardware Changes** Option in the **Device Manager** Window

Note: If the device is still not detected, check whether or not the BIOS version in the Host PC is latest, and if PCIe is enabled in the Host PC BIOS.

7. If the Host PC has any other installed drivers (previous versions of Jungo drivers) for the PCIe device, uninstall them.

a. To uninstall previous Jungo drivers go to device manager and right-click on **DEVICE**. Refer to Figure 9.

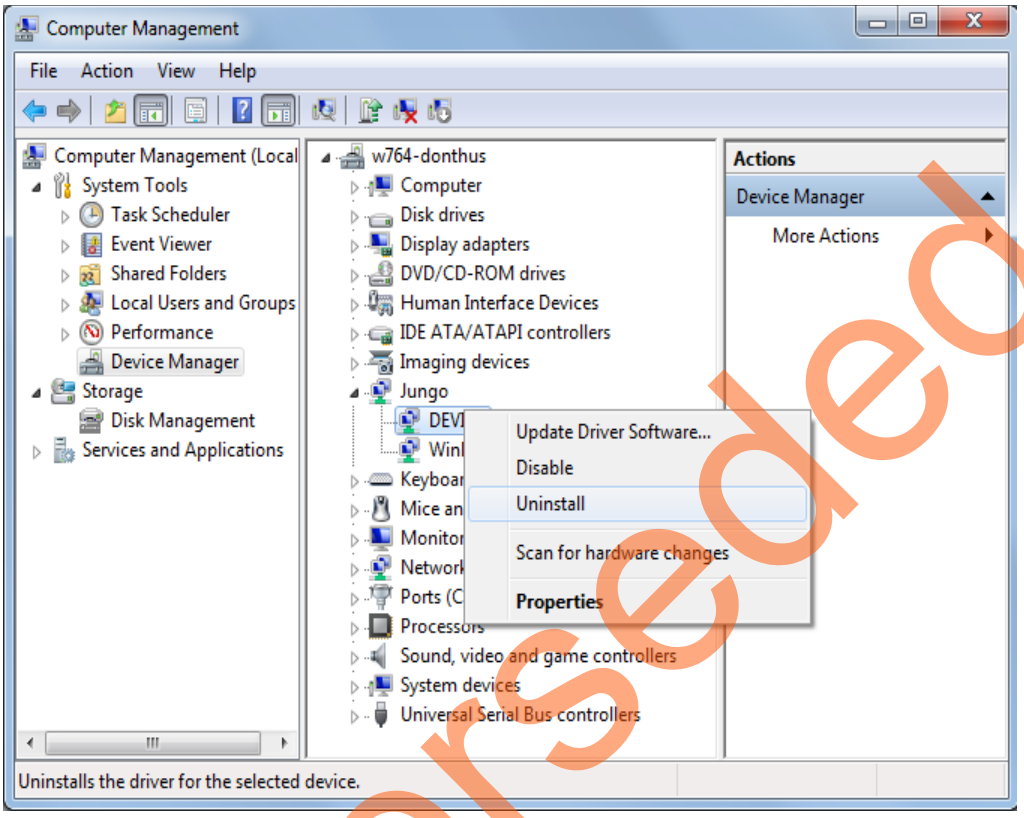

Figure 9 • **Uninstalling Jungo Driver**

b. From the **Confirm Device Uninstall** dialog, select **Delete the driver software for this device** and click **OK**. After uninstalling previous Jungo drivers, make sure that the PCIe Device is detected in the **Device Manager** window. Figure 10 shows the **Delete the driver software for this device** check box in the **Confirm Device Uninstall** dialog.

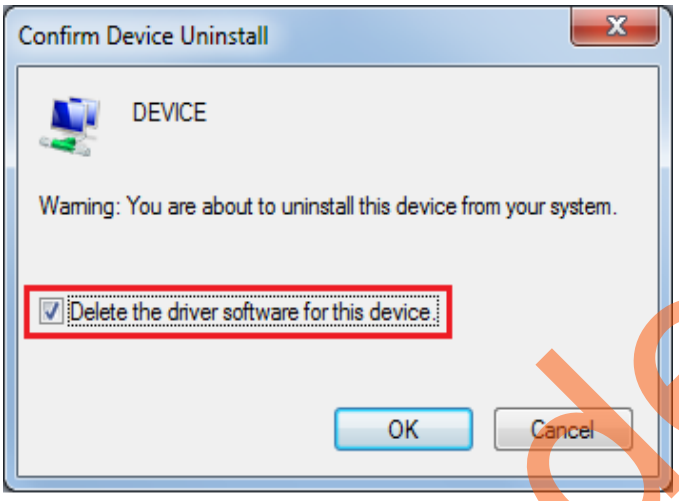

Figure 10 • **Selecting Delete the Driver Software for this device** check box in **Confirm Device Uninstall Dialog**

Drivers Installation

The PCIe Demo uses a driver framework provided by Jungo WinDriverPro. The following steps describe how to install the PCIe drivers on Host PC:

1. Extract the PCIe_Demo.rar to C:\ drive. The PCIe_Demo.rar is located at:
   <Download Folder>M2S_PCIe_MSSHPDMA_SMCFIC_DF\PCIE_DMA_DEMO_DF\Drivers_64bitOS\PCIe_Demo.rar
2. Run the batch file Jungo_KP_install.bat located at C:\ PCIe_Demo\DriverInstall\

Note: Installing these drivers require administration rights.

3. If the **Windows Security** dialog appears asking if to install or not, click **Install**. Figure 11 shows the Jungo Driver Installation in the **Windows Security** dialog.

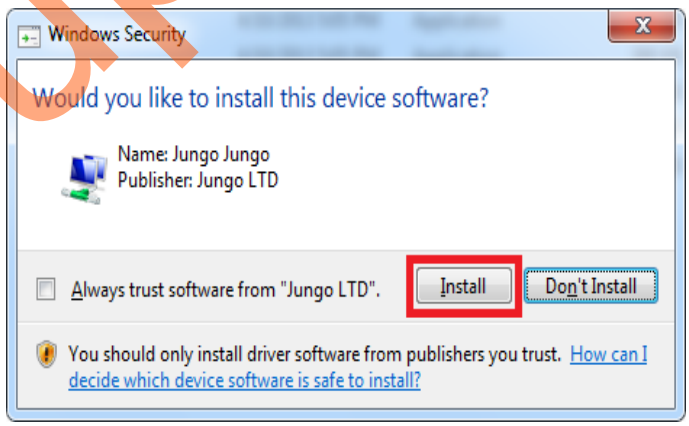

Figure 11 • **Jungo Driver Installation**

Note: If the installation fails, invoke the command prompt in administrator mode and run the batch file Jungo_KP_install.bat located at C:\PCIe_Demo\DriverInstall\

4. If the **Windows Security** dialog appears asking whether to install or not, click **Install this driver software anyway**.

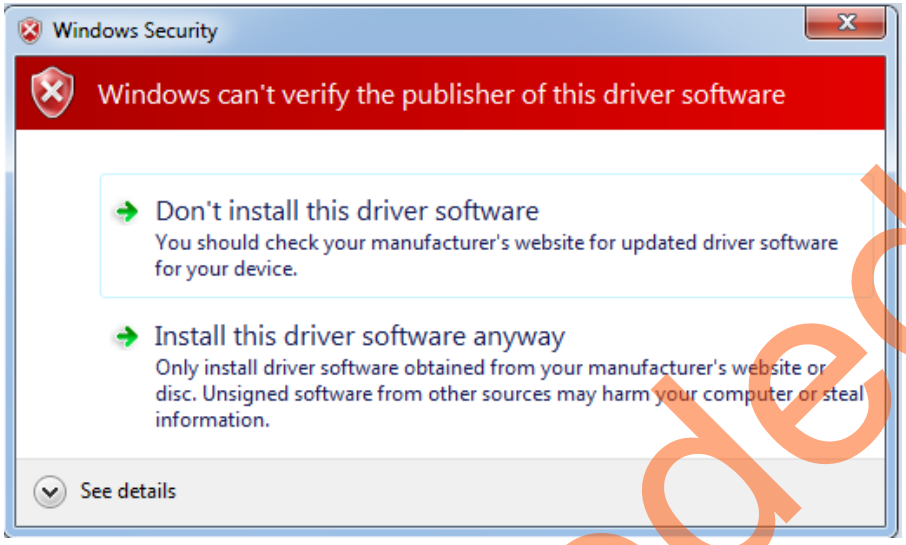

Figure 12 • **Windows Security Dialog**

PCIe_Demo Application

The PCIe_Demo application is a simple graphic user interface that runs on the Host PC to communicate with the SmartFusion2 PCIe endpoint device. It provides PCIe link status, driver information and demo controls. The PCIe_Demo application invokes the PCIe driver installed on the Host PC and provides commands to the driver according to the selection made. To install the PCIe_Demo application:

1. Go to <Download Folder>M2S_PCIe_MSSHPDMA_SMCFIC_DF\GUI\PCIe_Demo_GUI_Installer\ and double click **setup**. Do not change the default options and click **Next**.

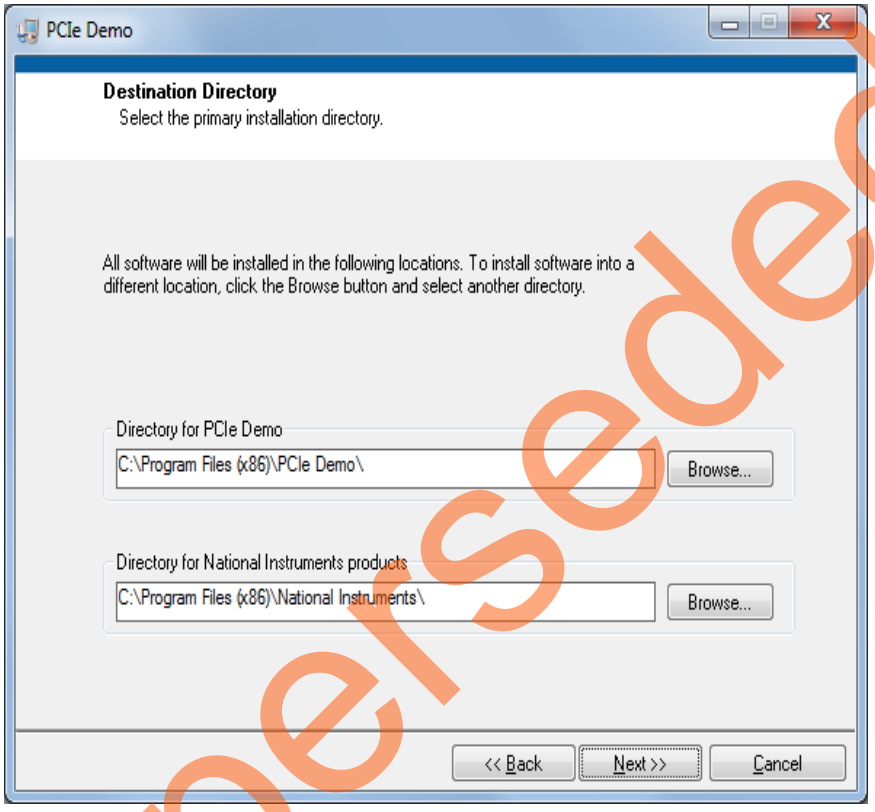

Figure 13 • **Installing PCIe_Demo Application**

2. Click **Next** to start the installation.

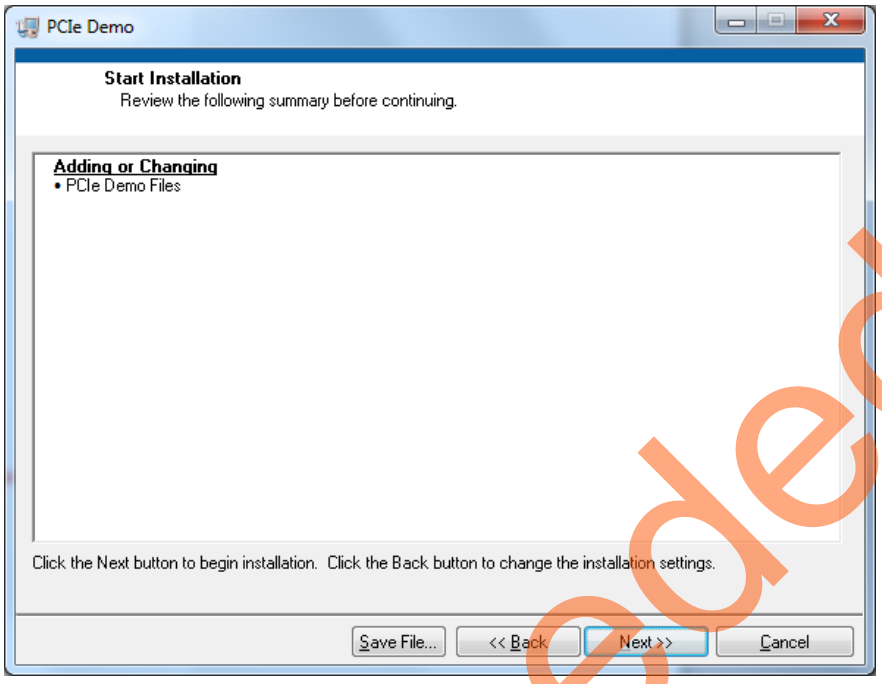

Figure 14 • **PCIe_Demo Application Installation Steps**

3. Click **Finish** to complete the installation.

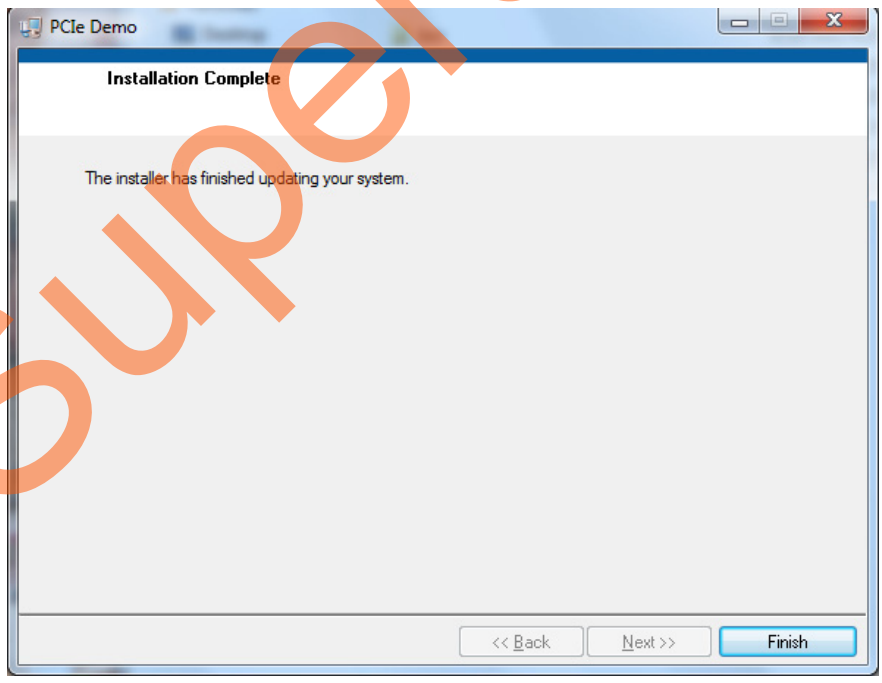

Figure 15 • **Successful Installation of PCIe_Demo Application**

4. Shut down the Host PC
5. Power Cycle the SmartFusion2 Development Kit.
6. Restart the Host PC.

Running the Design

1. Check the Host PC **Device Manager** for the drivers. Figure 17 shows the **Device Manager** window highlighting the Jungo drivers installed.

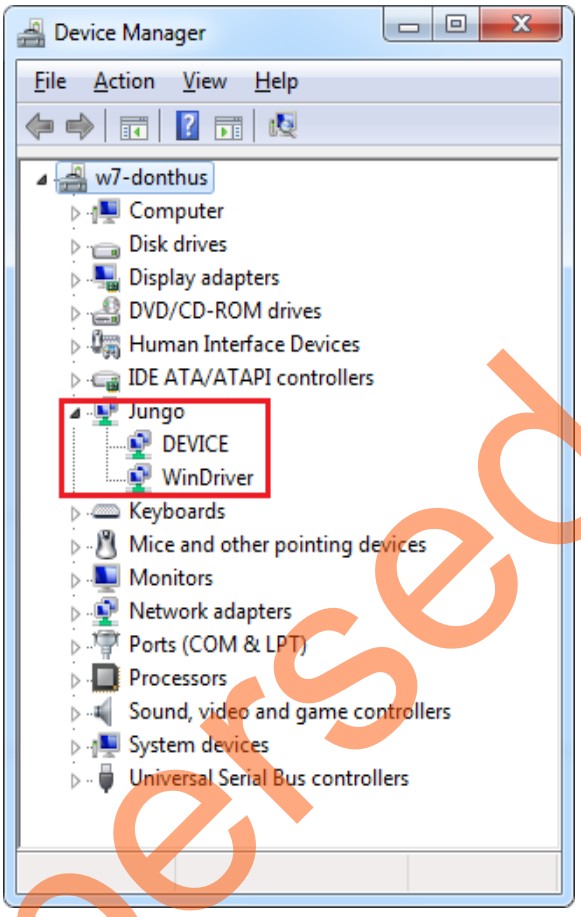

Figure 16 • **Device Manager - PCIe Device Detection**

2. If the device is not detected, power cycle the SmartFusion2 Development Kit Evaluation Kit and click **scan for hardware changes** in **Device Manager** window.

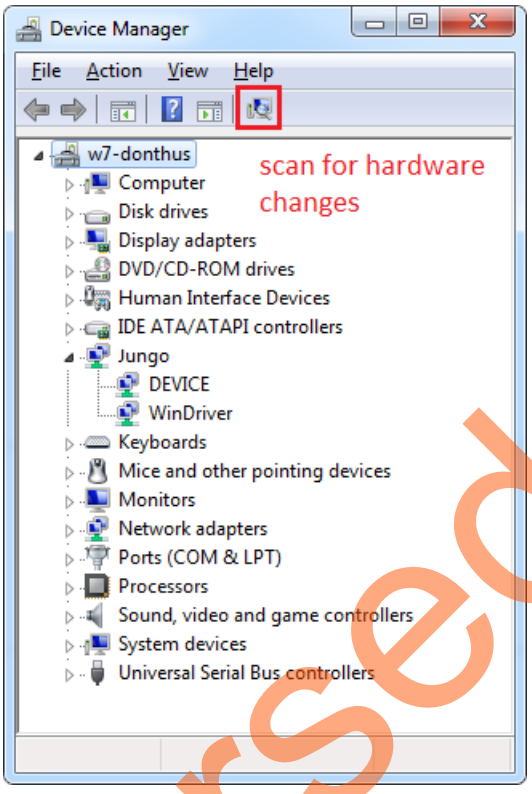

Figure 17 • **Scan for hardware changes** option in the **Device Manager** window

Note: If a warning appears on the DEVICE or WinDriver in the **Device Manager** window, uninstall the drivers and start from step1 of driver installation.

3. Invoke the PCIe_Demo application from **ALL Programs > PCIe Demo > PCIe Demo GUI**. Figure 18 shows the PCIe_Demo launch window.

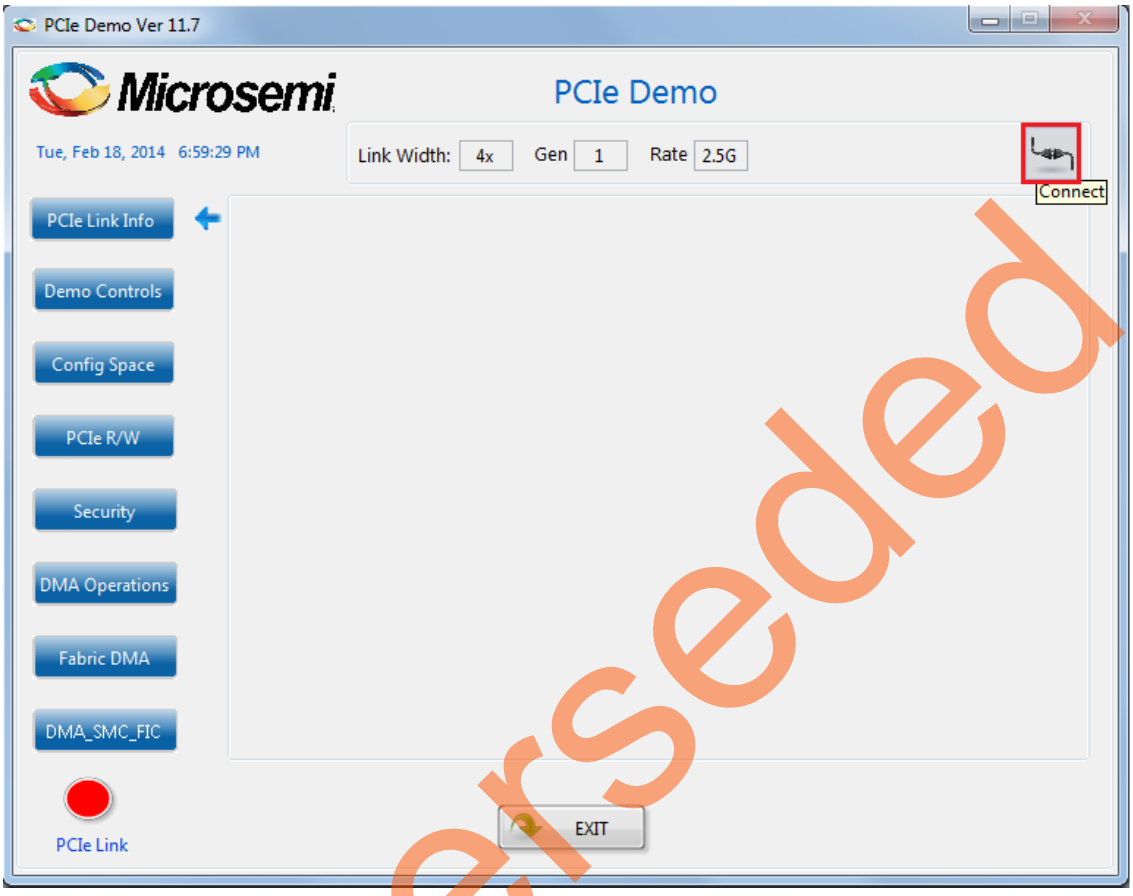

Figure 18 • **PCIe_Demo Application**

4. Click **Connect** at top right corner of the PCIe_Demo application. The application detects and displays the connected kit, demo design and PCIe link. Figure 19 shows the sample messages after the connection is established.

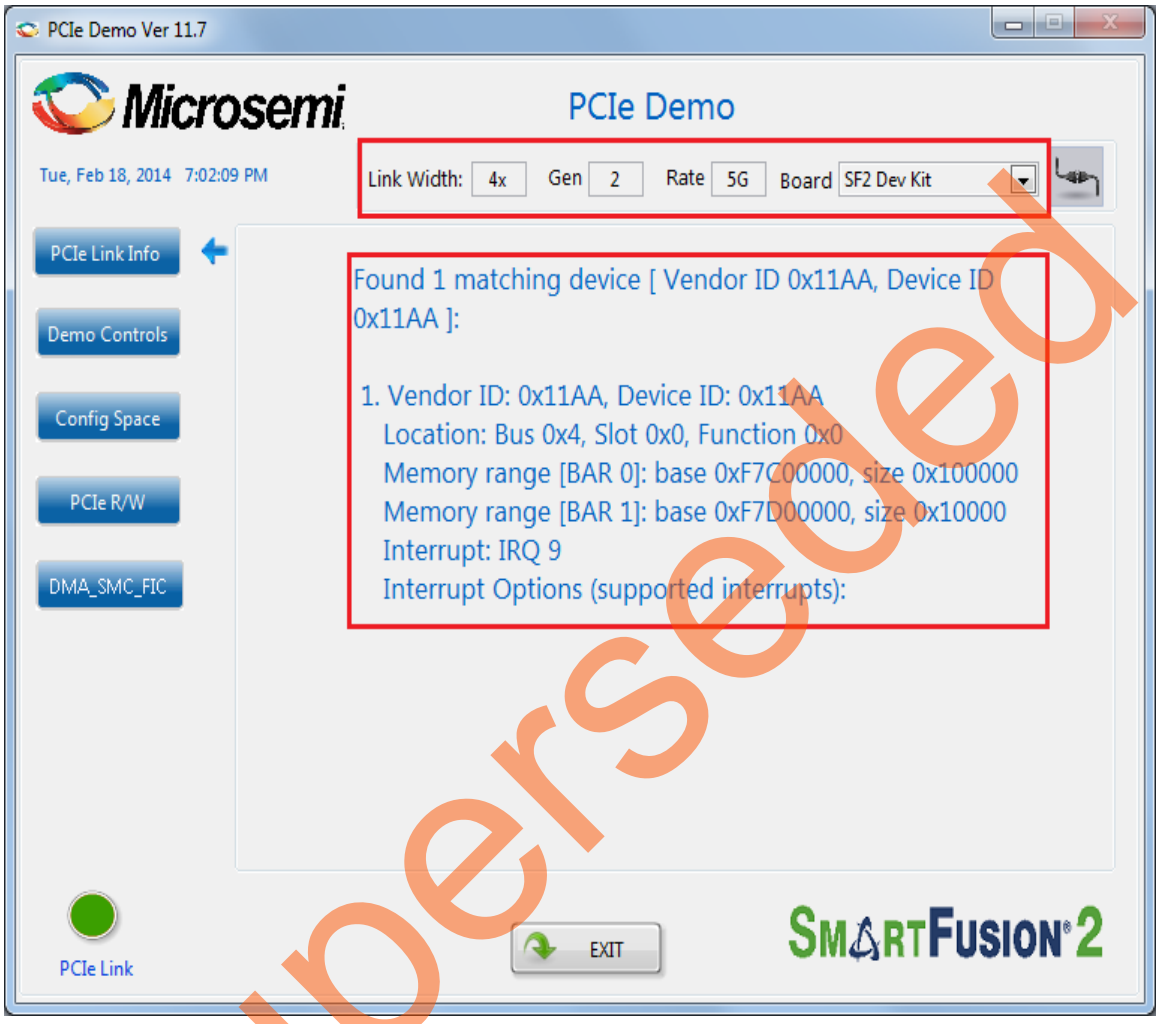

Figure 19 • **PCIe Device Information**

5. Click **Demo Controls** to display the LEDs options and DIP switch positions.Figure 20 shows the LED options and DIP switch positions in **Demo Controls**.

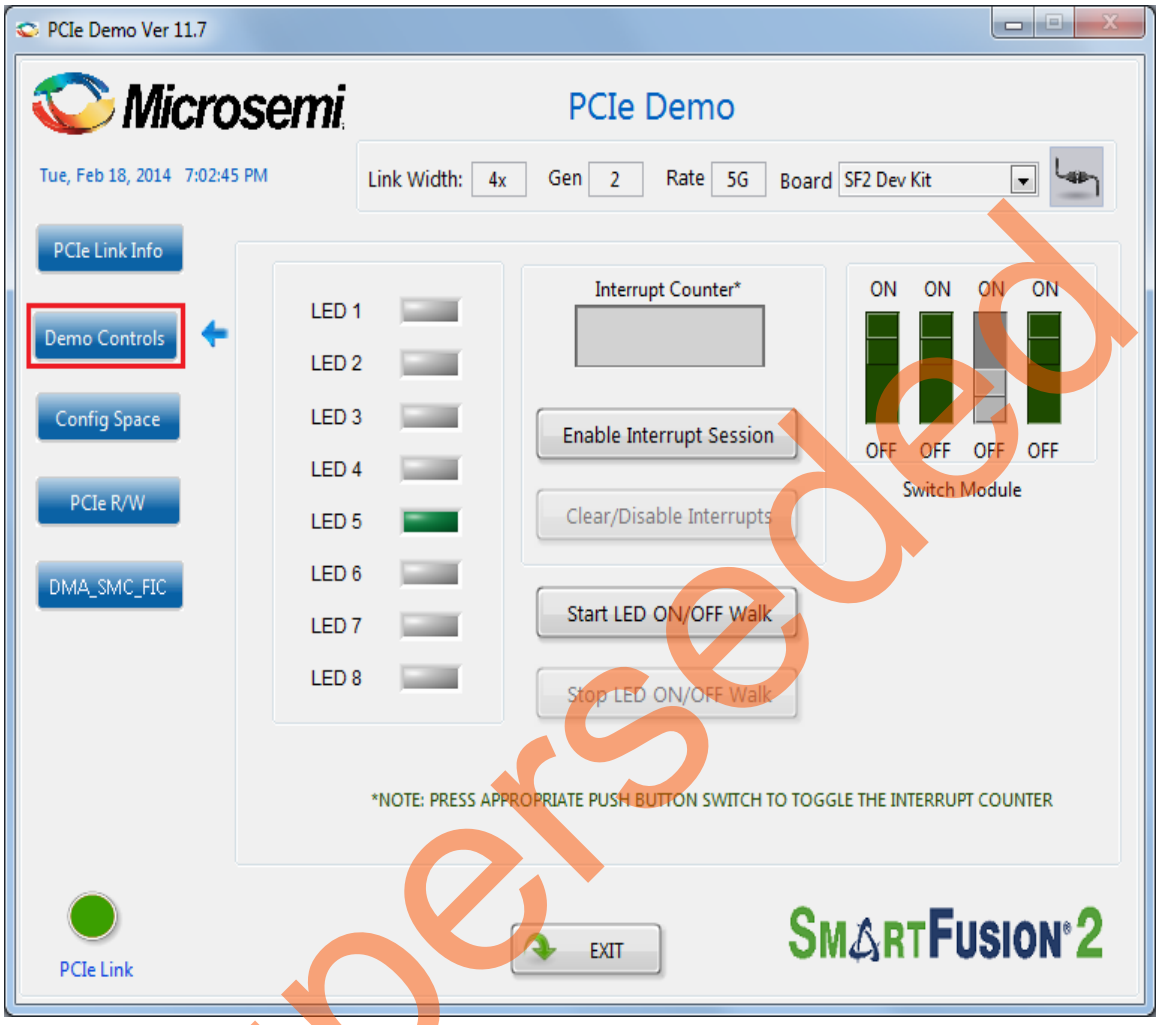

Figure 20 • **LED Options and DIP Switch Positions in Demo Controls**

6. Click **LEDs** to switch **ON** or **OFF** the LEDs on the board.
7. Click **Start LED ON/OFF Walk** to blink the LEDs on the board.
8. Click **Stop LED ON/OFF Walk** to stop the LEDs blinking.
9. Change the DIP switch positions on the board and observe the same reflected in the switches of the **Switch Module** of the PCIe_Demo application.
10. Click **Enable Interrupt Session** to enable the PCIe interrupt.

11. Press the push button, SW3 on the SmartFusion2 Development Kit board. Observe the interrupt count on the **Interrupt Counter** field in the PCIe_Demo application. Figure 21 shows the **Interrupt Counter** field in PCIe_Demo application.

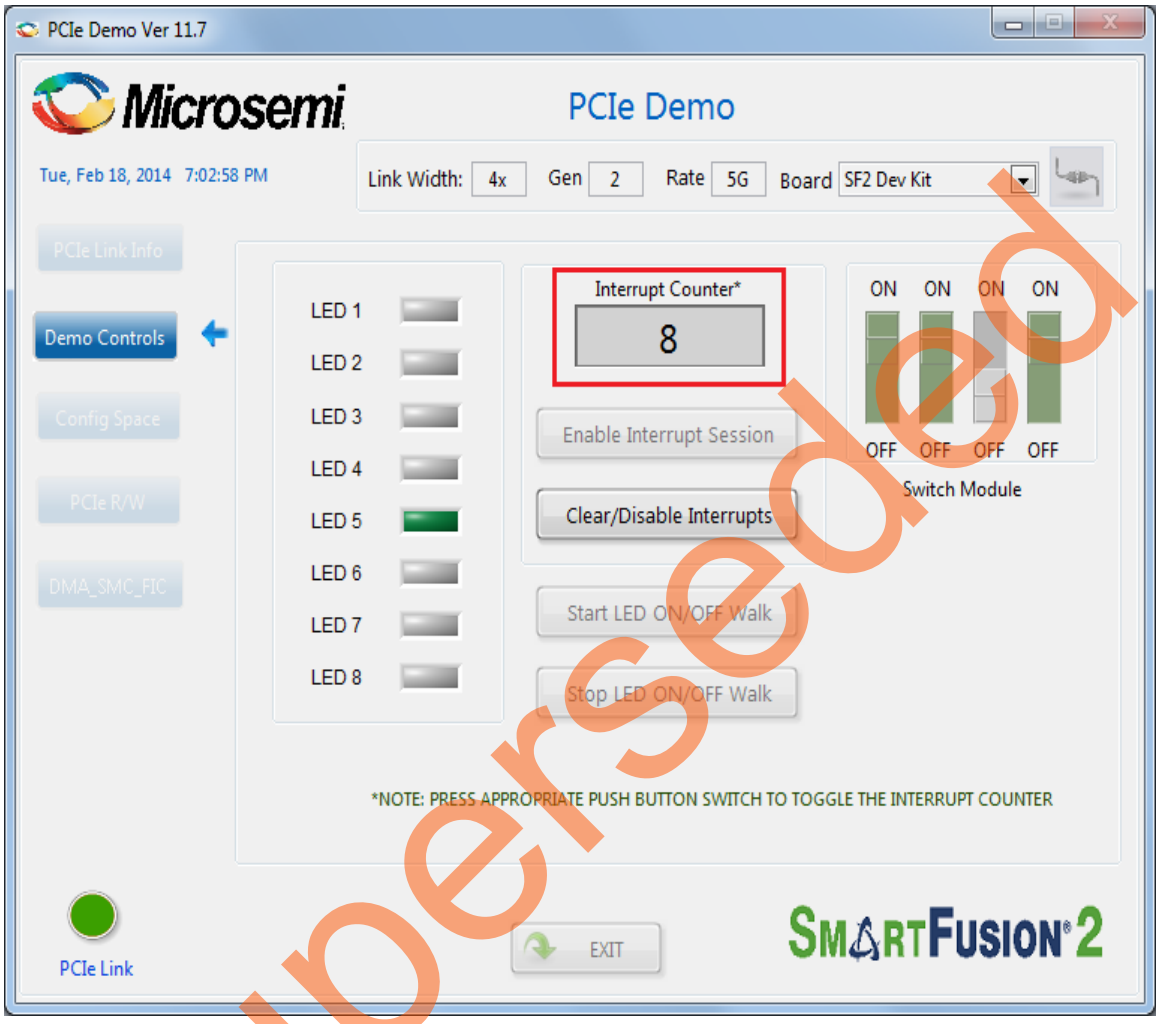

Figure 21 • **Interrupt Counter Field in PCIe_Demo Application**

12. Click **Clear/Disable Interrupts** to clear/disable the PCIe interrupts.

13. Click **Config Space** to see the details about the PCIe configuration space. Figure 22 shows the PCIe configuration space details.

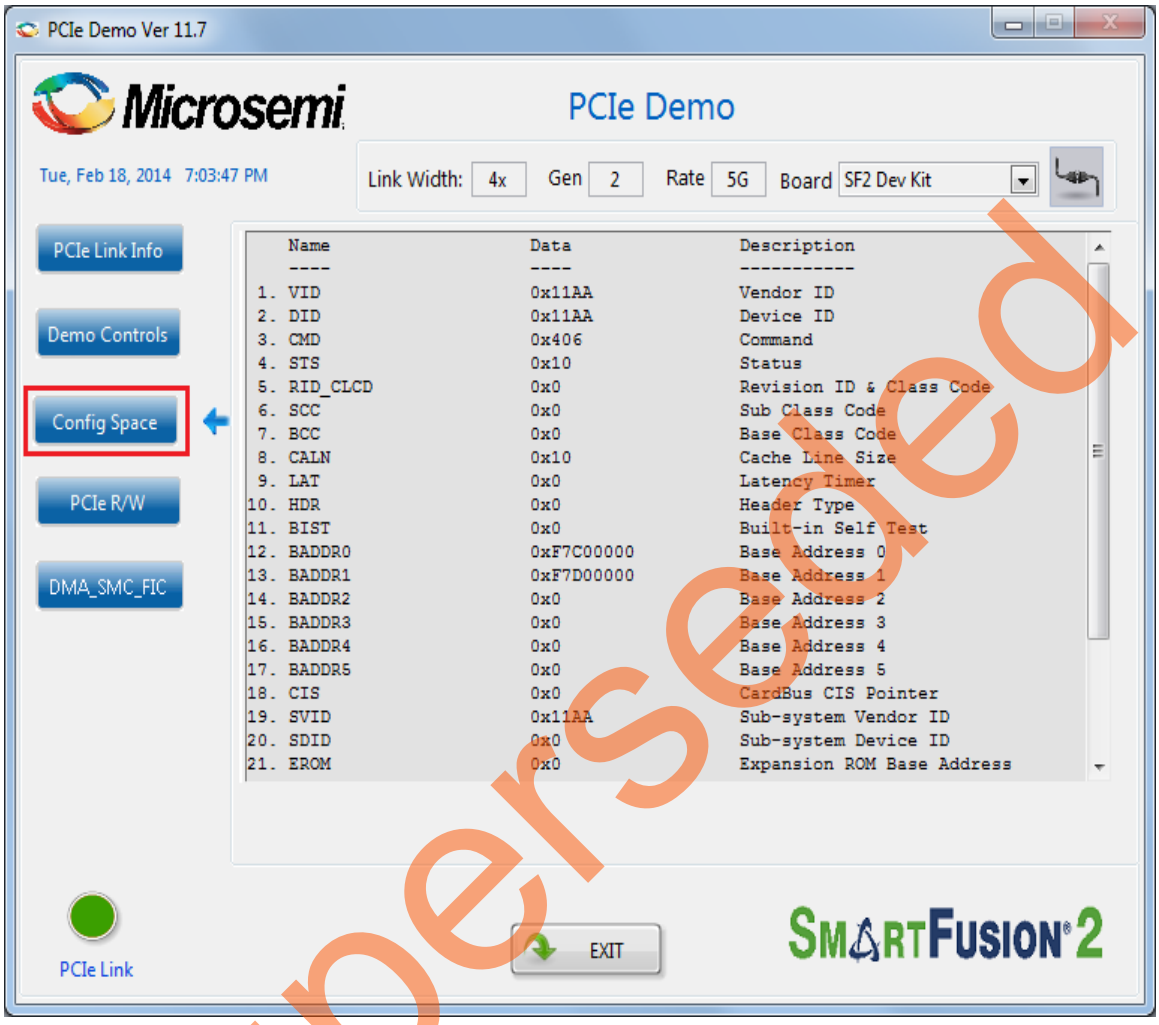

Figure 22 • **PCIe Configuration Space Details**

14. Click **PCIe R/W** to execute read and writes to a 32-bit scratchpad register through BAR1 space. Figure 23 shows the PCIe R/W panel.

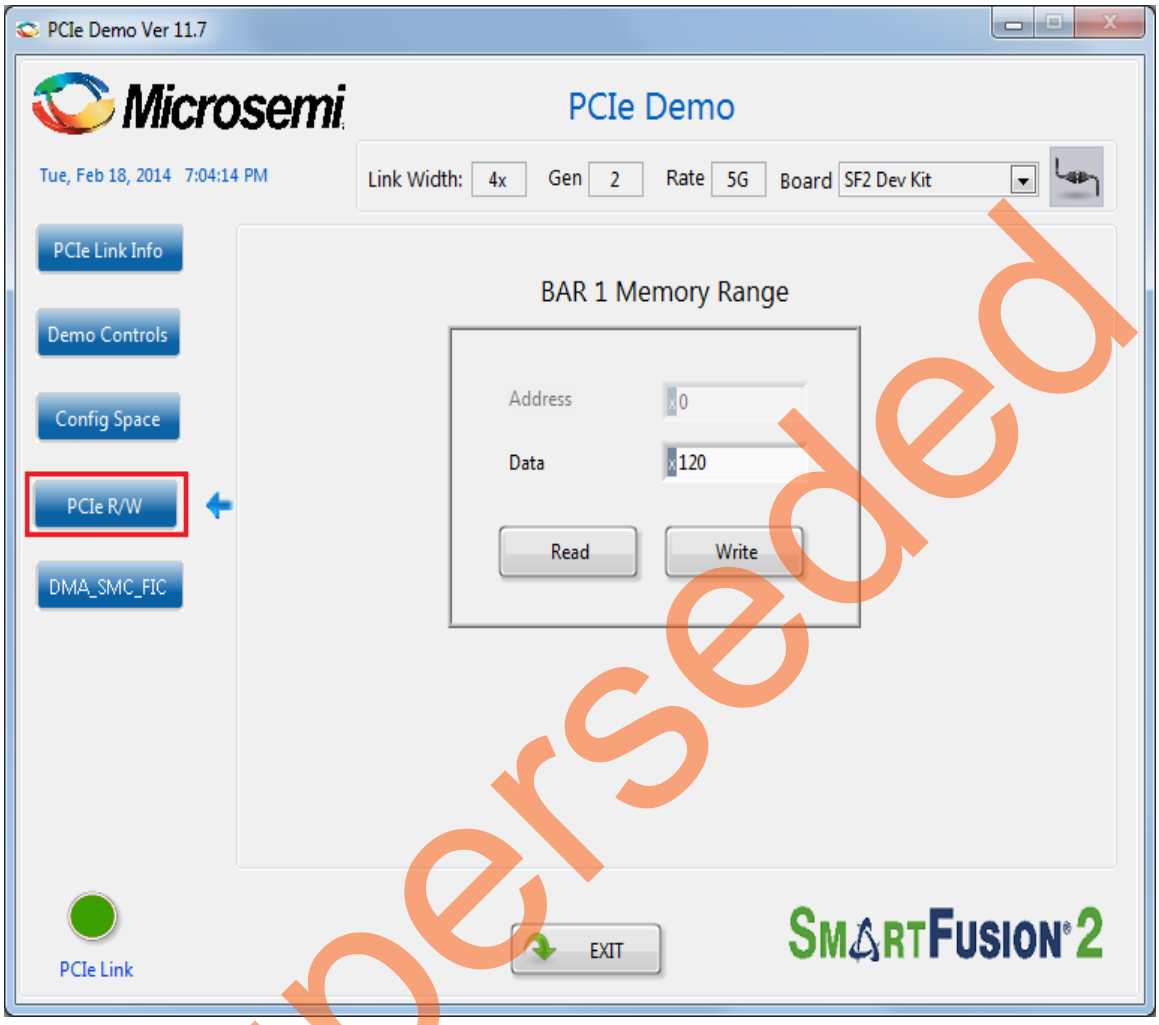

Figure 23 • **Read and Writes to Scratchpad Register**

15. Click **DMA_SMC_FIC** to run the DMA operations. Two types of DMA transactions are possible:
    - PC Memory to eSRAM
    - eSRAM to PC Memory

    For each operation, **Transfer Size** can be selected from 8KB to 32KB as shown in Figure 24. It also has a **Loop Count** field to run the DMA operation in loop.The Burst Size (TLP size) is fixed to 32 bytes to match the DDR bridge buffer size. The actual size of the PCIe packet is the size of a single AXI burst transfer which is 32 bytes.

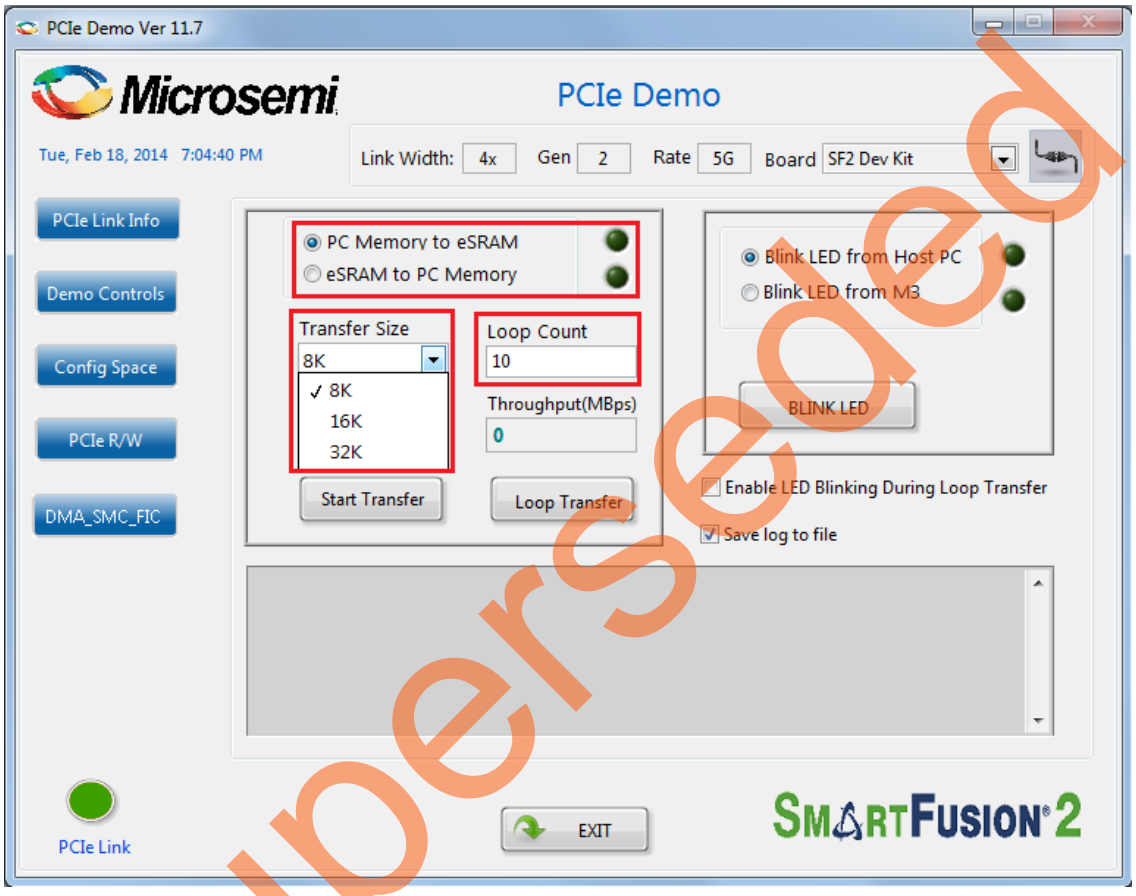

Figure 24 • **Fabric DMA Controls**

16. Select the type of DMA transfer as PC Memory to eSRAM and select 32K **Transfer Size**.
17. Click **Start Transfer**. Figure 25 shows the DMA Transactions between Host PC Memory and eSRAM.

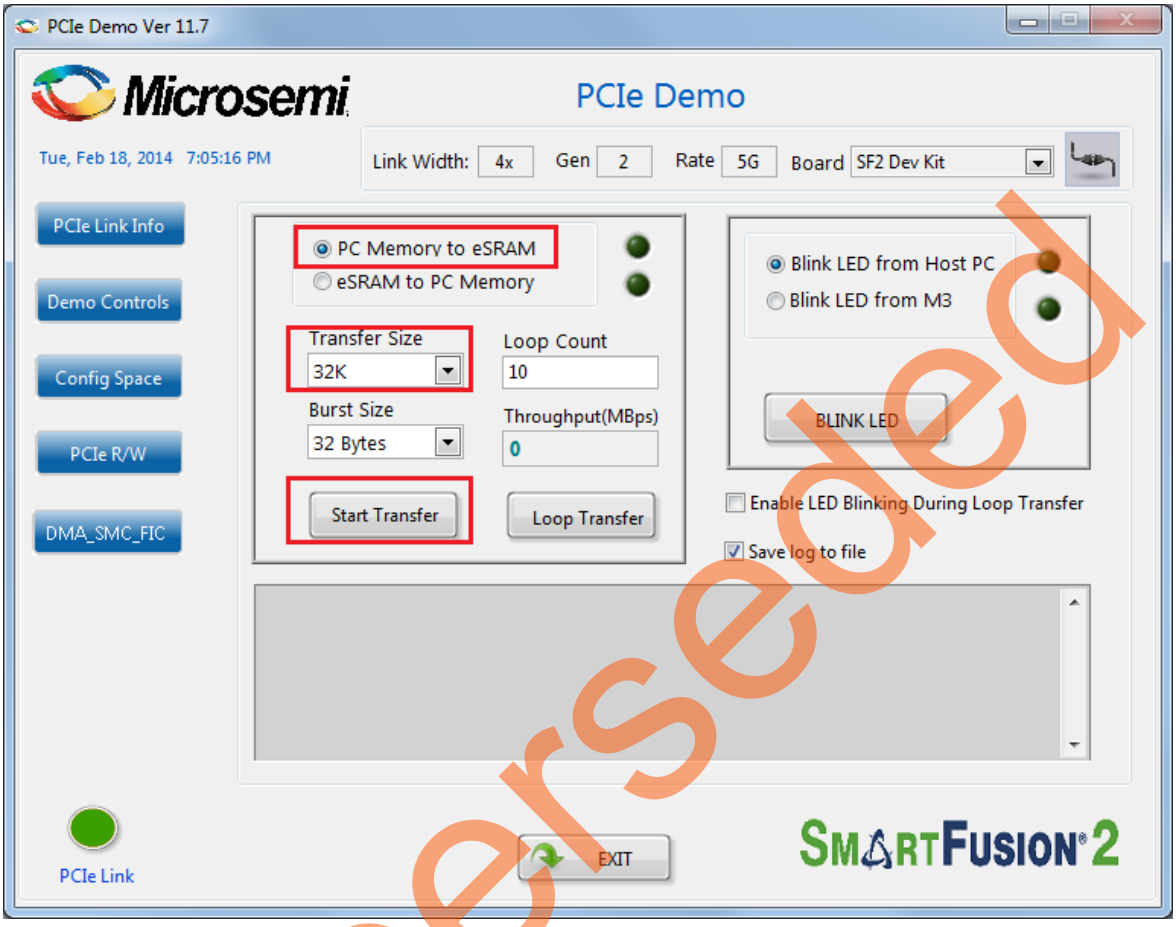

Figure 25 • **DMA Transactions between Host PC Memory and eSRAM**

18. After completion of data transfer, the throughput is displayed. Figure 26 shows the throughput in the DMA transactions from the Host PC to eSRAM.

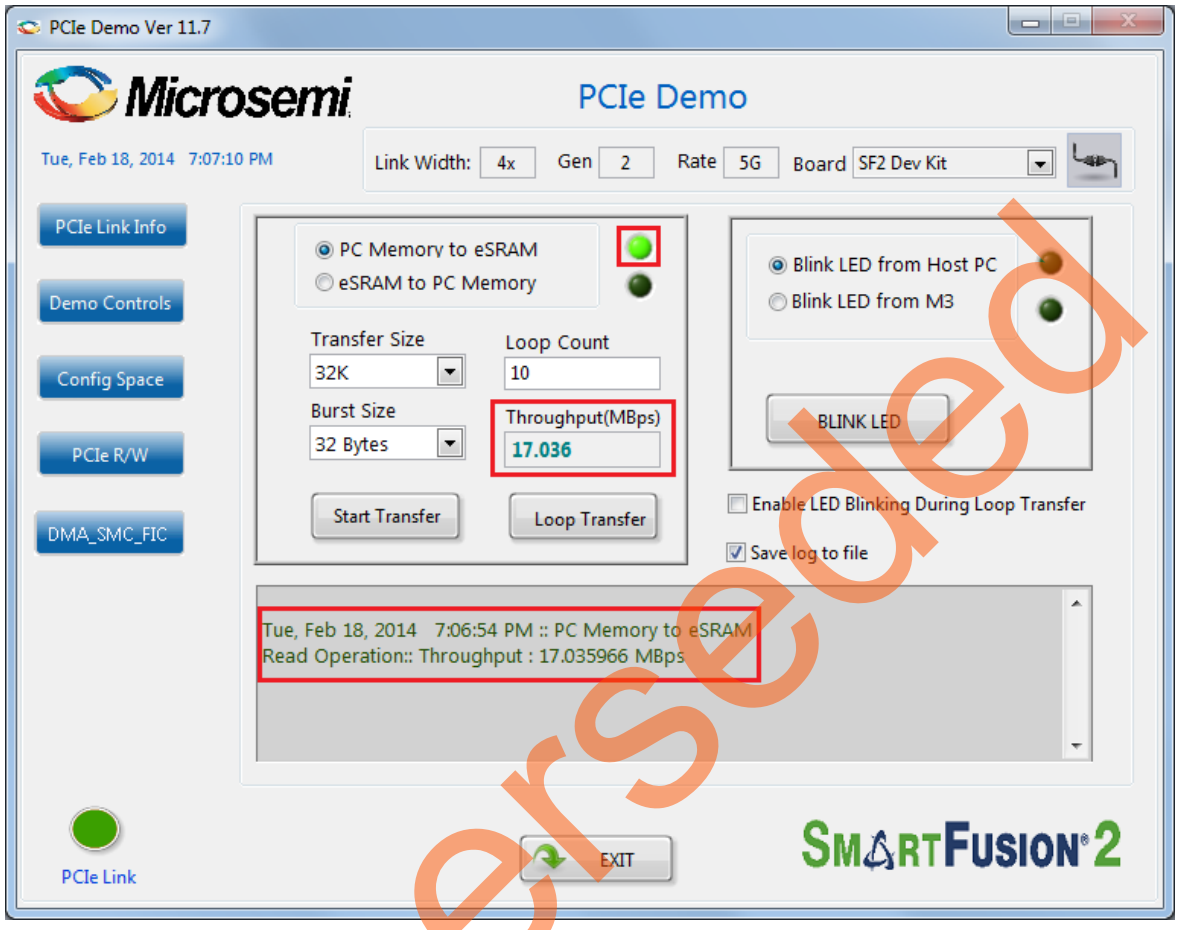

Figure 26 • **Throughput in DMA transactions from Host PC to eSRAM**

19. Enter 10 in the **Loop Count** field and click **Loop Transfer** to perform 10 sequential DMA transactions. After completion of data transfer, the PCIe_Demo application displays the throughput. Figure 27 shows the throughput in DMA transactions from Host PC to eSRAM. The average throughput is also logged. The log file is stored in the Host PC at C:\PCIe_Demo\DriverInstall.

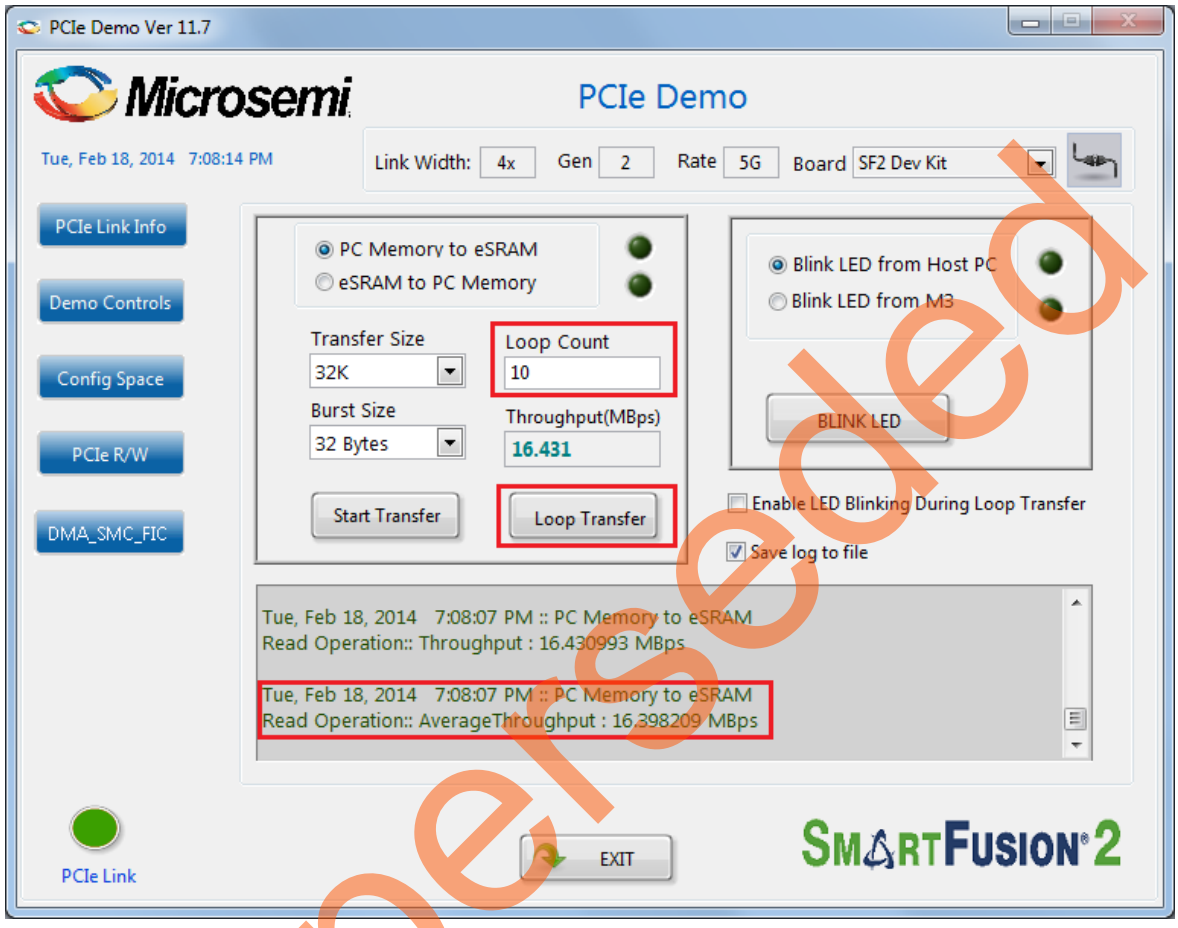

Figure 27 • **Throughput in the DMA Transactions from the Host PC to eSRAM**

20. Select the type of DMA transfer as eSRAM to PC Memory and select 32K Transfer Size. Click **Start Transfer** to perform a single DMA transaction. After completion of data transfer, the throughput is displayed. Figure 28 shows the throughput in the DMA transactions from eSRAM to the Host PC.

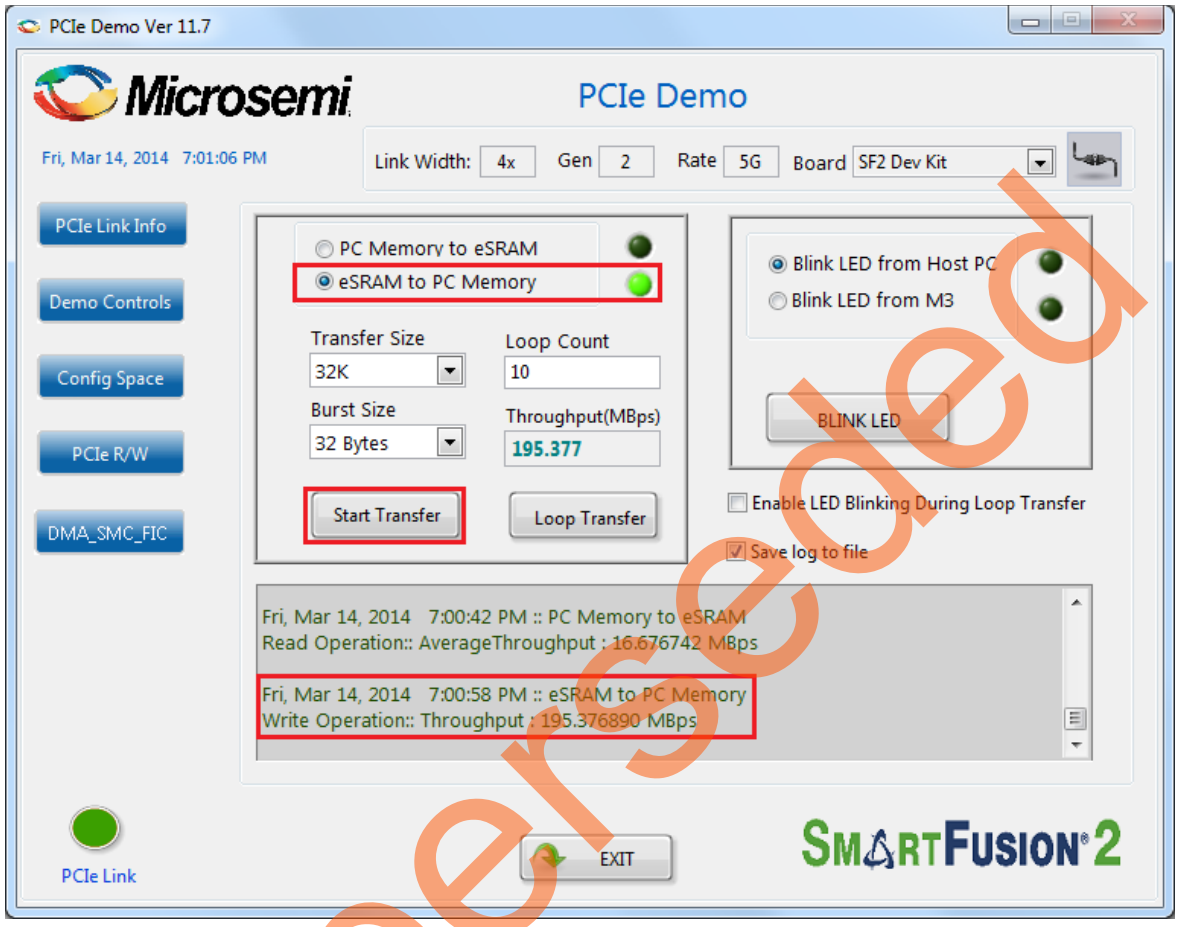

Figure 28 • **Throughput in the DMA Transactions from eSRAM to the Host PC**

21. Enter 10 in the **Loop Count** field and click **Loop Transfer** to perform 10 repeated DMA transactions. After completion of data transfer, the throughput is displayed. Figure 29 shows the throughput in the DMA transactions from eSRAM to the Host PC.

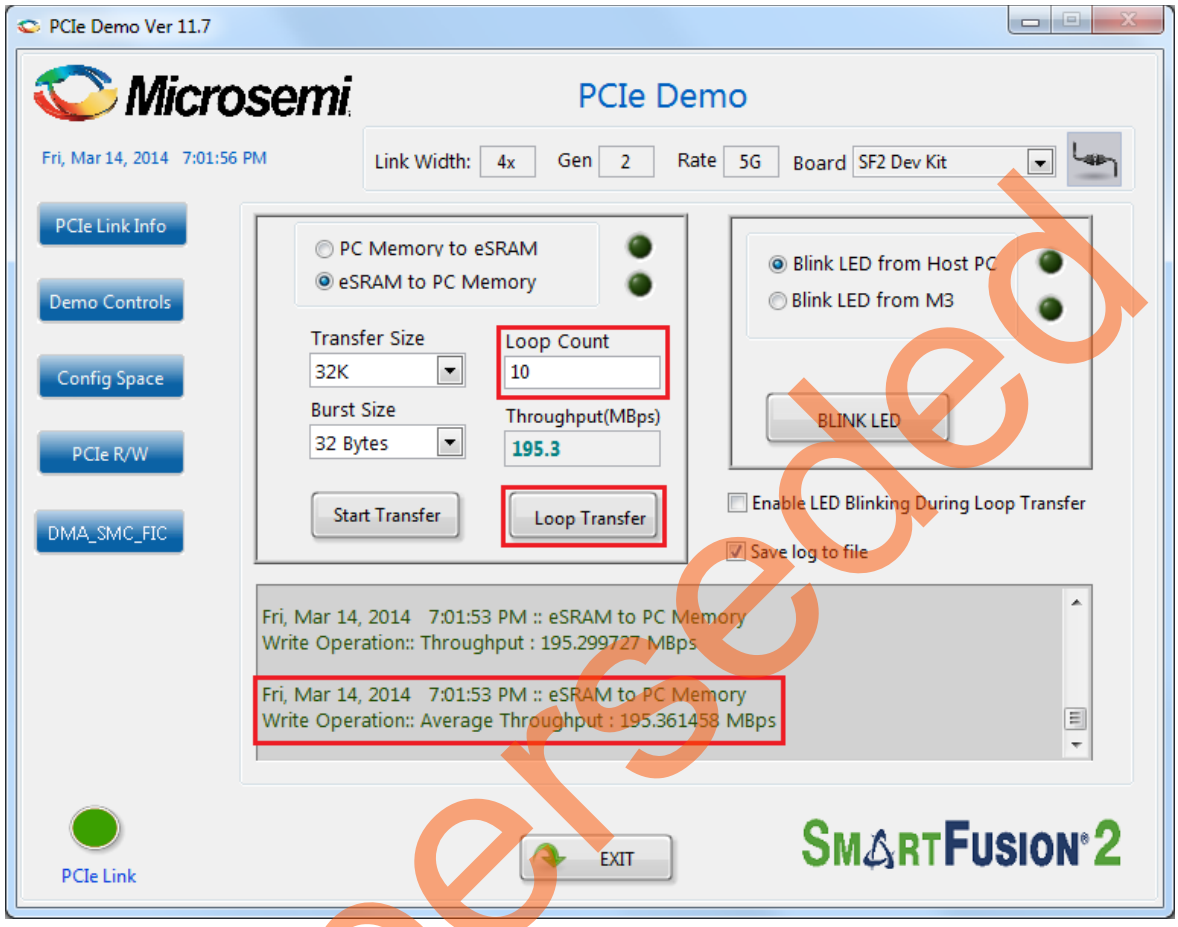

Figure 29 • **Throughput in the DMA Transactions from eSRAM to the Host PC**

The LEDs on the board can be blinked in parallel to the DMA operations by using the LED controls on the right side of GUI. The **Enable LED Blinking During Loop Transfer** check box need to be selected to do the LED blinking from Host PC and DMA transfers.

22. Click **Exit** to quit the demo.

Summary

This demo shows how to implement a PCIe Data Plane Design using MSS HPDMA and SMC_FIC. Data transfer occurs between PCIe and SmartFusion2 eSRAM. Throughput for data transfers is dependent on Host PC system configuration, type of PCIe slots used. Table 3 shows the throughput values observed on the Dell Optiplex 9020 PCIe slot 4.

Table 3 • **Throughput Summary**

DMA Transfer Type	DMA Transfer Size	Throughput (MBps)			
		Gen 1		Gen 2	
		Single Transfer	Loop Transfer	Single Transfer	Loop Transfer
Host PC Memory to eSRAM	8KB	6	6	16	16
	16KB	6	6	16	16
	32KB	6	6	16	16
eSRAM to Host PC Memory	8KB	136	136	195	195
	16KB	136	136	195	195
	32KB	136	136	195	195

Appendix 1: Register Details

Table 4 shows the registers used to interface with the PCIe MSS HPDMA SMC_FIC Design. These registers are in BAR1 address space.

Table 4 • **Register Details**

Register Name	BAR Space	Register Address	Description
PC_BASE_ADDR	BAR 1	0x8028	Host PC memory base address provided by the driver
DMA_DIR	BAR 1	0x8008	DMA direction **Direction** / **Register value** eSRAM to PCIe / 0x11AA1111 PCIe to eSRAM / 0x11AA2222
DMA_SIZE	BAR 1	0x8010	Size of DMA transfer **Size** / **Register value** 8KB / 0x2000 16KB / 0x4000 32KB / 0x8000
DMA_CLK_CYCLES	BAR 1	0x8018	Number of clock cycles taken to complete the DMA transfer.
DMA_STATUS	BAR 1	0x8020	1: DMA transfer completed 0: DMA transfer is not completed
BLINK_M3	BAR 1	0x8030	Blinks the LEDs from Cortex-M3 if the register value is 0x11AA0F0F
RW_REG	BAR 1	0x0	Scratchpad register for PCIe R/W
LED_CTRL[7:0]	BAR 0	0x13088	LEDs control register
SWITCH_STATUS[11:8]	BAR 0	0x13080	DIP switch status

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