LVPECL to HCSL Conversion Circuit

Introduction

LVPECL and HCSL signals have similar nominal signal swings of between 0.65 and 0.85 Vpp (single-ended). However they are biased to different levels. Typical 3.3V LVPECL signals are biased to 2.0V, for example, while HCSL signals are biased to 0.35V. The circuits in Figures 1 and 2 below can be used to passively convert an AC-coupled LVPECL signal to an HCSL signal. This can be used, for example, to interface a Microsemi LVPECL clock buffer output to an HCSL receiver such as a PCIe clock reference.

Conversion Circuits

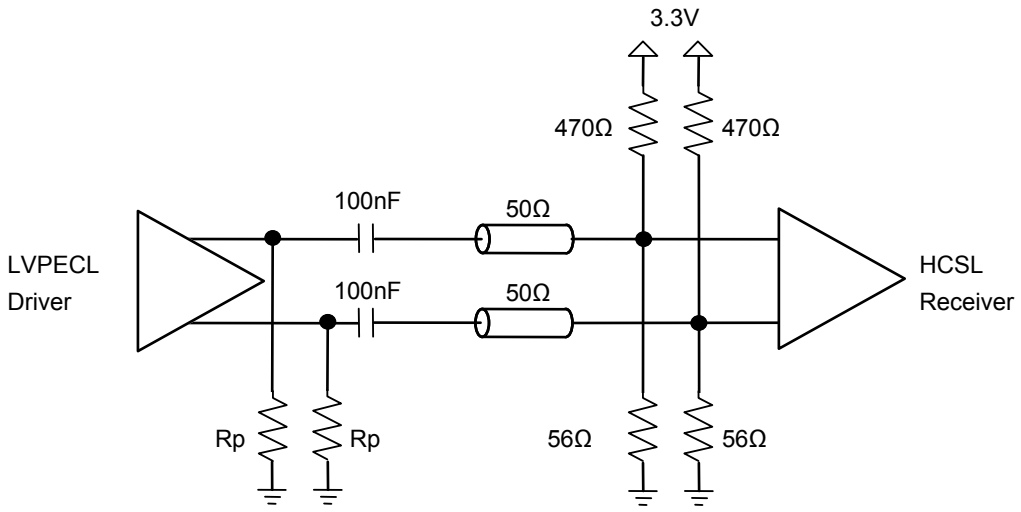

Figure 1 · LVPECL to HCSL Conversion Circuit with 3.3V Power Supply

Figure 1 shows the conversion circuit for the case in which the termination circuit is connected to a 3.3V supply. The 470Ω resistor in parallel with the 56Ω resistor provides a 50Ω termination resistance to match the 50Ω transmission line, which prevent reflections of the signal back to the transmitter. Additionally, the 470Ω in series with the 56Ω works as a voltage divider which sets the DC bias point of the receiver at 0.35V. Rp is the pull down resistance recommended for the LVPECL driver. In the case of a Microsemi clock buffer with a 3.3V supply, Rp is 120Ω. For a Microsemi clock buffer with a 2.5V supply, Rp is 60Ω.

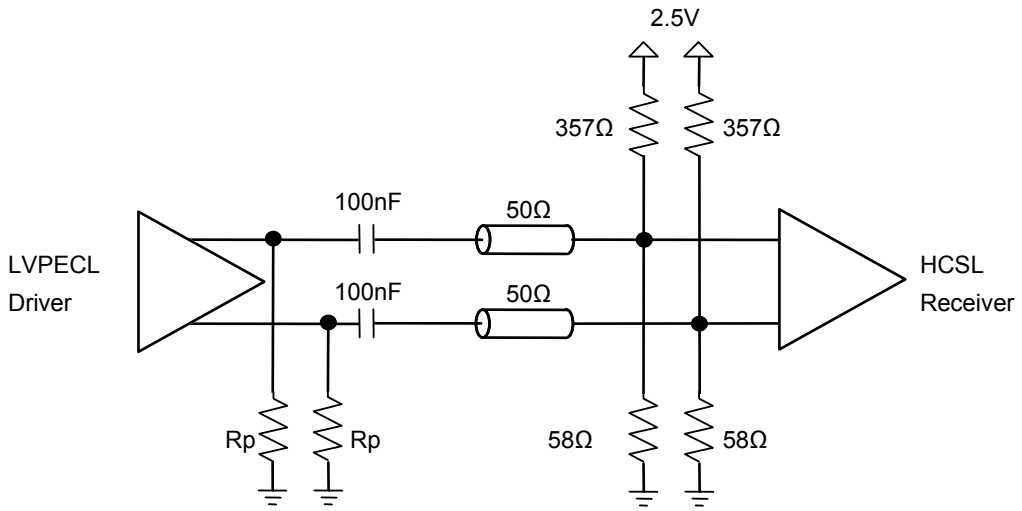

Figure 2 · LVPECL to HCSL Conversion Circuit with 2.5V Power Supply

Figure 2 shows the conversion circuit for the case in which the termination circuit is connected to a 2.5V supply. In this case, the 357Ω resistor in parallel with the 58Ω resistor provides a 50Ω termination resistance to match the 50Ω transmission line. The voltage divider created by the 357Ω resistor in series with the 58Ω resistor sets the DC bias point of the receiver at 0.35V. As in Figure 1, Rp is the pull down resistance recommended for the LVPECL driver.

Note that for both circuits, it is assumed that the HCSL receiver has high impedance inputs, and that no bias point has been set internally by the device. If the LVPECL signal swing is larger than 0.7Vpp, series resistors can be placed at the outputs of the LVPECL buffer to attenuate the signal to the desired level. It is good practice to perform IBIS simulations using the driver and receiver models to confirm signal integrity at the receiver.

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