

Release Notes For ModelSim ME 10.3a

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Key Information

- The following lists the supported platforms:
 - win32acoem Windows XP, Windows 7
 - linuxacoem RedHat Enterprise Linux 5 and 6, SUSE Linux Enterprise Server 10 and 11

Compatibility Issues with Release 10.3a

User Interface Compatibility

dvt64978 - (results) Setting the MODELSIM environment variable from within vsim or a
vsim [do] file, would not work correctly; the new setting would not take effect in all
cases. This has been fixed and will now update the simulator and GUI settings
appropriately from the new modelsim.ini file selected by the MODELSIM environment
variable. This change as the potential to effect existing [do] scripts that set this variable.

VHDL Compatibility

dvt64565 - (results) Now instances under VHDL generates can be specified as the SDF back-annotation point with -sdfmin/typ/max switches. For example, "-sdfmax /test/gen_buf1_inst(1)/wrap_buf1_inst=test.sdf", where instance "wrap_buf1_inst" is under the VHDL generate "gen_buf1_inst", now annotates successfully. Now VHDL and Verilog generate scopes (e.g. /test/gen_buf1_inst(1) above) are also accepted.



- dvt65205 (results) The simulation times reported by -printsimstats option to vsim would be incorrect if the simulation is terminate by a call to std.env.finish in VHDL. The simstats command from within the simulator results are correct.
- dvt35802 (results) In certain signal assign statements with indexes out of bounds proper
 error messages were not issued in vopt mode but were issued correctly in novopt mode.
 We will now be giving a suppressible warning for such cases in vopt mode. This can be
 changed to an error by using the -pedanticerrors switch for strict LRM compliance.

Coverage Compatibility

 dvt38061 - (results) HTML report bydu coverage items under function scopes were incorrect.

General Compatibility

• [nodvtid] - (results) The implementation of the VPI object model for GenScope, GenScopeArray, and the associated NamedBegin has been modified slightly to align better to the SystemVerilog LRM. Multiple generated scopes from a generate statement now have scope type vpiGenScope (not vpiNamedBegin; there is no vpiNamedBegin scope reported as the vpiGenScope is considered a more specialized representation of the begin/end block). The GenScopeArray is no longer a member of the scope class but is a separate VPI object under the parental scope.

General Defects Repaired in 10.3a

- [nodvtid] (results) The implementation of the VPI object model for GenScope, GenScopeArray, and the associated NamedBegin has been modified slightly to align better to the SystemVerilog LRM. Multiple generated scopes from a generate statement now have scope type vpiGenScope (not vpiNamedBegin; there is no vpiNamedBegin scope reported as the vpiGenScope is considered a more specialized representation of the begin/end block). The GenScopeArray is no longer a member of the scope class but is a separate VPI object under the parental scope.
- dvt65360 A crash would occur when running wlf2vcd on VCD files that had verilog real objects.
- dvt65682 Launching applications from the installation bin directory would fail if the installation path contains any spaces. This issue has been resolved.

User Interface Defects Repaired in 10.3a

• dvt65001 - The PrefSource(tabs) setting is now supported for the new Source window. This preference value set the number of columns for a tab character in the source



- window. The value can be set from the Preferences dialog box under the By Name tab, or by using the Tcl command "set PrefSource(tabs) 8".
- dvt64978 (results) Setting the MODELSIM environment variable from within vsim or a
 vsim [do] file, would not work correctly; the new setting would not take effect in all
 cases. This has been fixed and will now update the simulator and GUI settings
 appropriately from the new modelsim.ini file selected by the MODELSIM environment
 variable. This change as the potential to effect existing [do] scripts that set this variable.
- dvt65471 Two preference variables were added to provide control of source window behavior when a source file is modified external to the source window.
 PrefSource(CheckModifiedFiles) controls if the source window checks for external file modifications. PrefSource(AutoReloadModifiedFiles) will automatically reload a file into a source window if it is modified outside of the source window.
- dvt38091 Export Image capability on Windows has been fixed.

VHDL Defects Repaired in 10.3a

- dvt64721 A signal external name appearing in a PROCESS statement, and whose subtype indication is not locally static, could result in a simulator crash when the design was loaded.
- dvt64737 A configuration declaration that has the same name as the ENTITY that it is configuring cannot be compiled into the same library as that ENTITY. Previously this was a compiler warning resulting in an unloadable design, but this has been changed into a compiler error.
- dvt64565 (results) Now instances under VHDL generates can be specified as the SDF back-annotation point with -sdfmin/typ/max switches. For example, "-sdfmax /test/gen_buf1_inst(1)/wrap_buf1_inst=test.sdf", where instance "wrap_buf1_inst" is under the VHDL generate "gen_buf1_inst", now annotates successfully. Now VHDL and Verilog generate scopes (e.g. /test/gen_buf1_inst(1) above) are also accepted.
- dvt65205 (results) The simulation times reported by -printsimstats option to vsim would be incorrect if the simulation is terminate by a call to std.env.finish in VHDL. The simstats command from within the simulator results are correct.
- dvt35802 (results) In certain signal assign statements with indexes out of bounds proper error messages were not issued in vopt mode but were issued correctly in novopt mode. We will now be giving a suppressible warning for such cases in vopt mode. This can be changed to an error by using the -pedanticerrors switch for strict LRM compliance.
- dvt65986 The compiler erroneously emitted a syntax error when encountering a
 concatenation expression in which one operand is an object whose type is an interface
 type. The compiler now supports concatenation of interface-typed objects.



WLF and VCD logging Defects Repaired in 10.3a

dvt62912 - VHDL implicit signals (such as those created internally by the simulator when encountering the use of To_StdLogicVector() in a port map declaration) used to be logged to the WLF file. These usually appeared as signals with names such as "s__34_15" when viewing the WLF file in post-simulation mode. These implicits are no longer logged to the WLF file.

General Enhancements in 10.3a

- [nodvtid] -stats option has been enhanced to have the following syntax:
- -stats[=[+-]< features and modes >]

Feature options are:

- o time: Display Start, End, and Elapsed times of the executable
- o cmd: Echo the command line
- o msg: Display error/warning summary at end of execution
- o perf: Display performance stats: CPU time, Wall time, and Memory use
- o all: All stats features are enabled
- o none: All stats features/modes are disabled

Mode options are:

- o verbose: Display verbose information when available
- o list: Display the stats in a Tcl list style

Following commands support this option:

o vlog, vcom, sccom, mc2com, vopt, vcover, vencrypt, vsim

'Stats' modelsim.ini variable is equivalent for this option and has the default value of time,cmd,msg:

```
[vlog/vcom/vopt/sccom/vsim]
Stats = time,cmd,msg
```

Few functionality notes:



- o time,cmd,msg features are default ON for all the above commands.
- o -stats without any argument is equivalent to time,cmd,msg.
- Command line option further add/remove features to/from the default feature settings.
- o Multiple -stats options are allowed in the command line, but only the last specified option will take effect.

Following options are obsolete and replaced by -stats option:

- o -nostats; replaced by -stats=none
- o -printstats; replaced by -stats=perf
- o -printsimstatslist; replaced by -stats=perf,list





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