IGLOO2 and SmartFusion2 65nm Commercial Flash FPGAs

Interim Summary of Radiation Test Results

October 21, 2014

I. Summary

A series of tests have been performed to evaluate the behavior of *SmartFusion2 SoC FPGAs* and *IGLOO2 FPGAs* in heavy ion and neutron radiation environments. Further tests are planned. The tests so far indicate that IGLOO®2 FPGAs and SmartFusion®2 SoC FPGAs will operate in a satisfactory manner in neutron radiation environments encountered in aviation and ground-level applications. For flight-critical applications, mitigation of data upsets in flip-flops and SRAM blocks is advisable. The tests indicate that the IGLOO2 FPGAs and SmartFusion2 FPGAs encounter non-destructive latch-ups in heavy ion radiation testing, at energy levels low enough to cause concern in low earth orbit (LEO) space applications. It should be noted that the SEL onset threshold is in excess of 20 MeV-cm^2/mg, and that single-event latch-ups have not been observed at energy levels relevant for aviation applications.

II. Background

Microsemi SmartFusion2 SoC FPGAs and IGLOO2 FPGAs are 65nm, non-volatile, flash-based, low power FPGAs. Their intrinsic robustness, high density, high-performance, and unprecedented wealth of features make these devices very appealing to designers of high reliability and safety critical applications; including aviation, industrial, medical, and carrier-class communication systems. Background radiation poses a significant reliability threat to high reliability systems at ground level, at aviation altitudes, and in space. In this report we examine the behavior of the SmartFusion2 SoC FPGAs and IGLOO2 FPGAs in neutron and heavy ion radiation environments. Most tests are performed on the SmartFusion2 (SF2) SoC FPGA M2S050 devices, however the results are applicable to IGLOO2 FPGAs as the two families share a common manufacturing process (65nm flash at UMC) and the same fundamental FPGA architecture.

III. Single Event Latch-Up

Fourteen units of SF2 M2S050 were exposed to heavy ion radiation in three separate test campaigns. The first two campaigns were conducted in March and April 2014 at Lawrence Berkeley National Laboratory (LBNL), where devices were exposed to a 10MeV nucleon cocktail in the facility's 88" Cyclotron. Radiation exposure was at room temperature. The third campaign was at Texas A & M University (TAMU) in April 2014, with devices exposed to a 15MeV nucleon cocktail at 100°C.

In total, 14 units were exposed to 1.07 x 10^9 fluence at linear energy transfer (LET) levels up to 30.86 MeV-cm^2/mg. Devices were monitored for any evidence of latch-up—functionality and current were continuously monitored and data-logged. The test records were thoroughly inspected after each campaign. The SEL LET threshold for maximum operating voltages at 100°C is determined to be higher than 22.5 MeV-cm^2/mg, and therefore the device will be immune to proton and neutron induced SEL.

Non-destructive single event latch-ups were encountered in heavy ion testing at energy levels of 24 MeV-cm^2/mg and higher, making the SmartFusion2 SoC FPGAs and IGLOO2 FPGAs unsuitable for space-flight applications.

The results are summarized in Table 1: Single Event Latch-Up Summary, and in Table 2: Breakdown of SEL Occurrences Versus LET, as shown on the next page.

Table 1: Single Event Latch-Up Summary

Run	Device Tested	Number of Parts Tested	Test Facility	Test Temperature	Total Test Fluence	Number of SEL Events LET <= 20	Number of SEL Events LET > 20
1	M2S050	3	LBNL	Room Temperature	2.20×10^8	0	0
2	M2S050	3	LBNL	Room Temperature	4.09×10^8	0	0
3	M2S050	8	TAMU	100°C	4.41×10^8	0	2
Total		14			1.07×10^9	0	2

Table 2: Breakdown of SEL Occurrences Versus LET

LET	3/20/2014 at LBNL Room Temp		4/16/2014 at LBNL Room Temp		4/28/2014 at TAMU 100°C	
	SEL Count	Fluence	SEL Count	Fluence	SEL Count	Fluence
0.89			0	3.60×10^7		
1.03			0	4.00×10^7		
2.19			0	4.60×10^7		
2.53			0	3.20×10^7		
3.49	0	2.00×10^7	0	5.40×10^7		
4.03			0	2.00×10^7		
6.09			0	3.90×10^7		
7.03			0	1.00×10^7		
9.74	0	2.00×10^7	0	4.90×10^7		
11.25			0	1.00×10^7		
14.59	0	4.00×10^7	0	3.60×10^7		
16.85			0	1.00×10^7		
20.20					0	2.70×10^8
21.17	0	4.00×10^7	0	2.70×10^7		
22.50					0	5.00×10^7
24.00					1	6.50×10^7
26.00					0	4.50×10^7
28.60					1	1.10×10^7
30.86	0	1.00×10^8				

IV. Configuration Single Event Upsets (SEU)

Safety critical and high reliability applications require FPGAs to retain their configuration in radiation environments. The preceding generations of Microsemi flash FPGAs (ProASIC®, ProASIC Plus®, ProASIC®3, IGLOO®, Fusion®, and SmartFusion®customizable SoC) have exhibited a complete absence of radiation-induced upsets in the flash cells which control the configuration of the FPGA.

This is in direct contrast to SRAM-based FPGAs, which exhibit single event upsets in the SRAM configuration memory that configures the function of logic cells and connects routing tracks together. These radiation-induced single event upsets cause the SRAM FPGAs to change their function and behave unpredictably. This effect occurs due to the background radiation encountered by satellite systems, airborne systems, and even in terrestrial ground-level systems. Mitigation of configuration upsets is complex and cumbersome, and moreover it is not wholly effective because the mitigation schemes work by overwriting a corrupted configuration bit with a correct configuration bit. The corrupted configuration bit will cause device malfunction from the occurrence of the single event until it is corrected—a period of at least several hundred milliseconds. During that time the corrupted device will have been performing unpredictably, pouring erroneous data into the system. A demonstrated absence of configuration upsets due to radiation is an essential property for FPGAs being deployed in high reliability and safety critical systems.

Forty-eight units of Microsemi M2S050 SmartFusion2 FPGAs were exposed to heavy ions at LET levels up to 90.3 MeV-cm^2/mg in ten separate test campaigns at Lawrence Berkeley National Laboratory (LBNL) and Texas A & M Cyclotron facility (TAMU). Functionality of the FPGAs was monitored continuously during radiation exposure. Any change in configuration due to radiation would have resulted in functional upset of the data path, non-recoverable by power cycling, requiring the flash array to be reprogrammed. No configuration upsets were detected in testing on a total of 48 parts in a total fluence of 2.83 x 10^9 heavy ions.

Configuration SEU results are presented in Table 3: below. Upper-bound FIT rates are shown in Table 4: Configuration Single Event Upset Boundary of FIT rates on page 4.

Table 3: Configuration Single Event Upset Summary

Facility	Device Tested	Date	Number Parts Tested	Total Test Fluence	Temp	Number of Configuration Upsets
LBNL	M2S050	4/14/2013	3	1.70 × 10^8	Room	0
		8/28/2013	4	1.29 × 10^8	Room	0
		10/8/2013	2	1.09 × 10^8	Room	0
		3/20/2014	13	9.75 × 10^8	Room	0
		4/16/2014	3	4.09 × 10^8	Room	0
		5/5/2014	2	1.23 × 10^8	Room	0
TAMU		7/6/2013	2	2.30 × 10^7	Room	0
		8/14/2013	4	7.56 × 10^6	Room	0
		3/10/2014	4	2.49 × 10^8	Room	0
		4/28/2014	11	6.36 × 10^8	100°C	0
Total			48	2.83 × 10^9		0

Table 4: Configuration Single Event Upset Boundary of FIT rates

Environment	Upper Boundary of Configuration SEU FIT Rates
Ground Level (Sea Level, New York City)	Immune
Aviation (40,000 feet, New York City)	Immune
Space (Low Earth Orbit, 800 km circular, 85° inclination)	Immune

V. Data Single Event Upsets

Data single event upset testing was performed at the Los Alamos Neutron Sciences Center (LANSCE) at Los Alamos National Laboratory. Test structures providing maximum visibility of data upsets in flip-flops and memory blocks were used. Flip-flops were tested in nine large shift-registers, each comprising 2000 flip-flops. Sixty-nine LSRAMs and 72 uSRAMs were instantiated. All Core SRAM memory cells were configured as 18 bit words (LSRAM blocks configured as 18x1024 and uSRAM blocks configured as 18x64). The pattern which was written was Data=Addr padded with 0's, in order to help identify address upset. Total bit upsets and word upsets were collected to identify multiple bits upset within a word. Upsets were recorded so that the error rate could be calculated. The results are summarized in Table 5: Data SEU Summary (Single Bit Upsets) on page 5.

It should be noted that data upsets present a much less significant threat to system reliability than the configuration upsets discussed in Section III. Data upsets can be easily mitigated by error correction and detection encoding (EDAC), or by redundancy with parity checking, for example. In many cases upsets of single bits in a data stream are insignificant.

Flip-flop SEUs

Thirty-nine units of M2S050 were exposed to a total fluence of 4.35×10^{11} neutrons/cm^2 at LANSCE. For aviation applications, the error rate is computed at 1.13×10^5 FIT per million flip-flops at 40,000 feet altitude over New York City. For ground level applications, the error rate is computed at 218.3 FIT per million flip-flops at sea level in New York City.

Large SRAM Block SEUs

Thirteen units of M2S050 were exposed to a total fluence of 1.7×10^{11} neutrons/cm^2 at LANSCE. For aviation applications, the error rate is computed at 1.75×10^5 FIT per million bits at 40,000 feet altitude over New York City. For ground level applications, the error rate is computed at 340.6 FIT per million bits at sea level in New York City.

Micro SRAM Block SEUs

Thirteen units of M2S050 were exposed to a total fluence of 1.7×10^{11} neutrons/cm^2 at LANSCE. For aviation applications, the error rate is computed at 9.04×10^4 FIT per million bits at 40,000 feet altitude over New York City. For ground level applications, the error rate is computed at 175.3 FIT per million bits at sea level in New York City.

Multiple Bit Upsets

During testing of flip-flops, LSRAM blocks, and uSRAM blocks, no multiple-bit upsets were detected within any particular word. In part this is due to the physical distance between adjacent bits in the 65nm manufacturing node chosen by Microsemi for SmartFusion2 SoC FPGAs and IGLOO2 FPGAs, and in part it is due to the interleaving of logical bits in the physical implementation of memory blocks in Microsemi FPGAs. Figure 1: on the next page, contains a simplified illustration of this principle. By physically separating logically adjacent memory bits, high energy particles causing upsets in multiple physically adjacent bits cause only single-bit errors to logical words, which are easily corrected with low-overhead error detection and correction codes.

Table 5: Data SEU Summary (Single Bit Upsets)

Feature	Test Fluence (Neutrons/cm^2)	Error Rate Ground Level (Sea Level, NYC, FIT)	Error Rate Aviation (40,000', NYC, FIT)
Flip-flop	4.35 x 10^{11}	218.3 FIT / million flip-flops	1.13 x 10^5 FIT / million flip-flops
LSRAM	1.7 x 10^{11}	340.6 FIT / million bits	1.75 x 10^5 FIT / million bits
uSRAM	1.7 x 10^{11}	175.3 FIT / million bits	9.04 x 10^4 FIT / million bits

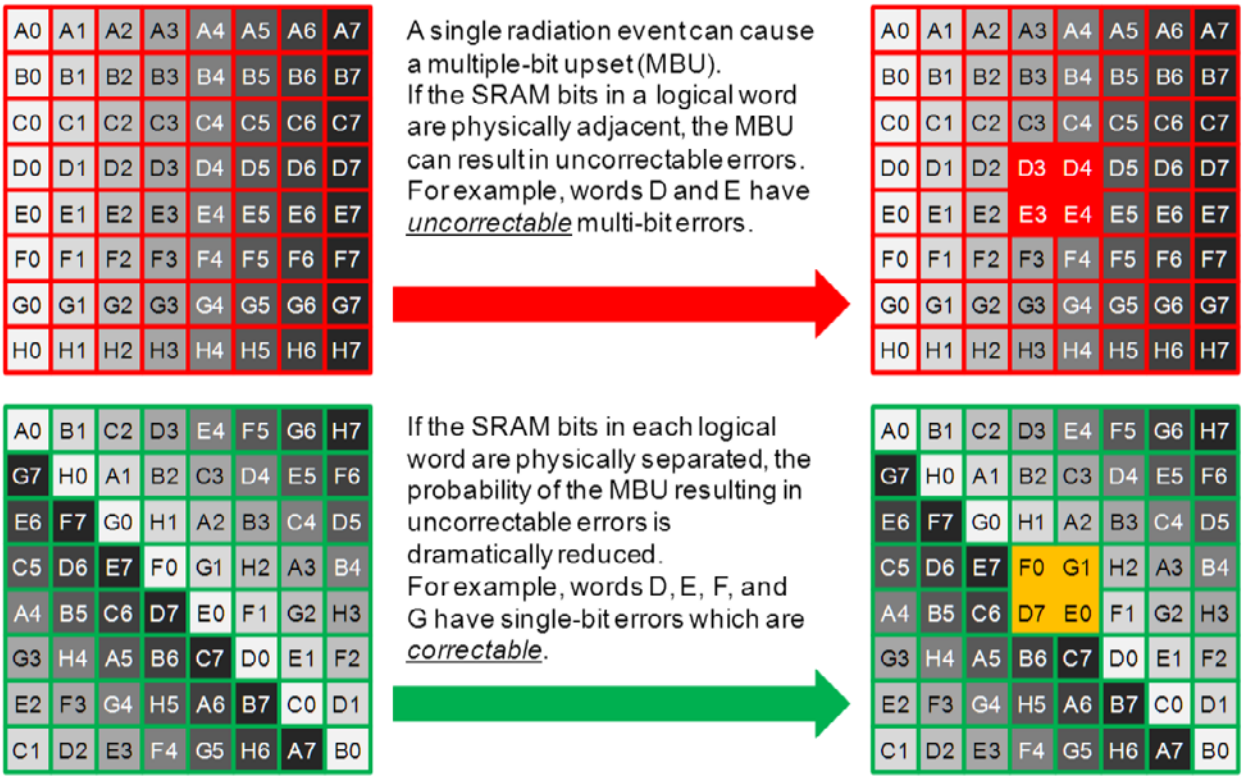

Figure 1: Illustration of Mitigation of Multiple Bit Upsets by Physical Interleaving of Memory Cells

VI. Single Event Functional Interrupts (SEFI)

Functionality of key features was monitored during neutron effects testing, performed at the Los Alamos Neutron Sciences Center (LANSCE) at Los Alamos National Laboratory. The Microprocessor Subsystem (MSS) was monitored for stoppages in functionality by observing the GPIO data. Likewise, the Phased Locked Loop (PLL) was connected to several flip-flop chains to help identify stoppages in the clock. SEFI results are summarized in Table 6: Single Event Functional Interrupt Summary on page 6.

Microprocessor Subsystem (MSS) SEFI

M2S050 FPGAs were exposed to a total neutron fluence of 7.11 x 10^9 n/cm^2 at the LANSCE test facility. As previously stated, functionality of the MSS was monitored by reading and writing a shifted pattern to the GPIO. No functional interrupts of the MSS were detected.

The fluence equates to more than 500 million hours of exposure to atmospheric neutrons at sea level in New York City, or almost one million hours of exposure to atmospheric neutrons at an altitude of 40,000 feet above New York City. The upper boundary of the FIT rate is computed to be 0.2 FIT at sea level and 113 FIT at 40,000 feet above sea level.

Phase Locked Loop (PLL) SEFI

M2S050 FPGAs were exposed to a total neutron fluence of 3.29 x 10^9 n/cm^2 at the LANSCE test facility in three separate test runs, as shown below in Table 6. Functionality of the PLL was monitored by observing for clock stoppage in the FF chain and by monitoring the PLL-lock signal. No functional interrupts of the PLL were detected. The fluence equates to more than 2.3 billion hours of exposure to atmospheric neutrons at sea level in New York City, or more than 4 million hours of exposure to atmospheric neutrons at an altitude of 40,000 feet above New York City. The upper boundary of the FIT rate is computed to be 0.4 FIT at sea level, and 219 FIT at 40,000 feet above sea level.

Table 6: Single Event Functional Interrupt Summary

Feature	Test Fluence (n / cm^2)	Number of SEFI	Equivalent Hours Ground Level (Sea Level, New York City)	Equivalent Hours Aviation (40,000 Feet, New York City)	Upper Bound FIT Rate, Ground Level (Sea Level, New York City)	Upper Bound FIT Rate, Aviation (40,000 Feet, New York City)
MSS	7.11 x 10^9	0	5.08 x 10^8	9.85 x 10^5	0.2	113
PLL	3.29 x 10^{10}	0	2.35 x 10^9	4.57 x 10^6	0.4	219

VII. Conclusion

A series of tests have been performed to evaluate the behavior of IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in heavy ion and neutron radiation environments. Further tests are planned. The tests so far indicate that IGLOO2 FPGAs and SmartFusion2 SoC FPGAs will operate in a satisfactory manner in neutron radiation environments encountered in aviation and ground level applications. For flight-critical applications, mitigation of data upsets in flip-flops and SRAM blocks is advisable. The tests indicate that the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs encounter non-destructive latch-ups in heavy ion radiation testing, at energy levels low enough to cause concern in low earth orbit (LEO) space applications. It should be noted that the SEL onset threshold is in excess of 20 MeV-cm^2/mg, and that single-event latch-ups have not been observed at energy levels relevant for aviation applications.

VIII. List of Changes

Revision	Changes	Page
Revision 2 (October 2014)	Table 5 header was updated.	5
Revision 1 (July 2014)	First Revision	NA

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