Libero IDE v9.2 Release Notes

Thank you for your interest in Microsemi's Libero Integrated Design Environment (IDE) v9.2.

Libero IDE v9.2 includes timing enhancements for RTAX™-S/SL/DSP and Axcelerator FPGA families. This version also updates the routing of long delay lines in RTAX4000S/SL/DSP FPGAs and adds a new design rule check to RTAX-S/SL/DSP pipeline SRAM.

Device Support in Libero IDE

Axcelerator® (including RTAX™-S, RTAX-D),
SX/SX-A (including RTSX/-S/-SU)
ProASIC PLUS (aka APA)
eX
42MX
40MX
ACT1
ACT2/1200XL
ACT3
3200DX
ProASIC (aka 500K)
ProASIC®3 is available for RT prototyping only

Libero SoC supports ProASIC®3, IGLOO®, Fusion, SmartFusion® and SmartFusion2 device families.

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What's New in this Release

New Implementation of Min-Max Timing Analysis for RTAX™-S/SL/DSP and AXFPGAs

Libero IDE v9.2 includes timing enhancements for Hold Check under Worst Case and Setup Check under Best Case timing analysis for

RTAX™-S/SL/DSP and Axcelerator FPGAs. Please read the Application Note AC395 : RTAX-S/SL/DSP Timing Analysis Using Libero IDE v9.2 for details. This document describes a detailed max-min analysis of the external setup and hold time and clock-to-output time for a synchronous design implemented in Microsemi RTAX™-S/SL/DSP FPGAs.

A Customer Notification CN 1410 has been issued.

Routing change for RTAX4000S and RTAX4000D.

Libero IDE 9.2 implements a routing constraint on RTAX4000S and RTAX4000D designs. The router will not create connections using more than four unbuffered long lines. This change to routing behavior is intended to avoid long propagation delays in RTAX4000S and RTAX4000D designs.
For more information, refer to Customer Notification CN 1412.

RTAX-S//SL/DSP and AX pipeline SRAM issue

Libero IDE v9.2 provides a new SRAM design rule check (DRC) put in place for RTAX and AX designs. This check will prevent the usage of a pipeline SRAM configuration which can result in race condition in the SRAM. For more information, refer to Customer Notification CN 1411

Resolved Issues in the v9.2 Release

Refer to your Technical Support Hotline Case Number to determine if it has been fixed in this release. The case number and SAR are listed below.

Table 1 Resolved SARs in Libero IDE v9.2 Release

SAR	Case Number	Product	Summary
25751	1-40412951	Synopsys	Need attribute to control AX DFM* macro inference.
27434	489394-107140793 489394-178835093 493642-30133523 493642-32925603 493642-559503196	VHDL Library	Inconsistent data in the DP RAM when the data is read back out.
28808	489394-198764592	SmartTime	Running datasheet report in SmartTime corrupts timing data in subsequent analysis.
30657	489394-399717782	Misc	RHEL6-Request for newer MOTIF Library Support in Libero Linux.
45569	493642-1063001761	Designer	Creating ANTIFUSESTATS report causes different AFM file.
44005	493642-1196381888	Compile	Libero v9.1 SP5 Designer crashes when an ADB created with libero 9.1.3 is opened.
44457	493642-1215350914	Designer	Designer crash during layout stage.
37665	493642-1028036568	Timing	RTAX-S/SL/DSP External Setup decreased when temperature increased
45502	493642-1215350914	Designer	Excessively long instance names causes crash during layout.
44838	493642-1219970789	Designer	RTSX-SU Prototyping flow for CQ84 is not implemented.
45501	493642-1231776798	Timing	SXA/S Net delay no change between FF to Latch even place a new location
47801	493642-1296864192	Timing	Re-open a saved ADB does not keep the min delay analysis
48809	493642-1355056818	Timing	Tcl command: st_expand_path does not generate complete report in CSV format.
50919	493642-1412481392	Timing	RH1280 design has large delay on bi-di bus.

51128	493642-1458982040	Timing	Best case analysis considers non zero Krad (radiation).
52134	493642-1474493016	CAE	AX Vital lib has wrong if statement.
52150	493642-1494513598	Timing	Timing driven layout crashes in Libero 9.1 SP5.
52296	493642-1495486649	SmartGen	RTAX_COUNTER: Compact counter does not function correctly at 26th bit & onward.
52323	493642-1499505826	Layout	Prototyping file generation is crashing.
53518	493642-1503387344	Timing	RTAX4000D: EMD factors still in default values.
53517	493642-1503387344	Timing	RTAX4000S -1 speed grade factor on nets is not correct.
52388	493642-1503683041	Timing	Max/Min delay constraints enhancement suggest.
53461	493642-1523263801	Timing	SmartTime issue with cross clock domain timing analysis.
53449	493642-1529815451	Timing	Incorrect clock constraint on inter-clcok domain analysis.
53765	493642-1539844086	Timing	Timing difference between SmartTime GUI & timing report.
53961	493642-1552954572	VHDL Library	APA Dyamic PLL simulation model issue.
30870	493642-25401413	Synopsys	Netlist Implementation of 40 MX and 42MX.
36094	493642-553205603	SmartTime	Constraints coverage report fails to recognize constraints.
36750	493642-622346682	SmartTime	Enhance data sheet reporting functionality.
36746	493642-624269471	Synopsys	Using syn_maxfan & syn_noclockbuf but singals are still buffered.
37748	493642-744434833	Compile	Optimized netlist is dropping INV from the original netlist.
53444	493642-752234875, 493642-1510861284	Compile	Port missing after publishing the Designer block.
32724	493642-87097473	SmartTime	Constraint Coverage Report.
40282	93642-945599141	Synplify Pro	Post-synthesis simulation failed with SynplifyPro 2010.09A-1 & speed_grade=STD.

Synopsys and Mentor Graphics Tools

The following versions are included with Libero IDE v9.2. Future releases of Synopsys ME tools will be released stand-alone as they become available.

- Synplify Pro ME G-2012.09A SP4 - This version resolves the problems described in PCN 1209, 1309 & CN 1404
- Identify ME H-2013.03M SP1
- Synphony Model Compiler ME I-2013.09M-1
- ModelSim 10.2c ME

Prerequisite Software: In order to run Synphony Model Compiler ME, you must have MATLAB/Simulink by MathWorks installed with a current license. You cannot run Synphony Model Compiler ME without MATLAB/Simulink.

OEM Release Notes and User Guides

Mentor Graphics ModelSim® ME
Synopsys Synplify Pro ME
Synopsys Identify ME
Synphony Model Compiler ME

Known Limitations, Issues and Workarounds

SynplifyPro will not run in batch mode with a node-locked license

If you want to run Synplify Pro ME in batch mode you need a floating license. Floating licenses for Libero Gold are free. If you are purchasing Libero Platinum, request a floating license product.

Unresponsive Buttons on Linux

Buttons (Close, Browse, OK, Cancel, Next, Back etc.) in the configurators and dialogs may be unresponsive to mouse clicks when the window is first opened.

Workaround*:* Move the entire dialog box slightly. The buttons will then respond.

Also, some of the buttons must be double-clicked (such as Execute Script dialog buttons), which is not typical button behavior.

Drag and drop of Catalog components to SmartDesign Canvas may stop working when using VNC on Linux

Use one of the following workarounds to solve the issue:

- Right-click the selected core in the Catalog and choose **Instantiate in SmartDesign**.
- Exit Libero. Create a new VNC session and log back in to the machine. Start Libero. The drag and drop feature will be enabled.

JTAG Reset Option Description in the Online Help is Incorrect

RTAX-S enables you to program an internal pull-up resistor for the JTAG TRST pin. This option is available in the Programming dialog box. The help topic for this dialog box is INCORRECT. It says:

Use the JTAG reset pull-up resistor - Forces the JTAG circuitry to constantly be in RESET. Microsemi recommends that you use this option.

The correct statement is:

Use the JTAG reset pull-up resistor – Programs the pull-up and forces TRST to HIGH so that it will not reset the Tap controller.

FlashPro Issues Previously Reported in Libero IDE v9.0 SP3 Release Notes

23423 - Error when using Inspect Device if JTAG chain is constructed by performing Auto-Chain Construction.

If the JTAG chain is constructed automatically by selecting Construct Chain Automatically in the **Configuration** Menu, and you click the Inspect Device button, you will see the following error:

Error: Cannot initialize debug engine: Cannot initialize the programmer: No available Actel products found on USB port.

Workaround*:*

Option 1: Construct the device chain by manually specifying the list of devices in the chain using the **Add Actel Device** or **Add non-Actel Device** options, and save the FlashPro project.

Option 2: Manually resolve the device by selecting the Actel device that is in the chain, and save the FlashPro Project.

Option 3: Load the programming file for the devices in the chain, execute read_idcode action in the programming files, and save the FlashPro Project.

6871 - Cannot load the same PDB for multiple devices or copy and paste.

Workaround: Use STAPL files. Generate STAPL files from Libero IDE or FlashPro.

6859 - When using FlashPro programmer with Windows Vista operating system, the Refresh/Rescan may remove the programmer from the programmer list.

Workaround: Restart the FlashPro software. This action will refresh the list of programmers.

System Requirements

Refer to System Requirements on the web for more information regarding operating system support and minimum system requirements.

Libero IDE v9.2 requires runtime components of Microsoft Visual C++ libraries. If a Libero IDE application fails to start, download and install one of the following packages:

- For 32-bit architecture install Microsoft Visual C++ 2008 SP1 Redistributable Package (x86)
- For 64-bit architecture install Microsoft Visual C++ 2008 SP1 Redistributable Package (x64)

Setup Instructions for Red Hat Enterprise Linux OS can be found on the Libero IDE Documents webpage.

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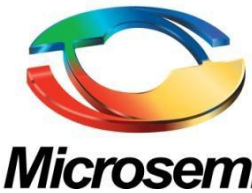
Windows and Linux Version Libero IDE v9.2



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