Libero SoC v11.3 SP1 Release Notes

Libero SoC v11.3 SP1 is an incremental Service Pack that must be installed over Libero SoC v11.3 or 11.3 SPA.

Libero SoC v11.3 is a comprehensive software suite for designing with Microsemi's SmartFusion2 and SmartFusion SoC FPGAs, and IGLOO2, IGLOO, ProASIC3 and Fusion FPGA families.

Visit the Documents tab on your device page at www.microsemi.com to obtain silicon Datasheets, Silicon User's Guides, Tutorials and Application Notes.

Development Kits and Starter Kits are available from the Microsemi website.

Contents

What's New in Libero SoC v11.3 SP1

SERDES support for REFCLK0 and REFCLK1 for Protocol1=EPCS

You can now use separate reference clocks, REFCLK0 and REFCLK1 for EPCS Protocol 0 and 1 respectively. Previous implementations of SERDES did not allow you to use separate reference clocks for the two EPCS protocols.

Hold time violation on Write Assembly Buffer for eNVM Fix

Issue: Standalone eNVM write doesn't work as intended due to a timing issue in the Assembly Buffer. There are no issues when programming a bitstream to both eNVM and FPGA.

Workaround: Change FREQRNG register to decimal 15

There has been a STAPL change that adjusts FREQRNG before eNVM programming and sets it back to user setting afterwards. There will also be an M3 driver change for eNVM (ISP, IAP, Flashloaders) coming in June-July as well as updates to eNVM write Application Note.

Introduced in Libero SoC v11.3

New Device Support

IGLOO2

Die	Package	Speed Grade	Temp Ranges	Free Libero Gold
M2GL005	144 VQ	STD, -1	COM, IND, Custom	Yes
M2GL005S	144 VQ	-1	IND, Custom	No
M2GL090	325 FCSBGA	STD, -1	COM, IND, Custom	No
M2GL090S	325 FCSBGA	-1	IND, Custom	No
M2GL090T	325 FCSBGA	STD, -1	COM, IND, Custom	No
M2GL090TS	325 FCSBGA	-1	IND, Custom	No

SmartFusion2

Die	Package	Speed Grade	Temp Ranges	Free Libero Gold
M2S005	144 VQ	STD, -1	COM, IND, Custom	Yes
M2S005S	144 VQ	-1	IND, Custom	No
M2S090	325 FCSBGA	STD, -1	COM, IND, Custom	No
M2S090S	325 FCSBGA	-1	IND, Custom	No
M2S090T	325 FCSBGA	STD, -1	COM, IND, Custom	No
M2S090TS	325 FCSBGA	-1	IND, Custom	No

Updating Your Design to Libero SoC v11.3

Pre-Libero SoC v11.3 designs may incorporate I/O standards that are no longer supported and/or out-of-date SERDES blocks.

Unsupported I/O Standards

The following I/O standards are not supported on the MSIO or MSIOD banks:

- SSTL18I
- SSTL18II
- HSTLI
- HSTLII

If your pre-v11.3 design contains I/O standards on unsupported banks or out-of-date SERDES blocks then the software automatically invalidates your Compile state.

If your design is affected then when you open your project you will see the following message:

Warning: Your design has been invalidated to a pre-Compile state because of unsupported I/O standards. Your design has been invalidated because it contains out-of-date SERDES blocks.

Designs Containing SERDES Blocks

Action required:

If your design contains out-of-date SERDES blocks you must replace the SERDES cores with the latest version available from the repository and regenerate the design. Re-run Compile. If your design does not compile because the I/O's are still on unsupported banks you must do one of the following:

- Unplace the I/O's.
- Move them to a DDRIO bank.
- Change the standard for the I/O's on the unsupported banks.

Software Enhancements

Libero SoC Secure IP Flow

Microsemi adopted IEEE P1735 and supports an encrypted IP design flow for the SmartFusion2 and IGLOO2 silicon families. See "Libero SoC Secure IP Flow User Guide" on the Microsemi web site for details.

Together with Synplify Pro ME from Synopsys and ModelSim ME from Mentor Graphics, Libero SoC enables a seamless design flow for designers targeting SmartFusion2 and IGLOO2 when they use IP cores in their design.

Use of IP cores not only shortens the design cycle time but also provides proven and reliable design components for re-use in multiple applications.

Please review the known limitations below.

To use the Secure IP flow email Microsemi SoC Marketing at soc_marketing@microsemi.com and request the public key.

Project Manager

Synplify Pro output in Verilog. EDIF is still the default.

Improved modular design methodology.

Use Verilog to avoid the EDIF limitations (single EDIF, no merging).

New BFM Checker Tool

Available when editing a BFM file in a Libero Text Editor.

SmartDesign

Canvas enhancements improve display, resizing, scrolling and notes.

Option to show Canvas grid.

Option to show net names on the routed lines.

System Builder

IGLOO2 & SmartFusion2 Enhancements

Integration of CoreAHBLite with up to 4 fabric masters.

Access to internally used resources such as CCC and oscillators.

SmartFusion2 MSS GPIO

IOMUX design rule checks

eNVM Configurator Integration

High Speed Serial Interface (SERDES) Configurator Updates

The High Speed Serial Interface Configurator GUI has been updated. Updates include:

- Support for the M2S090T(S) and M2GL090T(S) device with two PCIe controllers in the same SERDESIF block.

- GUI support for PCIe Master and Slave address windows
- Full data rate range support for the EPCS mode
- Single-Ended reference clock option

DDR Verification IP

Supports DDR3, DDR2, LPDDR

- Delivered as a Simulation Core available from the Catalog. It is a generic DDR memory simulation model that emulates DDR/DDR2/LPDDR DRAM non-timing functionality.

eNVM

Configurator

New Data Storage Content Type (Place Holder)

Simulation support for Data Storage Client

eNVM Content Update Tool

Users can fill in the Place Holder with actual data and decide when to program that client.

Timing Constraints

TDPR Scenarios for Timing Closure

If you have followed the usual procedures for timing closure and continue to see specific paths which are far from being satisfied, you can create a TDPR timing scenario.

1. Open the Timing Constraints Editor.
2. Click "View", "Scenarios".
3. Right-click to create a clone of your "Primary" scenario.
4. Mark the clone as being used for TDPR. This will automatically set the original Primary scenario as the default "Analysis" scenario.

In the TDPR scenario, you may specify a more aggressive timing constraint for a clock domain or add Max Delay constraints between logic sources and sinks which you wish to optimize. These constraints will be detected by the Layout tools and the timing for these paths should improve when you re-run Layout. In general, you should use the *real* requirements for constraining the design. This gives the Layout tools the most amount of flexibility to achieve timing closure.

CCC External Feedback Loop

New SDC constraint to compute external feedback.

Improved Handling of Constraints to I/Os and ASIC Blocks (MSS/DDR/SERDES) in TDPR

SmartTime

Two new extended SDC commands for specifying I/O constraints

- set_external_check
- set_clock_to_output

Options are now available to specify the feedback output and feedback input pins for PLLs with external feedback.

These options must be used with the create_generated_clock command. They are mandatory for PLLs using the external feedback option.

- -pll_output
- -pll_feedback

New SDC constraint to support calculation of CCC external feedback loop

Improved I/O Bank Assigner

Routing Improvements for Complex Designs

Multi-pass Layout script for SmartFusion2 and IGLOO2 designs

A new Tcl script is available for running multiple iterations of Place and Route to identify the seed that produces optimal performance for your design. Instructions for using this script are found in Libero SoC v11.3 Help and User Guide.

Programming

2 STEP IAP support for M2S/M2GL090

Programming Features and Configure Export Programming File Performance speedup

Enable Debug Policy within SPM

Resolved Issues

Issues Fixed in v11.3

SAR	Summary
42808	Fixed Warning: Unrecognized option ignored: "-_include"
51780	Attribute set on SYSRST macro is now propagated when Compile Point is set
51782	Synplify Pro handles when Compile Point is set to "soft" for a design using MSS.
52006	Able to generate the STAPL file with eNVM client of size 3 bytes or less
52013	EDIF netlist is now correct for designs using TRIBUF, BIBUF & -disable_io_insertion
52264	Error checking added for hex values to ensure min is less than max
52503	Instrumented design passes in synthesis when new implementation option is used
52718	VHDL generated for core has been fixed, eliminating synthesis error
53356	Live and Active probe are fixed for M2S150 and M2GL150

Customer Reported SARs fixed in v11.3 SPA

SAR	CASE	Product	Summary
56011	493642-1602905462	Layout	Layout fails during placement due to defect in the self-timed clock conversion.
53935	493642-1578052041	SERDES	Added support for 2 REFCLK sources for EPCS protocol

Customer Reported SARs fixed in v11.3

Refer to your Technical Support Hotline Case Number to determine if it has been fixed in this release. The case number and SAR are listed below.

SAR	CASE	Product	Summary
29652	489394-198764592	Verilog Lib	Update Timing resolution in Verilog simulation libraries.
37918	493642-752234875	Designer	Port missing after publishing the Designer block.
40268	493642-757597223	Project_Manager	Allow Simulator Profile to be created for Active-HDL.

43942	493642-1193065892	Project Manager	Libero should display the last report opened before the project was saved/closed.
44308	493642-1207163697	SmartDesign	Text box cannot be updated.
47387	493642-1313737649	Smartgen	Modifications done using "Add Note" feature is not getting saved.
47643	493642-1325709323	Project Manager	Tcl - generate_hdl_netlist is not supported run_tool fails for SmartFusion2.
48700	493642-1365137500	Project Manager	No SpaceKey Recognition in Libero 11.0.
49963	493642-1414829488	SmartDesign	SmartDesign generated VHD file incorrectly.
51456	493642-1472314192	SmartDesign	Display NET name in SmartDesign canvas.
52718	493642-1563679450	HDL	Syntax error in generated VHDL for Core.
52850	493642-1497780949	ModelSim	Edit ModelSim PLL warning message.
52984	493642-1523292958	FlashPro	Error when exporting chain STAPL for APA device
53315	493642-1525833322	SmartDebug	Add disable-M3 & live-probing interfaces.
53635	493642-1532166587	SmartGen	Division by zero in PLL simulation model causes ModelSim error: Iteration limit reached...
53715	493642-1534164169	FlashPro	Chain programming fails with PA3 devices.
54047	493642-1523263801	SmartTime	Issue with cross clock domain timing analysis.
54048	493642-1529815451	SmartTime	Incorrect clock constraint on Inter-clock domain analysis.

Known Limitations, Issues and Workarounds

Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines the InstallShield Wizard displays a message stating:

The installation of Microsoft Visual C++ 2005 SP1 Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Select **Yes** and the installation will complete successfully.

SmartFusion2 and IGLOO2

PCI Express Advanced Feature Limitations

SAR 53628 - PCIe registers are not initialized properly in all cases.

In Libero SoC v11.3 the PCIe SERDESIF does not support using a few of the advanced features. This is due to a problem in the peripheral initialization routine of the PCIe bridge registers. The limitations are as follows:

- ECRC Enable/Disable is not available.
- Power Management Capability Structure cannot be modified from default values.
- Completion Timeout cannot be modified from default value.
- AXI/AHB Master/Slave Windows
    - Only a single master or slave window can be assigned.

If any of these limitations are required for your design please contact Microsemi Technical Support at soc_tech@microsemi.com. Design-specific implementations may be available that will allow you to work-around the limitation. All of the above limitations will be removed in a future release.

SAR 55154 - PCIe SERDESIF reverse x1 mode not linking up

PCIe protocol does not linkup in a PCIe slot when configured in PCIe reverse mode as a x1. There is currently no workaround. This will be fixed in a future release.

SAR 55035 - PCIe SERDESIF configuration is lost when changing lane width

In the SERDES GUI Configurator when switching the link width, PCIe related settings are lost and go back to the GUI default values.

Workaround: Reopen “Config PCIe” to retain the PCIe settings after changing number of lanes.

SAR 52554 – 325 FCSBGA Package and SERDES lane limitations

In Libero SoC v11.2 SP1 the following protocols are supported:

- PCIe x1
- EPCS x1 and x2 (x2 is a special case where you MUST use the x4 mode to get to lane 0 and 2)

Only lanes 0 and 2 are bonded in this package. See the datasheet for a detailed package description.

There are no restrictions in the configurator today. There are no design rules in Compile to prevent unsupported configurations from passing.

SAR 51770 – MSS/HPMS VHDL Post-synthesis/Post-layout Simulation fails for projects created with Libero SoC v11.1 SP3 and earlier

In SmartFusion2/IGLOO2 VHDL designs that were created with Libero SoC v11.1 SP3 and earlier, post-synthesis and post-layout simulations that use the MSS or HPMS will fail in Libero 11.2 and later releases. Re-synthesize your design to work around this issue. This issue does NOT affect Verilog designs, nor does it affect new designs created using Libero SoC v11.2 or later releases.

SAR 48448 - Zeroization will be available in a future release.

SAR 46571 - M2S050 has only one Oscillator

When you instantiate the Oscillator in your design and also use MSS RTC, the Clock Source of the RTC must match the clock source used in the Oscillator. For example, configuring the RTC with Clock Source set to 32 KHz RTC Crystal Oscillator while the Oscillator block is configured with the External Main Crystal Oscillator set to 5 MHz is invalid. The frequencies must match.

MIL Temp Removed from 400 VF, 676 FBGA & 896 FBGA packages

Military Temperature for all SmartFusion2 and IGLOO2 packages was introduced in V11.2. Subsequently, we decided to offer MIL Temp only for 484 FBGA and 1152 FC packages.

If you started a design using Libero SoC v11.2 and selected MIL Temp for any 400 VF, 676 FBGA or 896 FBGA package, when you open the project in Libero SoC v11.3 the software will crash. Please contact soc_tech@microsemi.com for instructions on how to modify your project so that it can be opened in the current release.

For IGLOO2 projects use System Builder for the following cores; do not use these cores from the Catalog directly.

- DDR Memory Controller
- CoreConfigP
- CoreResetP
- CoreConfigMaster

Secure IP Flow

SAR 54743 - Synplify Pro errors out when unencrypted module has pragma definitions for the encryption envelope.

This issue is seen when you attempt to run synthesis with the unencrypted RTL that includes the pragma encryption envelopes.

Workaround: Use either "pragma translate_off, translate_on" or "synthesis translate_off, translate_on" around the pragma definitions.

SAR 54660 - Check HDL errors out for encrypted HDL

Encrypted modules will trigger false errors when 'Check HDL' feature is run. These errors can be ignored.

SAR 54310 - Importing RTL or netlist with fully encrypted top level is not supported

Libero SoC supports 'Secure IP Flow' with the expectation that the top level module of the design is unencrypted. The requirement is that the port interface and module definition for the top level are unencrypted. The remaining contents of the top level module can be encrypted.

SAR 54309 - Selecting "Edif netlist" option under "Project Settings" is not supported with Secure IP Flow and may produce confusing error messages during Compile

If your design includes secure IP blocks, you must select the "Verilog netlist" option under "Project Settings".

If the default "Edif netlist" option is selected, the compile step will issue error messages. The error messages will vary based on your design and the cause is not intuitively clear.

For example, one possible error message is: ERROR: CMP002: Net: _name_of_net_ is not driven

SAR 54271 - Hierarchy of design not preserved in ChipPlanner for a partially encrypted design

SAR 54122 - Libero fails to resolve design hierarchy when encrypted IP modules are defined in multiple files

Libero does not support design hierarchy resolution if the encrypted IP block is defined in multiple files.

When working with an encrypted IP block defined in multiple files, you must manually pass all the required files for the following steps:

- Synthesis
- Pre-synthesis simulation

To pass the required files, right click on the flow step in Libero --> Organize Input Files --> Organize Source Files. Select the 'User' radio button and add the missing files to the list.

SAR 54054 - Secure IP Flow: VHDL compiler directive ‘protect’ treated as illegal syntax

Check HDL will show false errors for Encrypted VHDL modules. This error prevents you from instantiating Encrypted VHDL modules in SmartDesign.

Libero

When a Pre-Libero SoC v11.3 project using EDIF netlist flow is changed to Verilog netlist flow, the project will be invalidated post-synthesis.

SAR 54877 – Block design cannot be used with Verilog flow.

Every block component has a black_box attribute in the _syn.v file. Synplify Pro will not write the definition in the .vm file for a module that has a black box attribute on it. You have to provide details for this black box if you run compile.

SAR 51880 – Project Archiving tool states are not retained when a Libero Project is uploaded on SVN

Workaround: Zip the project and upload to SVN in order to retain the tool states.

SAR 50267 – Selecting SMEV RAM available in Fusion's Advanced Analog System Options dialog degrades the Resolution performance

In the datasheet we state a resolution of 1/0.25 Deg while using ADC in 10/12 bit mode. When using SMEV RAM we have observed a resolution of 3-4 Deg. in some cases.

SAR 49569 – Libero does not support importing aFDC file. To add constraints for Compile Point, you must open Synplify Pro to add them.

SAR 48929 - SmartDesign shows incorrect Memory Map for SmartFusion2 FIC_1

In designs with the default FIC Regions configuration for SmartFusion2, FIC_1 has the following Fabric Slave regions: 0x80000000-0x8fffffff, 0x90000000-0x9fffffff, 0xf0000000-0xffffffff. However, SmartDesign incorrectly shows FIC_1 slaves in the 0x70000000-0x7fffffff region. This is a display issue, and the generated netlist is correct.

SAR 47957 - SmartFusion2/IGLOO2 RAM Initialization Configurator – Importing Simple-Hex and Motorola-Hex files is not working

When you try to import Simple-Hex or Motorola-Hex files for initialization for simulation, Libero may crash or the import may fail (content initialized to all zeroes).

Workaround: There is a workaround available that utilizes a *.shx file generated for Fusion. Contact Microsemi Technical Support at soc_tech@microsemi.com for details. Ask for the workaround for SAR 47957.

SAR 46161 - The post-synthesis EDN file will not appear in the design hierarchy until the project is closed and reopened.

SAR 43772 - Linux: The SmartFusion2 configurators for DDR and FICs are missing the diagram describing the details of the block

This issue will be fixed in a future release.

SAR 42170 - MVN Cross probing is not supported for Path List and Expanded Path View of the Min and Max Analysis windows

This issue will be fixed in a future release.

SAR 41619 - IGLOO+ hot-swappable option is not displayed correctly in the GUI

Hot-swappable is always ON for IGLOO+ and cannot be changed. The GUI allows you to check/uncheck this feature, but it is ignored by the tools. These I/Os are always hot swappable.

SAR 40881 – When selecting the 2 AHB mode in the FDDR configurator, you must manually edit the register DDR_FIC_NUM_AHB_MASTERS_CR.

Workaround: Manually edit the register value. The configurator is not setting the correct value for the register DDR_FIC_NUM_AHB_MASTERS_CR.CFG_NUM_AHB_MASTERS.

System Builder

When the eNVM mem file is updated using the option "Update eNVM Memory Content" the update is not get reflected into the memory file that is used for simulation.

Workaround: SmartDesign top level needs to be regenerated for the new mem file data to be updated into the mem file (ENVM_init.mem) used for simulation.

SAR 55154 - PCIe SERDESIF reverse x1 mode not linking up

PCIe protocol does not linkup when configured in PCIe reverse mode with one lane. There is currently no workaround. This will be fixed in a future release.

SAR 55035 - PCIe SERDESIF configuration is lost when changing lane width

PCIe related settings are lost when the number of lanes are changed in the SERDES configurator.

Workaround: Reopen “Config PCIe” to retain the PCIe settings after changing number of lanes.

SAR 53628 - SmartFusion2 and IGLOO2 PCI Express Advanced Feature Limitations

In Libero SoC v11.3 the PCIe SERDESIF does not support using a few of the advanced features. This is due to a problem in the peripheral initialization routine of the PCIe bridge registers. The limitations are as follows:

- ECRC Enable/Disable is not available.
- Power Management Capability Structure cannot be modified from default values.
- Completion Timeout cannot be modified from default value.
- AXI/AHB Master/Slave Windows
    - Only a single master or slave window can be assigned.

If any of these limitations are required for your design please contact Microsemi Technical Support at soc_tech@microsemi.com. Design-specific implementations may be available that will allow you to work-around the limitation. All of the above limitations will be removed in a future release.

SAR 49025 – System Builder shows incorrect Memory Map for IGLOO2

In the Memory Map page, the addresses for the HPMS FIC_0/1 slaves are shown as 0x80000000. It should read as (0x00000000-0x0fffffff + 0x20000000-0x2fffffff + 0x400000000-0x4fffffff + 0x60000000-0x6fffffff).

System Services simulation is planned for a future release.

You must configure PDMA dynamically.

SmartTime

SAR 34365 - Asynchronous Register paths are not displayed in Timing Analysis view

This issue will be fixed in a future release.

SAR 43767 – Maximize Window button is missing from the title bar for Constraints Editor, Max Analysis and Min Analysis

Workaround: Double-click the title bar to maximize the window.

SAR 43726 - The exported Tcl file does not include commands to organize SDC files.

Workaround: Requires editing the exported TCL file carefully. This issue will be fixed in a future release.

SmartPower

SAR 49868 – The Power Report is generated only for the first run when using the Multi-pass Layout option.

This will be fixed in a future release.

Synopsys Synplify Pro

SAR 55543 - The *.so has *.edf option for synthesis_1/2 implementation through Libero

You can create synthesis_<1/2> implementation by invoking Synplify Pro interactively through Libero. Run synthesis and Libero gets updated accordingly. However, after creating the synthesis_<1/2> implementation if you go back to Libero and change to any different die and run synthesis for

synthesis_<1/2> implementation, the synthesis_<1/2> implementation will not be updated correctly. Libero will report the following error:

Unable to find the file 'P:\Test_edif_multiple\synthesis\synthesis_1\dotp_accsub_unsign_asrstn_en.edf', cannot add it to Libero project.

Error: Synthesis failed.

Workaround: After changing to a different die in Libero, invoke Synplify Pro interactively and copy the synthesis implementation to a new name, run synthesis for this new implementation and Libero will be updated correctly.

SAR 54584 - Generic of std_logic in VHDL RTL reports error in Compile for VM flow

When the generic is defined as STD_LOGIC and the value is assigned in ‘ ‘ in RTL, the .vm netlist generated will error in Compile. The reason is Synplify Pro considers ‘ ‘ also as part of value and then tried to escape it using ‘\’while writing it in the vm netlist.

Work-around: Use std_logic_vector(0 downto 0) instead of std_logic in RTL.

SAR 46982 - Synplify Pro treats the PLL as a black box

SDC constraints applied to the PLL input do not propagate forward. To actively constrain it; you must constrain both the input and the output of the PLL using the create_clock and create_generated_clock constraints. More information can be found in KI70291.

SAR 46983 - False Path, Multicycle Path and Max delay constraints are not propagated to the SDC file used by Synplify Pro

For more information about constraints consult Chapter 4, Specifying Constraints, in the Synplify Pro User Guide.

Synplify Pro Warning: Unrecognized technology/part/package in Synplify Pro

When executing synthesis using the Libero integrated flow a warning appears if the silicon family, die or package is not present in Synplify Pro. In most cases the design will automatically be mapped to an existing device and continue. If no mapping exists the flow will halt.

Missing Die

```
Unrecognized part [die] specified for device [silicon_family] in
[design_name]:synthesis
```

Design will be mapped to a pre-programmed default and synthesis will proceed.

Missing Package

```
Unrecognized package [package_name] specified for part [die] in
[design_name]:synthesis
```

Design will be mapped to a pre-programmed default and synthesis will proceed.

Missing Silicon Family

```
Warning: Unrecognized technology: [silicon_family]
Unrecognized technology: [silicon_family] in [design_name]:synthesis
```

Synplify Pro halts.

Synopsys Identify ME

SAR 55517 - Stand-alone Identify Instrumentor error

Users will see the following error if any Synplify Pro-Identify instrumented project is opened in stand-alone Identify Instrumentor.

ERROR: Cannot load 'synthesis_1' instrumentation: couldn't execute "T:\ Synopsys\ synplify_I201309MSP1\bin\synplify.exe": no such file or directory

Workaround: Use Synplify Pro to invoke Identify Instrumentor and it will automatically open the relevant project.

Programming

SVF for SmartFusion2 and IGLOO2 will be available in a future release.

SAR 55421 - "Device I/O states During Programming" Option crashing on Linux

Segmentation fault error occurs for a SmartFusion2 or IGLOO2 project, when you select Edit Design Hardware Configuration -> Device I/O states During Programming -> Configure Options, then Edit I/O State and close GUI.

SAR 51767 - Error: The command 'load_programming_data' failed.

During programming file generation if the serialization content files cannot be found, then you will see the following error : "Error: The command 'load_programming_data' failed."

Workaround: Open **Update eNVM Memory Content** and specify a valid path for each serialization content file.

SAR 45867 - STAPL player for SmartFusion2 or IGLOO2 will be available in a future release.

SAR 41069 - Add PDB loading from DDF for Libero environment

You may get an exit 6 idcode failure when chain programming within Libero using a PDB file.

Workaround: Use a STAPL file or use the standalone FlashPro tool for chain programming

SAR 47452 - FlashPro verify and erase errors are reported as programming failures.

If you run programming ACTION VERIFY/ERASE and there is a failure, then the error code will indicate it is a programming failure even though you were running action VERIFY/ERASE.

SmartDebug

SAR 54004 - Search in Debug FPGA GUI does not support wild card. This will be supported in a future release.

SAR 55368 - eNVM cannot be accessed from SmartDebug when UPK1 is used to lock eNVM update protection.

SmartFusion2 devices will read invalid memory content if the MSS is held in the reset state or M3 is executing invalid microcode programmed into the Flash Memory.

Workaround: Program a valid design. Confirm that the MSS is not in the reset state.

SmartDebug SERDES will not work for M2S050PP and ES parts.

SmartDebug Tcl commands in the Libero flow will be supported in a future release.

System Requirements

Refer to System Requirements on the web for more information regarding operating systems support and minimum system requirements. 64-bit OS is required for designing SmartFusion2 and IGLOO2 devices.

Setup Instructions for Linux OS can be found on the Libero SoC Documents webpage.

Synopsys and Mentor Graphics Tools

These tools are included with the Libero SoC v11.3 installation.

Synplify Pro ME 2013.09M SP1 Release Notes

ModelSim ME 10.2c

Identify ME 2013.09M SP1 Release Notes (Windows only)

Synphony Model Compiler 2013.09M-1 Release Notes

Prerequisite Software: In order to run Synphony Model Compiler ME, you must have MATLAB/Simulink by MathWorks installed with a current license. You cannot run Synphony Model Compiler ME without MATLAB/Simulink.

Download Libero SoC v11.3 SP1

Installation requires Admin privileges

- Download Libero SoC v11.3 SP1 for Windows
- Download Libero SoC v11.3 SP1 for Linux

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