SmartFusion2 SoC and IGLOO2 FPGA Characterization Report for SGMII/1000BASE-X

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I. Introduction

A. Overview of SmartFusion2 SoC and IGLOO2 FPGAs

The Microsemi SmartFusion2® SoC and IGLOO®2 FPGA device family provides compliant Serial Gigabit Media Independent Interfaces (SGMII) for use as a connection bus for the Ethernet MACs and PHYs defined by Cisco Systems. The standard applies to Gigabit Ethernet and 1000BASE-X standards which all use similar electrical domains and are clock tolerance compliant with Ethernet specification.

SGMII replaces the wide parallel media interface connections with a low pin count, four-pair, differential SERDES connection. The legacy GMII interface defined in the IEEE 802.3 specification is strictly for gigabit rate operation. However, the Cisco SGMII specification defines a method for operating 10 Mbps, 100 Mbps and 1000 Mbps over the same interface.

The number of SERDESIF modules on the IGLOO2 and SmartFusion2 SoC FPGA depends on the device size. The smaller devices support a single SERDESIF with four SGMII/1000BASE-X interfaces. The larger devices support up to four SERDESIF modules for a total of 16 SGMII/1000BASE-X interfaces. More information on the SmartFusion2 SoC and IGLOO2 FPGA device family can be found on the SmartFusion2 SoC and IGLOO2 FPGA Product Page at *www.microsemi.com*.

B. Scope of this Report

Complete testing and validation of specifications required by SGMII/Gb Ethernet/1000BASE-X standards were conducted on the SmartFusion2 SoC and IGLOO2 FPGA device. This report provides the user community a summary of testing completed to demonstrate compliance to the standard, as defined by the IEEE 802.3 1 Gigabit Ethernet Task Force. The testing analyzed voltage, temperature, and process variations for electrical validation. This report serves as a reference to specific testing used to provide high confidence that the devices will perform as expected in SGMII/1000BASE-X specific systems.

References:

- SGMII- Serial-GMII Specification- Cisco Systems Revision 1.8, April 2005
- GIGABIT ETHERNET- PMD Sublayer, Type 1000Base-X, Sections 38 and 39 of IEEE Standard 802.3, 2000 Edition

II. Electrical Compliance Testing

Table 1: SGMII/1000BASE-X Transmit Test Specifications

Parameter	Min	Max	Units
AC Specifications			
Cycle to Cycle Clock Jitter		100	pS p-p
Imperfect Duty Cycle		30	pS p-p
Data Dependent Jitter		70	pS p-p
Skew		100	Ps p-p
Total Jitter		< 550	mUI
DC Specifications			
Output Voltage High		1525	mV
Output Voltage Low	875		mV
Output Differential Voltage	150	400	mV
Output Offset Voltage	1075	1325	mV
Output Impedance(differential)	40	140	ohms

III. Microsemi Test Boards

Testing is performed on the Microsemi Signal Integrity Board (SI),that is equipped with a test socket and provides connections to vary power supply conditions. To ensure the integrity of the characterization measurements, special attention is given to the signal integrity of the high-speed serial channels. Detailed analysis ensures the board performs as designed. The transmitter (Tx) and receiver (Rx) signal paths for each SERDES are carefully routed to high-bandwidth SMP connectors to ensure good signal integrity and performance. The PCB channel is measured and de-embedded when performing tests.

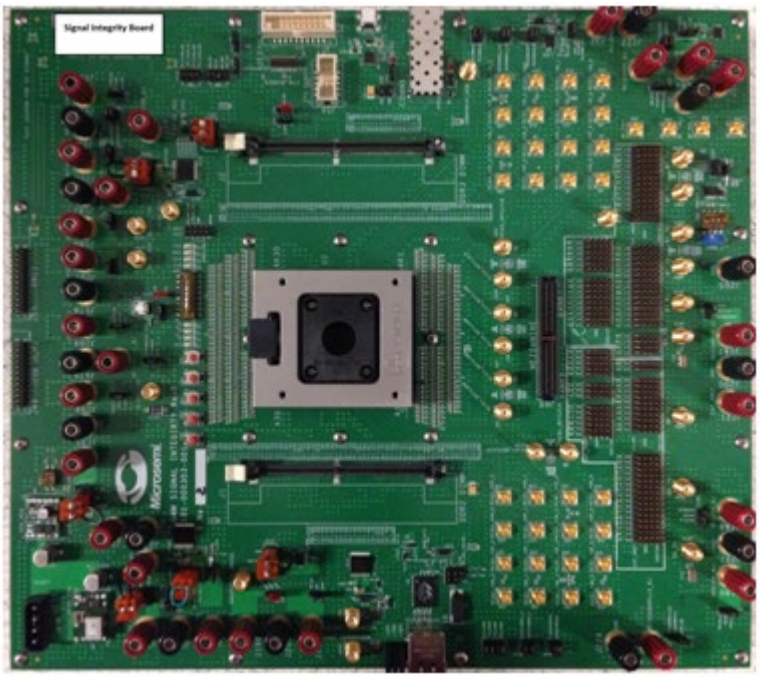

Figure 1: SmartFusion2 SoC and IGLOO2 FPGA Signal Integrity Board

IV Device Testing Samples

Testing was conducted on a sample of devices representing process variations across silicon fabrication. These devices were separated from a larger group of devices representing the worse-case corners to report the results. The results are correlated as presented in the data as worst-case.

V Electrical Device Testing

Bench test equipment was used for both of the Rx jitter and the Tx jitter and amplitude measurements.

A. Electrical Testing Equipment/Software

- Agilent DSA91204A 12 GHz Oscilloscope
  - EZJIT Plus, Jitter Analysis Software
  - Serial Data Analysis Software
- Two Stanford Research Systems 2.05 GHz Clock Generators Model CG635
- Agilent N6701A Power Supply Mainframe
  - Four individually controlled P/S Modules

- Agilent E3648A Dual Output Power Supply
  - Silicon Thermal, Temperature Control Unit
  - Silicon Thermal Cooler CH400
  - Silicon Thermal Linear Power Supply PS190-L
  - Silicon Thermal Controller LB190-L
  - Thermal Head Adapter
- Quantity: two SMA (m)-to-SMP cables to mate with DUT (~ 1-3 ft long)
- Quantity: two SMA (f) adapters for Scope
- Quantity: two Mini – Circuits SMA Bias Tees ZFBT- 4R2G
- Agilent E5071A 20GHz ENA (for impedance measurements)
- E-Cal Module for ENA
- Microsemi Engineering, Signal Integrity Board

B. Electrical Testing Environment

Device electrical testing was conducted by the Microsemi factory using variations on power supply voltages and temperatures. Minimum voltage (Vmin) and maximum voltage (Vmax) were varied by +/-5% of the typical voltage (Vtyp) supply for the supplies related to the SERDES PMA blocks of the device. The devices were also tested at the industrial temperature limits (-40C to +125C).

Table 2: Temperature Specifications

Specifcation	Temperature Range
Military Temperatures	-55^0C to 125^0C
Industrial Temperatures	-40^0C to 100^0C
Commercial temperatures	0^0C to 85^0C

C. Testing Conditions

Table 3: Power Supply and Temperature Test Conditions

Voltage and Temperature Matrix						
Voltage Dependencies	**1.2 V VDD range**					
xDDR_PLL_VDDA	3.15 V	3.3 V	3.45 V	3.15 V	3.3 V	3.45 V
CCC_xyz_PLL_VDDA	2.375 V	2.5 V	2.625 V	3.15 V	3.3 V	3.45 V
SERDES_x_PLL_VDDA	2.375 V	2.5 V	2.625 V	3.15 V	3.3 V	3.45 V
SERDES_x_L[0:3]VDDAPLL	2.375 V	2.5 V	2.625 V	2.375 V	2.5 V	2.625 V
SERDES_x_L[0:3]VDDAIO	1.14 V	1.2 V	1.26 V	1.14 V	1.2 V	1.26 V
SERDES_x_VDD	1.14 V	1.2 V	1.26 V	1.14 V	1.2 V	1.26 V
VDD (Core Supply)	1.14 V	1.2 V	1.26 V	1.14 V	1.2 V	1.26 V
Temperatures	-55C	-55C	-55C	-55C	-55C	-55C
	-40C	-40C	-40C	-40C	-40C	-40C
	0C	0C	0C	0C	0C	0C

Voltage and Temperature Matrix						
Voltage Dependencies	**1.2 V VDD range**					
	25C	25C	25C	25C	25C	25C
	85C	85C	85C	85C	85C	85C
	100C	100C	100C	100C	100C	100C
	125C	125C	125C	125C	125C	125C

VI Transmitter Test Results Summary

Table 4: SGMII/1000BASE-X Transmit Test Results

Defined Test	SmartFusion2/IGLOO2 Devices				
	Parameter	**Spec**	**Worst Case Test Results**	**Unit**	**Pass/ Fail**
Transmitter Testing					
VOCM, DC-DC Offset	Max	1075<=Value<=1325	1130	mV	Pass
VOCM, AC – Common Mode Noise	Min	Value <= 25mV	2	mV	Pass
VODpp – Peak to Peak			636	mV	
VOD – Differential Swing	Max	150mV<=Value<=400mV	318	mV	Pass
TR – Rise Time	Max	100ps<=Value<=200ps	189	pS	Pass
TF– Fall Time	Max	100ps<=Value<=200ps	199	pS	Pass
TJ – Total Jitter(TX)	Max	Value <= 192ps(0.24UI)	71	pS	Pass
DJ– Deterministic Jitter	Max	Value <= 80ps	37	pS	Pass

A. SGMII/1000BASE-X Transmitter Tests

SGMII/1000BASE-X Transmitter Test Setup

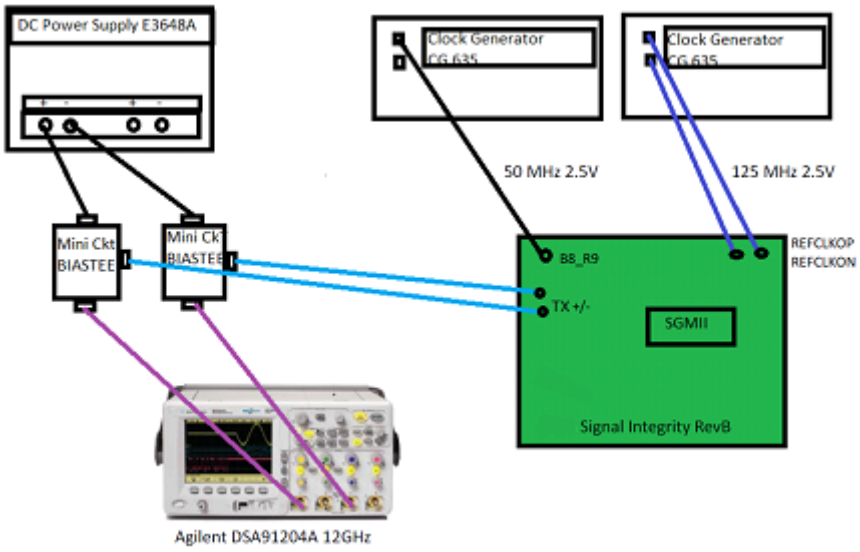

Figure 2: Transmitter Test Setup

The signals were tested differentially on a powered device with an inactive transmitter.

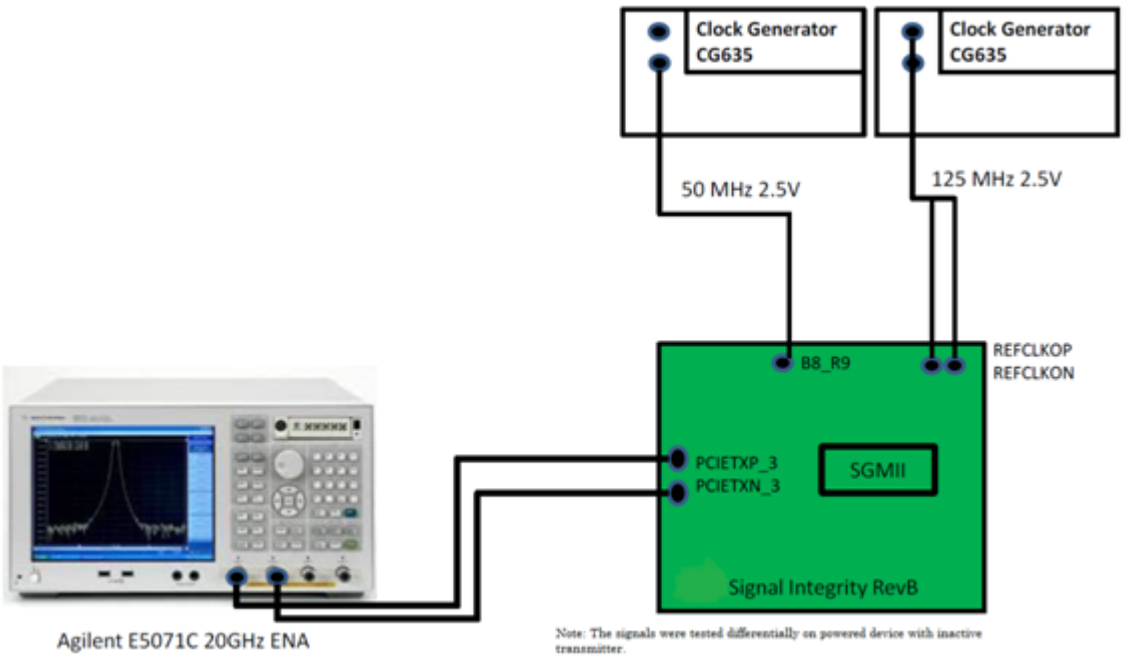

Figure 3: Impedence Test Setup

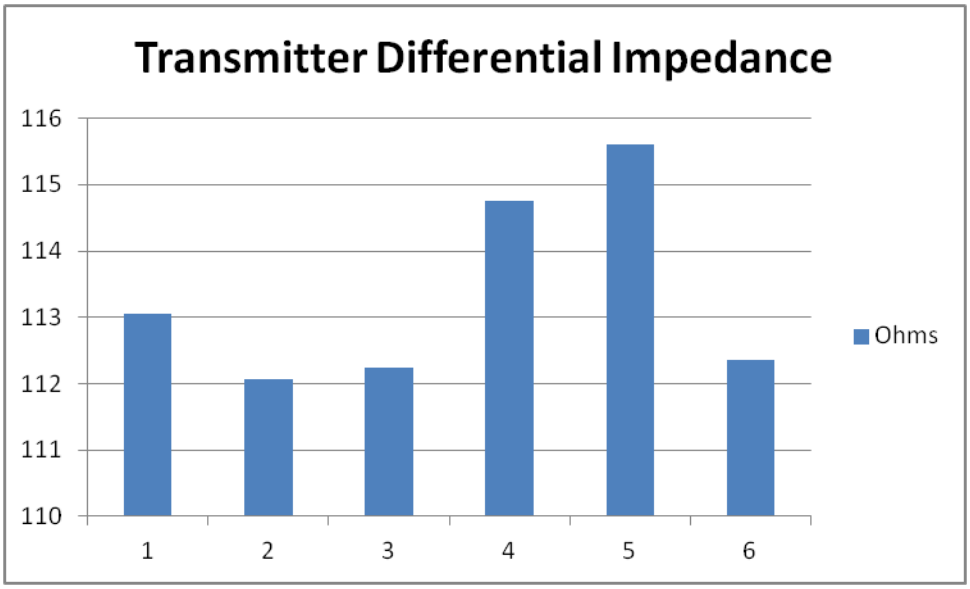

Figure 4: Impedence Test Plot

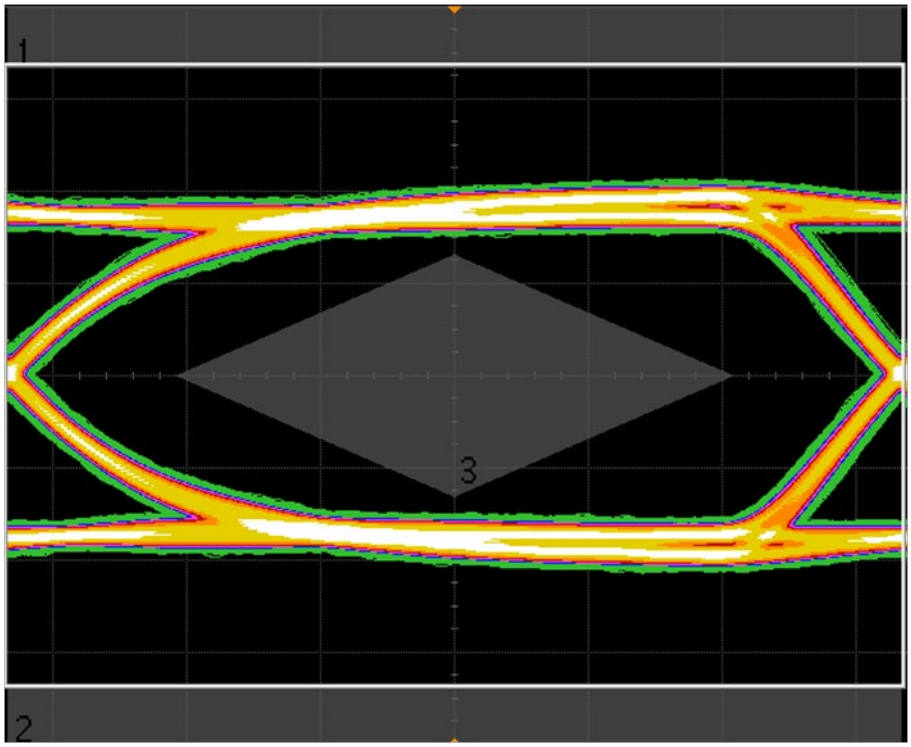

Figure 5: Transmit Eye Mask

Table 5: Transmit Eye Intervals

Symbol	Value	Units
X1	0.25	UI
X2	0.5	UI
A1	675	mV
A2	1725	mV

VII Conclusion

The test results demonstrate that the capabilities of the SmartFusion2/IGLOO2 SGMII GB Ethernet and 1000BASE-X solutions requires high reliability. The report provides a baseline summary of the thorough testing performed by the Microsemi factory to assure users that the device will meet the performance and functional requirements in their customized applications.