Overview

High-energy transients (surges) can appear on data ports and can cause anything from system upsets to hard failure accompanied by charred boards.

Surges have been well known to have caused data transmission errors, memory scramble (mess-up), Process interrupts, program lockups, latch-up/failure in SCR/ICs, power supply failures, hard-disk crashes, and general circuit board failure. Add to that now, more specifically: burnt PHYs, PSEs and PDs.

Interest in Surge events has literally peaked in recent years due to observations and analysis of the phenomenon. Manufacturers, particularly of switches/hubs, have noticed a very strong correlation between products that had been previously observed in internal product qualification testing to have relatively lower, or somewhat compromised surge survival thresholds, and their escalating number of field returns. This correlation grew stronger especially after a storm had passed over a certain area. Data/telecom cables that snake around a building, pass noisy mains wiring, and often go outside too, behave as great antennas. Not only for picking up noise, which we struggle to reject by use of twisted pairs, data transformers, and so on, but for *surges* too.

Surges have a lot of residual energy which can hardly be rejected or washed away by using only twisting cables and other similar solutions. Neither can we afford to ignore it. PoE sections being “front-end” from the viewpoint of an incoming surge on the data lines are relatively vulnerable. Therefore, to avoid a rash of product returns, a keen understanding of what exactly happens during a surge event is required, and is the key to enhancing product reliability and brand reputation.

Approximately 80% of recorded surges are due to internal switching transients caused by turning on/off motors, transformers, photocopiers and so on. Externally generated surges due to induced lightning, grid switching, or from adjacent buildings account for the remaining. Surges which are related to *lightning strikes* in particular can produce surge energies of hundreds of joules. These surges can be the result of a direct lightning strike (very rare, almost impossible to survive), or more frequent cloud-to-ground and cloud-to-cloud discharges. All these events can create a powerful electro-magnetic field which can then capacitively or inductively couple on to the mains wiring and onto LAN/telecom cabling.

ANSI/IEEE C62.41 is a relatively modern standard titled “IEEE Recommended Practice on Surge Voltages in Low-Voltage AC Power Circuits”. Along with UL1449, it has become the de facto standard for characterizing and implementing surge protection. Keep in mind that

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the older version of C62.41 was called IEEE 587-1980, and for years was the go-to reference document on this topic. C62.41 standard lists different waveforms a surge suppresser is to be tested with. It has three categories (A, B, and C), each having three subcategories (1, 2, and 3). For example, it has created the Category B3 ringwave, and also the B3/C1 *combination wave* to represent higher energy internal surges. It also has a Category C3 combination wave (20kV, 10kA), which represents very high-energy surges caused by lightning. A surge suppressor device ("SPD") gets Underwriters Laboratories (UL) 1449 "listing" when it is tested with the C62.41 waveforms and declares its let-through voltage. Let-through voltage refers to the amount of transient voltage passed through a power conditioning unit to the load. SPD ratings range from 330 volts to 6000 volts.

The guiding international (European-origin) standard for Surge waveforms and Surge-protection of equipment is CISPR 24 titled "Information technology equipment - Immunity characteristics - Limits and methods of measurement". CISPR stands for Comité International Spécial des Perturbations Radioélectriques, or loosely translated into English as: "Special International Committee for Radio-electric Perturbations". This standard is advisory in nature, much like the IEC standard for safety, IEC 60950-1. Ultimately all these international standards need to be ratified by local governments and are then accepted as law in that region. So for example, in Europe CISPR 24 became the (mandatory) European norm EN55024.

EN55024 lays down the requirements for surviving surges. But it also refers to another pan-European standard, EN61000-4-5, for the actual test methods and procedures. Based on the EN documents, we arrive at the following summary of requirements for PoE:

a) The mandatory pass level is Level 2, corresponding to ±1kV surge (see Table)
b) The Surge waveform applicable here is the "1.2/50µs" open-circuit voltage waveform, which is the same as the "8/20µs" short-circuit current waveform.
c) The surge should be applied *common mode* (equally, and precisely at the same moment on two or more data lines, with respect to Earth ground).
d) The mandatory minimum to pass is "Performance Criteria B". This allows interruption, but recovery without user intervention.
e) The total source impedance for the surge waveform, as applicable to PoE/Ethernet testing, is 42Ω (that includes 2Ω source impedance inside the surge generator).
f) Five zaps of positive polarity followed by five zaps of negative polarity are required (but *do not alternate the polarity*: that can create up to as twice the voltage swing as necessary).
g) The interval between successive zaps is 1 minute or less (can be set exactly to 60s).

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Level	*Open-Circuit test Voltage ± 10% (kV)*
1	0.5
2	**1.0**
3	2.0
4	4.0
x	Special
Note: x is an open class. This level can be specified in the product specification	

Table 1: Definition of levels as per EN61000-4-5, with mandatory level for Ethernet/PoE bolded (Level 2)

Going beyond the Minimum EN Standards: Higher Voltages

OEMs have shown a strong correlation between field reliability and Surge survivability. The mandatory EN level is just 1kV, but as per data from IEEE 587, we can get hit by 1 surge of 5kV once a year, and 3 to 4kV surges thrice a year (at least in the US). This can be a lot of field returns. So there is an increasing demand for passing surge ratings higher and higher. Several issues arise in choosing the best target to chase in the economical aspect.

How high should we aim? Sparkovers (flashovers) which occur almost naturally in building wiring systems protect most equipment locations for surges above 6kV. So 6kV is the upper limit we should be concerned about. Note that poor or mediocre wiring insulation materials ironically help protect equipment better than excellent and expensive insulator materials.

There is increasing talk about "6kV surge protection". We now realize why 6kV is being picked. However, we should keep in mind that so far such requirements are voluntary. But even if they do become mandatory, note that there are already designated "levels" of surge withstand capability: 2.5kV, 4kV, and 6kV, similar to CISPR 24. So it is probable that much like with CISPR 24/EN55024 we may only need to comply with a level lesser than max.

Incidentally, CISPR 24/EN55024 is now also proposing testing data ports with only the *(softer but wider) 10/700µs profile* (discussed later). But it does have a "loophole" to revert back to the usual 1.2/50µs test (See Table 2, Page 17, footnote "g" of the EN55024-2010 standard: "*where the coupling network for the 10/700µs waveform affects the functioning of high-speed data ports, the test shall be carried out using a 1.2/50 (8/20) µs waveform and appropriate coupling network*").

Meeting high-voltage surge requirements initially means increasing the PCB clearance/creepage requirements. This also means that data isolators/opto-couplers need to be checked carefully for their withstand rating. But the biggest culprit, or "stumbling block", is the "2kV" Y-cap present inside every "magjack" (ICM) port. That takes the brunt

of the entire surge voltage across itself. How can we hope to pass a 4kV test with any certainty, with an *existing* 2kV rated magjack? Yes, with discrete magnetics, that is possible to achieve. But most equipments (switches/hubs and so on) are not built that way any longer. Therefore, for now we are concerned only about achieving up to 2kV surge levels (which is still twice the EN mandatory level).

Recommended Surge Test Setup and Procedure

The surge test procedure is as on the lines of EN 61000-4-5, but we can go to higher voltages. See Figure 1 for a recommended setup which also highlights several key recommendations, particularly for ensuring no "ground loops" and retaining the general integrity for surge testing.

The following points must be kept in mind:

a) Five 8/20µs current surges are applied with positive polarity, and then 5 surges with opposite polarity. Surges are 1 minute apart (or faster).
b) Surges are applied in "common-mode" manner. That is *with respect to earth ground.*
c) The minimum compliance level (mandatory) is ±1kV. We can go to 2kV if desired.
d) The critical factor in the surge setup affecting survivability is the *surge impedance*. It is supposed to be 42Ω for telecom applications.
e) Though not mandatory, it is preferred for the PoE link to remain "up" before and after surge test. Thus the small PD load card draws only 10-15mA, but also contains a LED which should remain lit.

In Figure 2, we show the same setup in a more schematic-specific manner for clarity. We have highlighted the key capacitors involved in the process, and we discuss that next.

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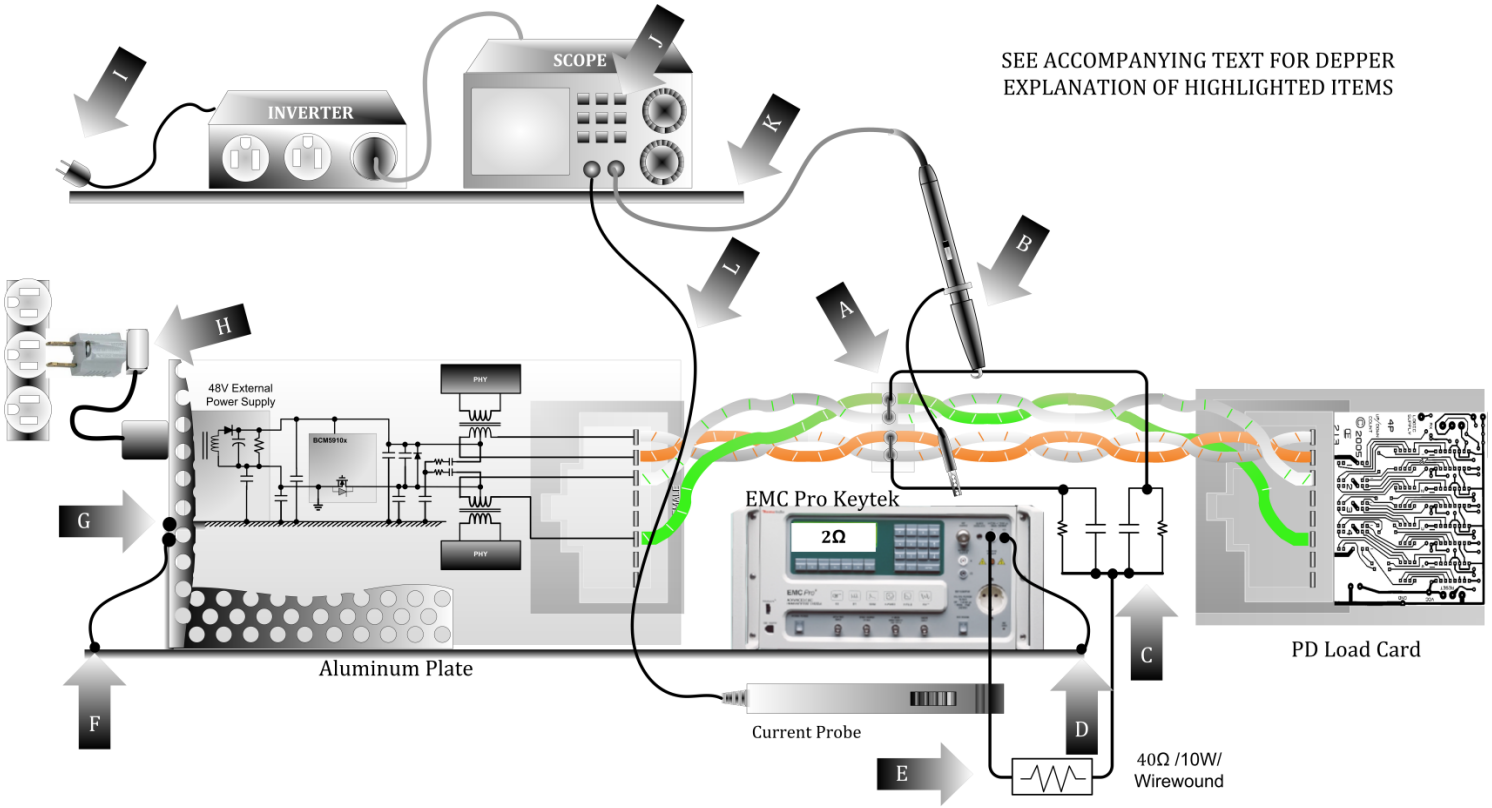

A) A small "breakout board. B) High-voltage scope probe. C) Two metalized polyester or preferably polypropylene high-voltage caps, each of 0.5µF/4kV. Bleeder resistor chain for 1M/4kV. D) Screw firmly to aluminum plate. This serves as the chassis (earth) ground for the Surge test. E) A 40 ohm wirewound resistor combined with 2 ohms from the Surge generator (EMC Pro Keytek) provides a total of 42 ohms surge impedance. F) Screw enclosure of switch/hub firmly to this metal plate. G) The connection on the enclosure which connects to the aluminum plate. H) 3-pin to 2-pin AC adapter plug to disconnect the AC-DC power supply from the Earth wiring (plug this in) I) Unplug AC cord of inverter for the duration of the Surge test. J) Scope floated (on battery power). K) Wooden shelf L) Current probe to measure Surge current.

Figure 1: A Recommended PSE Surge Test Setup with Highlighted Explanations

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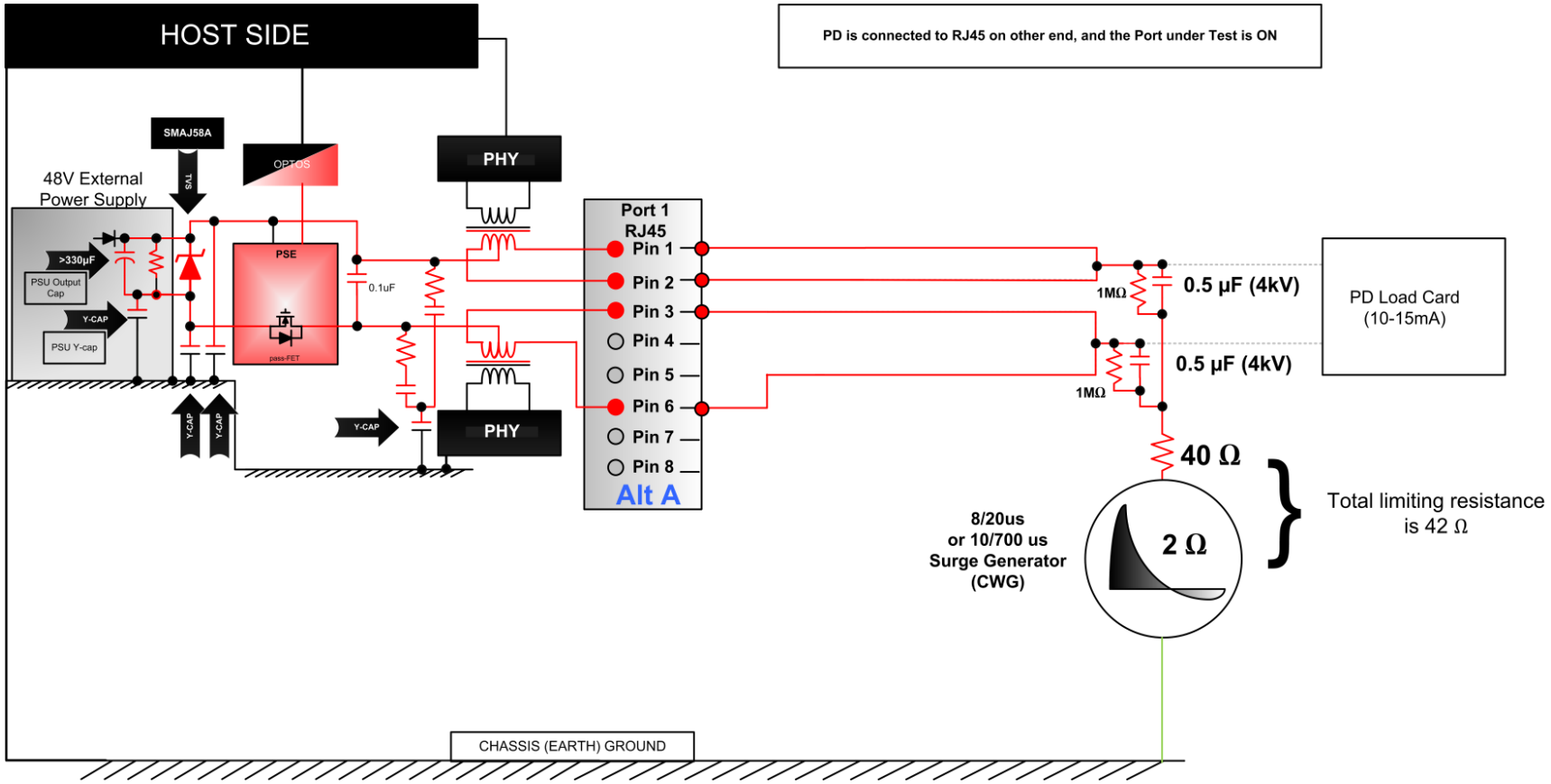

Figure 2: PSE Surge Test Setup as per EN 61000-4-5

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What Exactly Happens During Surge Test

In Figure 1 we indicated that we were monitoring the voltage and current associated with the surge. In Figure 3 we show all the paths of currents during positive and negative surges.

Let us do some simple math around this. If we apply +2kV across a dead short (say the almost uncharged caps at the input or output of the PSE), we will get an instantaneous current of I = V/R = 2000/42 ≈ 47 Amps. This is the *simplified* limit. In reality we can get *much less*. There are two (related) reasons for that. First, the surge voltage does not reach 2000V *immediately*. It takes a few µs for it to get there according to its profile, and things can change quite dramatically during that brief instant. This brings us to the second reason: all the surge current must pass through the Y-caps, so if we reduce the Y-caps, the current will obviously decrease too.

Note: a good test for checking the integrity of our surge setup is disconnecting/removing all Y-caps that we know of, including at terminations and inside the "48V" PSU (power supply unit). If we still see any current using the current probe in Figure 1, there is something very wrong. We should not proceed with the Surge test till all "sneak paths" have truly been eliminated.

The two reasons above are related, as mentioned, because a relatively small Y-capacitance will charge up at least partially during the few µs that it takes for the surge waveform to reach its peak. Eventually, the current at the peak is *less* than the simple calculation 2000V/42Ω = 47A. Now the current will actually be based not on the surge waveform voltage, but on the *difference* between it and the voltage of the partially charged Y-cap. So if the cap had meanwhile gotten charged to 800V, the current when the surge waveform peaks would be (2000-800)/42 = 28.5A instead. This is admittedly intuitive, not a rigorous way of approaching what is truly a complex and *iterative mathematical problem.*

If we reduce the total Y-capacitance, we also significantly reduce the stresses in the PSE circuitry arising from the surge. If we indiscriminately increase the Y-capacitance, or even short it (effectively, from the AC viewpoint), all applied 2kV will eventually appear across the PSE circuitry and will certainly destroy it, *unless we can safely absorb that energy (we will come to that shortly).*

Surges are Applied Common-mode

In a twisted pair scenario, one of the assumptions made is that any incoming disturbance is "common-mode" – picked up equally by two wires with respect to chassis-ground (enclosure). Disturbances are certainly common-mode with respect to the two wires of

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each twisted pair, but the EN standard also assumes that it is applied common-mode with respect to all the wires of the cable.

We realize that the PSE certainly can't get damaged by any *common-mode* surge, *especially if there are no Y-caps present*; unless the disturbance is somehow "differential-mode" across the PoE pairs (positive and negative port rails). Differential-mode surge waveforms are not typically a requirement for PoE or EN61000-4-5, though some more stringent standards like GR-1089 may require it as discussed later. Yet, we do deal with differential-mode *side-effects*. Because even though the applied surge voltage is considered "common-mode" when it is applied, the line impedances are so different on the two rails on which the surge is injected. Therefore this so-called "common-mode" applied waveform gets converted and creates a significant differential-mode component across the positive and negative PoE lines. Eventually this can lead to overvoltage, and that can cause the port pins of the PSE chip (front-end) to burn out.

Having understood this, the obvious temptation is to entirely dispense with all Y-caps on the PoE board. Unfortunately, we need Y-caps for *EMI suppression*. We also do not want the cable to either *emit* excessive EMI, or *pick-up* excessive EMI (susceptibility for data traffic). For the latter, we have the RC terminations on the center taps of the data transformers going to a single Y-cap. But many more Y-caps such as Cpsu, C1 (2×) and C2 (2×) are typically mounted on the PoE board (see Figure 3). Their main purpose is to prevent noise from going *out and on to the data lines* (EMI emission). So we need to stop and ask: where is the noise *coming from*? The PSE is, metaphorically speaking, just a gate that opens or closes for the incoming "48V" DC rails. It can rarely contribute to noise/EMI itself. Yes, the PSE may have some high-frequency on-board clocks for timing or data communication functions, or for on-board data processing, but usually the EMI from all that is insignificant. Basically, any outgoing EMI from the PSE is very likely coming from the PSU, *not the PSE*. So, rather than use brute-force methods like sprinkling Y-caps everywhere, it is better to ask the vendor of the culprit PSU to ensure their PSU has very low EMI also on its output cables. Most ITE (Information Technology Equipment) power supplies are only tested for EMI on the AC mains input lines, but power supplies for telecom applications should actually be tested for EMI on their output lines too (to ease the pain of the end-product systems designers).

Surviving Positive Surges

We realize that *reduction of Y-capacitance is one of the best ways for ensuring surge survivability, especially in AC-disconnect cases.*

The reason for that statement emerges more clearly from a quick study of the current paths under a surge event, as sketched out in Figure 3. Let us discuss this figure in more detail now.

a) In the top half of Figure 3, we are applying a surge of positive polarity from the CWG (combination wave generator) generator to the PoE board. The current paths are shown.

b) Paths "A", "B", and "F" are particularly marked as "dangerous" as they charge the input and output caps of the PSE.

c) "F" is certainly the most dangerous, as a 47A (or 28.5A) current solely passing through Cport (0.1µF) would destroy it immediately.

d) "A" and "B" are paths parallel to "F" and are usually the reason we don't have to worry about path "F" at all. As "A" and "B" go through a very low impedance Cpsu, they divert most of the current through this path rather than "F". Since the value of the capacitance Cpsu is typically very large, even with a 47A or 28.5A surge current through it, it handles it with aplomb, not getting excessively charged. In brief, path "F", despite being marked "dangerous", is actually the savior. This is what happens with DC disconnect. We can fix the amount of bulk capacitance required, as we do in the following sections.

e) *With AC disconnect, paths "A", "B", and "C" are blocked* by a diode in the positive port rail (not shown in Figure 3). So now all the stress can come on Path "F" which charges up the port capacitor. Clearly, such a huge surge current cannot be handled with such a tiny cap and we need to take drastic steps. Steps for *reducing the total Y-capacitance* and for causing the surge current to slow down or stop completely *within the few µs it takes for the surge waveform to peak.*

Surviving Negative Surges

a) In the lower half of Figure 3 we have explained that the *negative* surge test actually creates very similar waveforms to those created by the positive surge test, but only during Part 2 of the test. In Part 1 of the negative surge test, the CWG pulls in current from the PSE. Most of this current comes either through the body-diode of the PSE's pass-FET, or through a Schottky diode (typically 2A/100V) parallel to the FET (placed pointing the same direction as the body-diode, very close to the pass-FET and connected to it by short and thick copper traces see Figure 4). The reason for asking for a paralleled external diode across the PSE's pass-FET is to actually divert the surge current away from the body-diode for protecting the bond wires of the PSE/FET pack. A Schottky bypass diode is used since the drop across this diode must be much less than the drop across the body diode of the FET it seeks to bypass,

so that the surge current will "prefer" this external diode over the internal body-diode. From Figure 4 we see an alternative, much more lossy method can be use. A method which does not require a Schottky, but is however less sensitive to layout or diode characteristics. But neither of these external bypass diode methods is typically required unless a surge capability of more than 2kV is sought (using 8/20µs waveform and 42Ω surge impedance). It is recommended to survive GR-1089 (discussed later). Therefore, a placeholder is recommended on the PCB.

b) If the PoE circuit survives Part 1 of the negative surge test (with the help of a parallel bypass diode, if necessary) then we go to Part 2 of the negative surge test, as explained in Figure 3. This reversal happens when the CWG suddenly raises the voltage at the end of the injection cap to Earth ground. Since injection cap is charged in one direction and cannot discharge immediately, the voltage difference across it is maintained and so its other end suddenly raises. That in effect conducts a positive surge test on the PSE, albeit with somewhat diminished amplitude. In other words, Part 2 of the negative surge test is almost identical to the regular positive surge test. And it too has the potential of creating *overvoltages* (not undervoltages as in Part 1 of the negative surge test). The PSE chip can fail exactly the same way, and so the fixes we propose for the positive surge test apply equally to the negative surge test. The failure modes are almost identical too. *So provided we can ensure bond wires do not burn during the first part of the negative surge test, then all the steps we took to survive the positive surge test will apply to the negative surge too.*

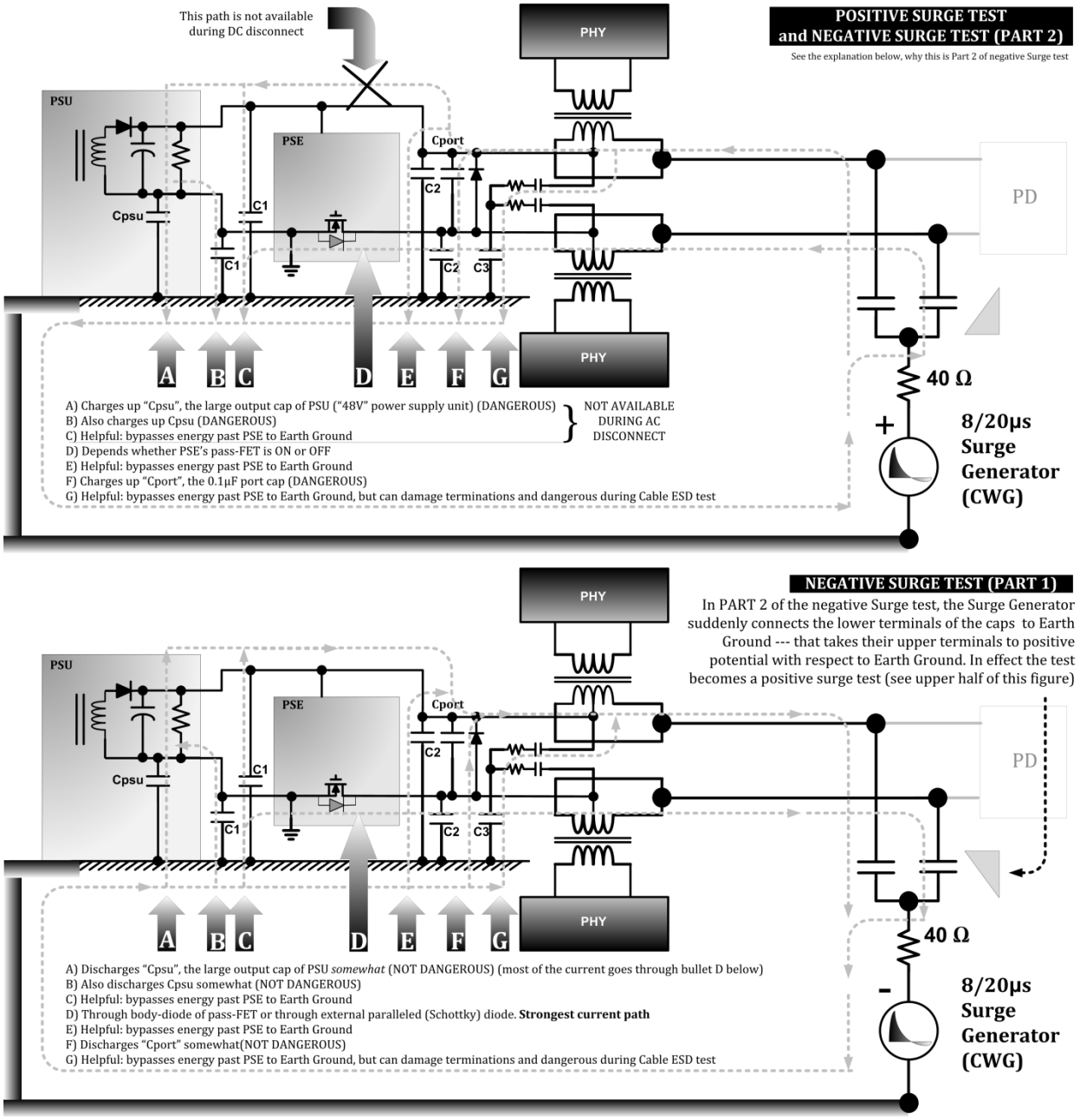

Figure 3: Tracing the Paths of Currents Diring Positive and Negative Surges

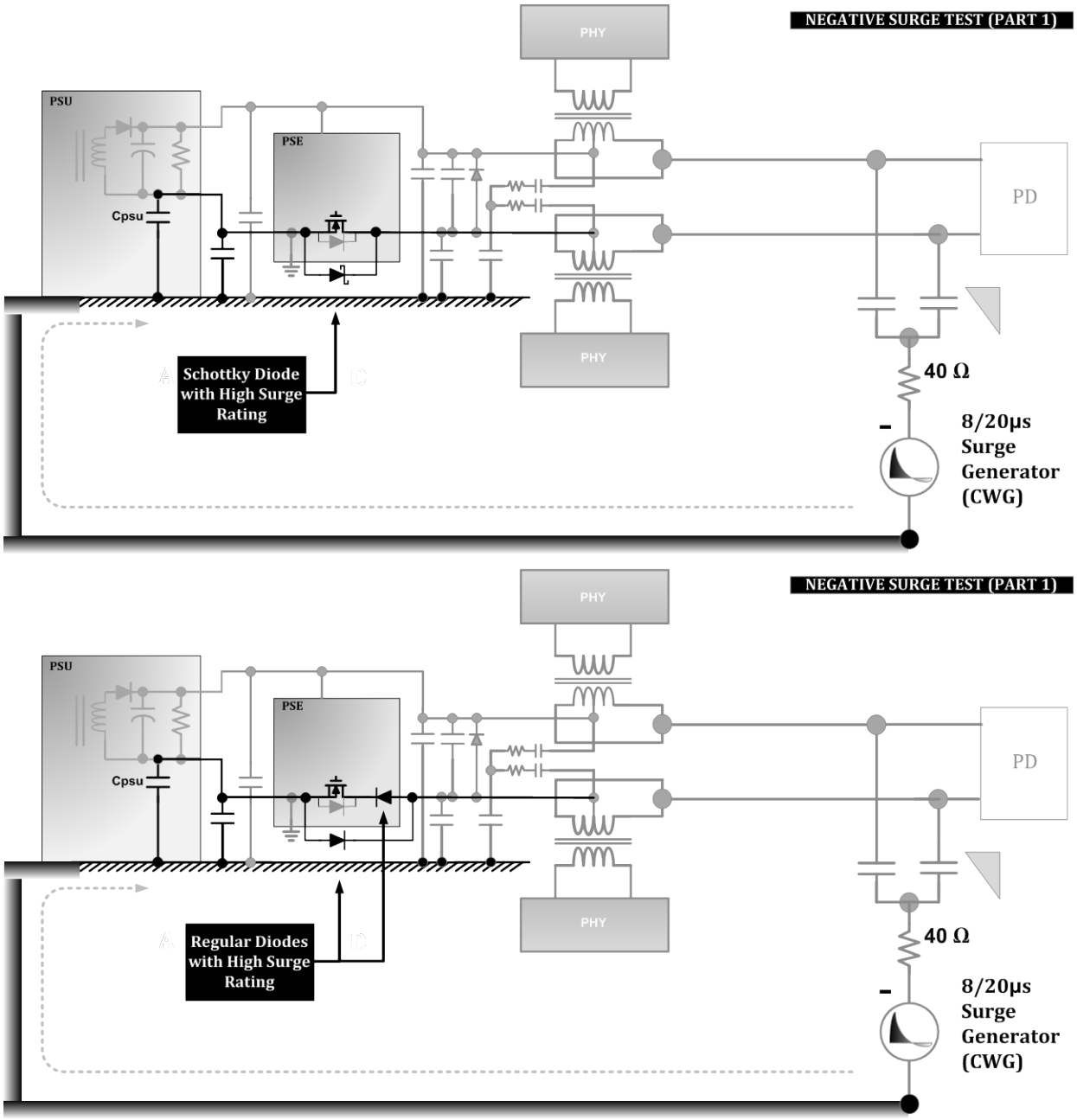

Figure 4: Bypass Diodes to Survive High Negative Voltage Surges

Specific Recommendations for AC Disconnect

The problem with AC disconnect is that access to the bulk cap of the PSU (and input 58V TVS) is denied because of the AC disconnect diode blocking in a reverse direction. The surge waveform can therefore play havoc with the front-end, especially the 0.1µF port caps, and from there to the port pins or FETs.

The easiest way of handling this is to maintain a *small* Y-capacitance. The idea that stands behind it is as follows. The applied surge waveform has a certain dV/dt, and if the Y-capacitance charges up at the same rate or a little faster, we will stay in a "comfort zone". That means that the applied voltage will almost equal the voltage across the Y-capacitance (same rate of rise) on an instantaneous basis. Thus, in effect, there will be no "leftover" voltage which adds to the existing port capacitor voltage. This is the underlying principle here.

Based on a detailed mathematical analysis, we will see that in fact, with a 42Ω surge impedance, the surge voltage waveform peaks somewhere between the open-circuit value of 1.2µs and the short-circuit current value of 8µs. It is actually 3.2µs to be precise. However, it is not a straight line, and based on its initial slope, it actually extrapolates to a 1µs rise time (for any surge voltage peak). We therefore demand that the *Y-cap charge up fully to the max. applied voltage within 1µs*.

$$Cy = \frac{I \times \Delta t}{\Delta V} = \frac{I \times 1\mu s}{Vdc}$$

And I≈ V/R = Vdc/Zext, where Zext = 4Ω (including CWG impedance of 2Ω into this). So

$$Cy = \frac{\cancel{Vdc} \times 1\mu s}{42 \times \cancel{Vdc}} = 24nF$$

The conclusion is that we thus need to *restrict the net lumped capacitance to 24nF for any surge voltage*. See also Figure 5 (top), where this is explained graphically.

This provides the maximum *lumped capacitance* measured between any of the wires coming from the RJ-45, to the grounded enclosure.

Note that with the Y-capacitance sized in this manner, *surge survivability no longer depends on whether the pass-FET is ON or OFF during the surge test*. Therefore path "D" in the top half of Figure 3 needs not to be present. That is good since under a surge event such a huge current passing through FET may in any case cause its protection circuitry to switch it OFF momentarily.

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Recommendations for DC Disconnect

Assuming we have easy access to the bulk capacitor of the PSU with DC disconnect, we can calculate how much energy is being delivered by the surge, and how much bulk capacitance is available to absorb is. We can basically assume a triangular current waveshape of height I_{max} and 120µs (extrapolated duration as shown in bottom half of Figure 5). Then, based on an average current of $I_{max}/2$ lasting for a full 120µs, we can equate the energy delivered by the surge event to the change in stored energy based on $½ \times CV^2$. We thus get 524µF for 3kV. We can also use the following closed-form equation:

$$C_{bulk} = \frac{Vpse \times Imax \times 120\mu}{V_f^{\,2} - Vpse^2}$$

Here V_{pse} is the normal operating PSE voltage (say 51V) and V_f is the max. voltage we want to see on the cap (say 58V). V_f helps keeping headroom for a few additional volts coming from the drop across the ESR of the bulk cap, and finally basws it on 74V Abs Max rating (process limit).

For example, for achieving 2kV surge capability with DC disconnect, the output cap of the PSU must be at least

$$C_{bulk} = \frac{51 \times 43.3 \times 120\mu}{58^2 - 51^2} = 347\ \mu F$$

We can pick a standard 330µF (nominal) value as it is in the ballpark, within calculation's inherent errors/tolerance.

Are there limits on the Y-capacitance in this DC disconnect case? Not much. Since we have calculated *all* surge energy gets absorbed in the bulk cap, we are not relying on the Y-capacitors to charge up and terminate the surge current early. Nevertheless, we should keep reasonable limits on Y-capacitances since they also need to bleed in a reasonable time. Based on that, it was empirically established that a good target is maintaining net Y-capacitance of less than 0.2µF, distributed evenly on the port lines, on any side of the pass-FET. That is a maximum of 0.1µF on each line to Earth ground. We should not forget that the *voltage rating* of these caps must be commensurate with their expected surge voltage capability. Large capacitance values with large voltage ratings are expensive (film caps) and hard to find in general. Ideally they should also have high dV/dt capability and self-healing properties. The best option is to redesign the "48V" PSU for low EMI, as mentioned.

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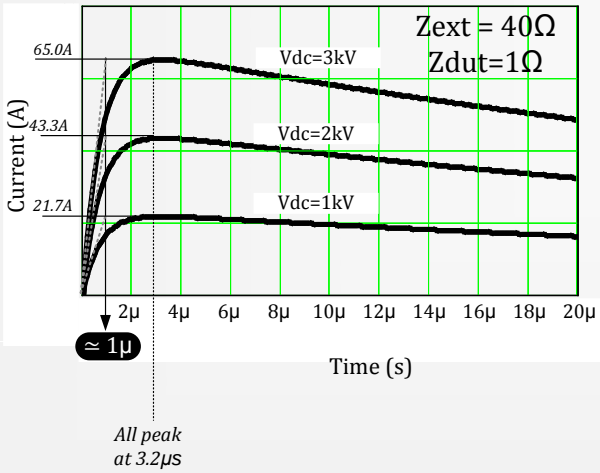
Note that in DC disconnect, the bulk cap can be accessed by the surge from the positive rail (paths "A", "B", and "C" in the top half of Figure 3). So once again *surge survivability no longer depends on whether the pass-FET is ON or OFF*, irrespective of the value of Y-capacitance. In fact, we could have done the Surge test with *no PD load connected*. The results would have been the same (pass thresholds unaltered).

Hint: these can be plotted out using the equations provided, with Mathcad, and plotting Vo(t), since voltage across the 1Ω resistor (Zdut) equals the current through Zdut

Both set of curves below are the same, just different time scales.

AC Disconnect calculations

(bulk cap of PSU not available to absorb surge energy)



The total Ycap "Cy"should charge up exactly at the rate of rise of Surge waveform. Initial rate of rise is V/t where V is the max voltage Vdc, and t is 1µs (extrapolated). So

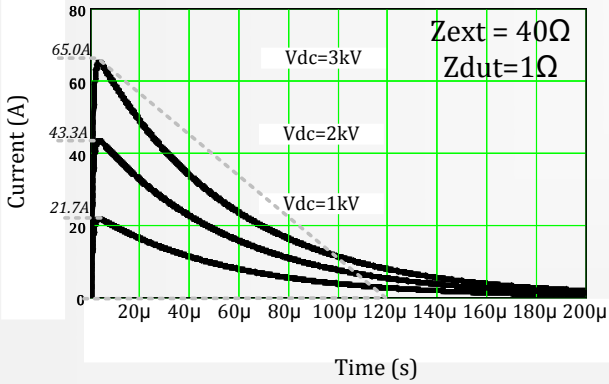
$$Cy = \frac{I \times \Delta t}{\Delta V} = \frac{I \times 1\mu s}{Vdc}$$

and $I \approx V/R = Vdc/Zext$ where Zext = 42Ω. So

$$Cy = \frac{\cancel{Vdc} \times 1\mu s}{42 \times \cancel{Vdc}} = 24nF$$

DC Disconnect calculations

(bulk cap of PSU available to absorb surge energy)



To determine energy delivered, approximate current as shown. For example, we can then say that for Vdc = 3kV, the current is an average of 65A/2 = 32.5A for 120µs. So Joules is V x I x t = 51V x 32.5A x 120µs=0.2 Joules.

If this is to be absorbed in the bulk cap, and it is allowed to go from 51V to 58V, we get

$$\frac{1}{2} \times Cbulk \times (58^2 - 51^2) = 0.2$$

Solving

$$Cbulk = \frac{2 \times 0.2}{(58^2 - 51^2)} = 524\ \mu F$$

For 3kV Surge capability

Similarly, for 2kV surge capability, we get 348 µF

Figure 5: AC and DC disconnect Recommendations

Surviving the 10/700µs Surge Test

The most recent version of EN55024 standard now seems to ask for testing immunity of telecommunication lines. This is done using a CWG with an open circuit voltage waveform of 10/700µs (the corresponding short-circuit current waveform is of 5/320µs). This is an alternative to the usual 1.2/50µs open circuit voltage (8/20µs short-circuit current) test. EN55024 also states that the 10/700µs test is "*applicable only to ports which according to manufacturer's specification may connect directly to outdoor cables*" (see Table 2 of the EN55024 standard). It also provides another loophole of sorts in the footnotes of Table 2, where it states that "*where the coupling network for the 10/700µs waveform affects the functioning of high-speed data ports, the test shall be carried out using a 1.2/50 (8/20) µs waveform and appropriate coupling network*". Keep in mind that Ethernet and PoE are in effect built around indoor cables. So the applicability of the 10/700 µs waveform to PoE is not very clear. Nevertheless here are the pros and cons and ways to meet the requirement, if so desired.

a) The first thing to look for is the specified impedance of the surge generator. The EN55024 standard specifies is to be 40Ω as previously. So the short-circuit currents are the same as before: I=V/R = 1000V/40Ω=25A.
b) However, we also know that if our total Y-cap is small enough (<25nF), we manage to charge up the Y-cap in about 1µs with that level of short-circuit current dt =(C/I) dV = (25n/25A) × 1kV = 1µs. So in 1µs the surge current flow would stop entirely because the Y-cap was *fully charged*. Looking at it dynamically, it meant that with a 1.2/50µs waveform, the Y-cap charged up at almost the same rate as the rising voltage waveform. So there was no significant voltage accumulating differentially across the PoE lines and PoE circuitry. Now, with an even slower rise time (between 5 and 10µs as with the new 10/700µs profile), as proposed by the recent EN55024 standard, we can essentially increase the Y-cap *by at least 5 times* (to 125nF) and still be well-protected by the simultaneous charging up of the Y-capacitance. In other words, the softer "attack time" of the new profile actually allows us much higher Y-capacitances for the same PoE voltage stresses. That is true for both AC and DC disconnects. So for that reason alone we can say "*in the case of limited Y-capacitance, the 10/700µs profile is actually an easier test to meet than the 1.2/50µs test*".
c) But if the Y-cap is not controlled, we have to imagine that the surge current continues as long as the surge waveform is applied. So in this case, no Y-cap charges up causing the surge current to stop. This case would occur if there was a dead short between PoE ground and chassis ground. It is worst-case, but impracticably so.

However, assuming this worst-case for now, if we have to store the entire surge energy in the bulk cap (at the output of the AC-DC power supply), we can calculate that we need at least 347µF bulk capacitance for passing 2kV of (1.2/50µs) surge. That is *with no limit on the Y-capacitance* and when using DC disconnect (so that the bulk cap can be accessed by the surge). The equation to use is

$$C_{bulk} = \frac{Vpse \times Imax \times 120\mu}{V_f^2 - Vpse^2}$$

The 120µs is based on the extrapolated decay curve of the 1.2/50µs waveform. Keep in mind that this equation assumes that the short-circuit current is an average of $I_{max}/2$ for the entire duration of the surge. We can now redo the same calculation using only 25A (for 1kV as per EN55024) but this time using an extended time of 1000µs (based on a half-point value somewhere between the open-circuit voltage value of 700µs and the short-circuit current value of 320µs). We get

$$C_{bulk} = \frac{51 \times 25 \times 1000\mu}{58^2 - 51^2} = 1670\mu F$$

This corresponds to dumping the *entire* surge energy into the bulk cap (for very large Y- Caps – like a short between PoE ground and chassis ground). This requires access to the bulk cap, so we need DC disconnect to be able to use the bulk cap to absorb the surge energy safely.

A more practical alternative is reducing the Y-cap (to ~ 100nF) too, and that would once again significantly limit the required energy to be stored in the bulk cap. So we would then be able to achieve 1kV surge protection for the 10/700µs waveform, even with a small bulk cap (~10µF), and *with both AC or DC disconnect*. So the best way is controlling the Y-capacitance, as we have constantly recommended. This applies especially for AC disconnect but now also for DC disconnect, so as to avoid using impractically large bulk capacitance values.

If we do happen to have DC disconnect, we could in principle increase *both* Y-cap and bulk capacitance *together*, starting from 100nF and 10µF respectively, but this time very judiciously. That would lead to a practical solution to meet the 1kV-10/700µs requirement (if applicable).

Protecting the PD From Surges

In a similar manner, we can test the PD for surges too. The logic is the same actually, because looking in from the cable, the PD looks (coincidently) very similar to the PSE. We "see" a bunch of Y-caps, a port cap of 0.1µF, a TVS, *and also a bulk cap*. The latter being the input cap of the DC-wired in DC disconnect, The DC converter that follows. See Figure 6. *Just as in the case of a PSE.*

This leads to an equivalent circuit akin to a PSE with DC disconnect, so it should be handled the same way too. In particular, to handle 2kV surge, the electrolytic bulk cap at the input of the DC-DC converter must be 330µF, just as for a PSE.

But the bulk cap can be much less too since in a PD we may be able to reduce the Y-capacitance significantly. In very rare cases a low-power PD may in fact have *no* connection to Earth ground. It may even have a two-prong AC plug. However, since it has a DC-DC switching converter inside it, elimination of Earth ground may pose serious problems meeting EMI radiated and conducted emission limits. The PD may be encased in plastic and have no user accessible metal surfaces, allowing loosening the isolation requirements. Yet for conforming in particular to radiated EMI emission limits, there will likely be a metallic foil or metallic spray coating inside the plastic, and this would need to be connected to the Earth ground (through the middle prong of an AC plug). So even though the Y-capacitance in a PD may be significantly less than a multi-port switch (in which all of the Y-caps of the magjacks aggregate together), the Y-capacitance of a PD cannot be eliminated altogether. That said, it is much easier for a PD to survive Surge testing than a PSE, and this is the reason. If the Y-cap charges up quickly, and we have calculated that 24nF will charge up fully within 1µs, the surge current flow will stop, and we will be able to reduce the bulk cap from 330µF to much less than 180µF, which is a threshold considered desirable for PDs, concerning Inrush and Power-up. But for that, we have to minimize the Y-capacitance significantly.

How high should the PD's voltage rating be? It seems to have become fashionable for PD chip vendors to almost brag about their "100V" process, and the excellent field reliability of their PD's as a result thereof. However, as mentioned, the PD survives the surge test much more easily than the PSE usually does. And when a surge strikes, it is on a cable that has a PSE on one end and a PD on the other. They are effectively in parallel from the viewpoint of the surge. Further, the weakest link is usually the PSE. And if that can survive (with some design skill and almost no added cost) using just a typical "74V" fabrication process, why do we need a 100V process for a PD which already has much reduced Y-capacitance to start with? Keep in mind that in the case of a PSE with DC disconnect in it, the >330µF bulk

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capacitance of it *will fall across the line* during a surge, and will absorb the surge energy, protecting the PD in the bargain, which is effectively just in parallel with the PSE.

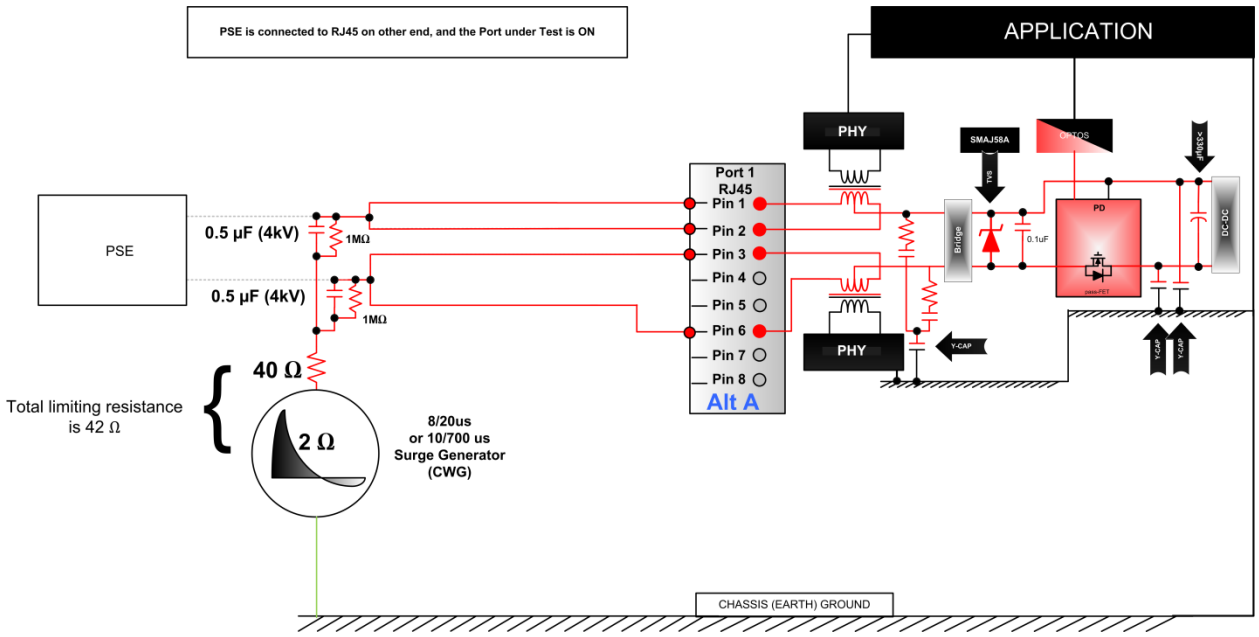

Figure 6: PD Surge Test Setup as per EN 61000-4-5

Semiconductors for Protection

So far, we have deliberately avoided mentioning the "58V" TVS (transient voltage suppressor), habitually placed on the PD and PSE. The question is: how much good does it really do?

Despite the common belief, its use is actually limited. *In fact it cannot even work on its own*. The reason is that this diode has a max. peak current rating of only 4.3A, whereas the measured surge currents are closer to 20-40A at 2kV, depending on the amount of used Y-capacitance (it can theoretically be as high as 2000V/42Ω≈ 50A with higher Y-capacitances). Further, with only 4.3A max passing through it, this TVS clamps not at 58V as commonly assumed *but at 93.6V*. So not only is its current rating inadequate, so is its voltage rating (and its energy rating too). Basically, the TVS works only to *supplement* the bulk cap's action as previously discussed. Since the bulk cap is usually physically far, with long traces or wires intervening, and there may even be an ill-advised common-mode filter en route as discussed, TVS serves to clamp the voltage to a safe value *till the bulk cap starts to act*.

So TVS serves only to absorb *high-frequency* spikes, or just the *incoming edge* of the lightning surge waveform. And yet, it is also not so quick, because a typical PSE contains several controller chips all sharing the same TVS (at their common input). Further, the TVS needs to be physically close to all the chips for maximum effectiveness (low intervening trace inductances), but that is impossible. The TVS cannot be close to *all* PSE chips at the same time. We will typically put it in roughly at the center of several PSE chips, but it cannot service all of them well. Therefore, we also need *local decoupling* at the chip level till the TVS itself starts to act. And that takes the form of 0.1µF ceramic caps (X5R or better) placed on each chip.

Note that vendors of protection devices have a bunch of products they claim to solve all problems in Surge protection. There are, for example, diode+TVS (bidirectional clamping) arrays with ultra-low capacitance too. These will not affect data and therefore can be placed directly across the two wires of a twisted pair just as it comes into the RJ-45. Then there are also diode+Sidactor arrays. A Sidactor is similar to a thyristor or a gas discharge tube. On being triggered, it crowbars to a low voltage, pulling in a lot of current (usually intending to blow out a series fuse and thereby rendering the equipment non-operational, but "safe"). We also have MOVs (metal oxide varistors) in SMD packages nowadays, and so on. But these are still habits of the past. Such arrays/devices were used to protect ISDN/DSL/telephony lines for years. In applying them to PoE, we need to keep in mind the following points.

a) A voltage differential across a twisted pair will not affect PoE since PoE is at the center tap of the transformer (symmetrical). This voltage differential, however, can certainly get transmitted across the data transformer's isolation barrier and damage the PHY. But for that we can actually put the protection arrays on the PHY-side, closer to the chip they are protecting. It is not a PoE issue in any case. We can also wonder how the voltage appeared differentially across a twisted pair to begin with.

b) We can put bidirectional diode protection array from one of the data lines, or one of the PoE lines, to Earth ground, in an effort to shunt away the surge energy. But we are very likely to fail the mandatory Hi-Pot test, unless we also use some questionable "loophole" that the Asian vendors claim. Disconnecting all Line to Ground TVS arrays before a Hi-Pot test, then reconnecting them after passing the test. This seems to be common practice at some major Asian ODMs. Does it protect the user from an electrical shock? No, unless the TVS is rated to withstand 2.5kV.

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c) Almost out of force of habit, some ODMs are also known to have placed an expensive bidirectional TVS across the PoE port (from Port_P to Port_N). However they did not realize that there is a reverse polarity protection diode in parallel, and since it conducts in one direction anyway, there is just no use of bi-directional protection parallel to it. See "Path A" in Figure 7.

d) Some PSE vendors replaced the reverse polarity protection diode with a 58V TVS, same as the TVS at the input of the PSE. This has questionable advantages, but some major OEMs believe it helps. However, take a look at Path B in Figure 7. If the bulk cap is there to absorb the surge energy, does the TVS really help (in DC disconnect)? Let's not forget that there is a high-frequency port output cap present for the short duration in which the bulk cap comes into play.

e) Keep in mind that a weak front-end "protection" can do more harm than good if it fails prematurely at lower levels of energy. And *any* component failure, wherever it comes from, will bring down the entire switch/hub. So, we must make sure that in the most hazardous locations, such as those closest to the RJ-45, we place not the weakest, but the *toughest* protection devices. Most semiconductors do *not* have the ability to sink a lot of energy, and will develop internal hot-spots and melt. So in this case we recommend to let the energy in, and then let it be fully absorbed by the PSU's output bulk cap.

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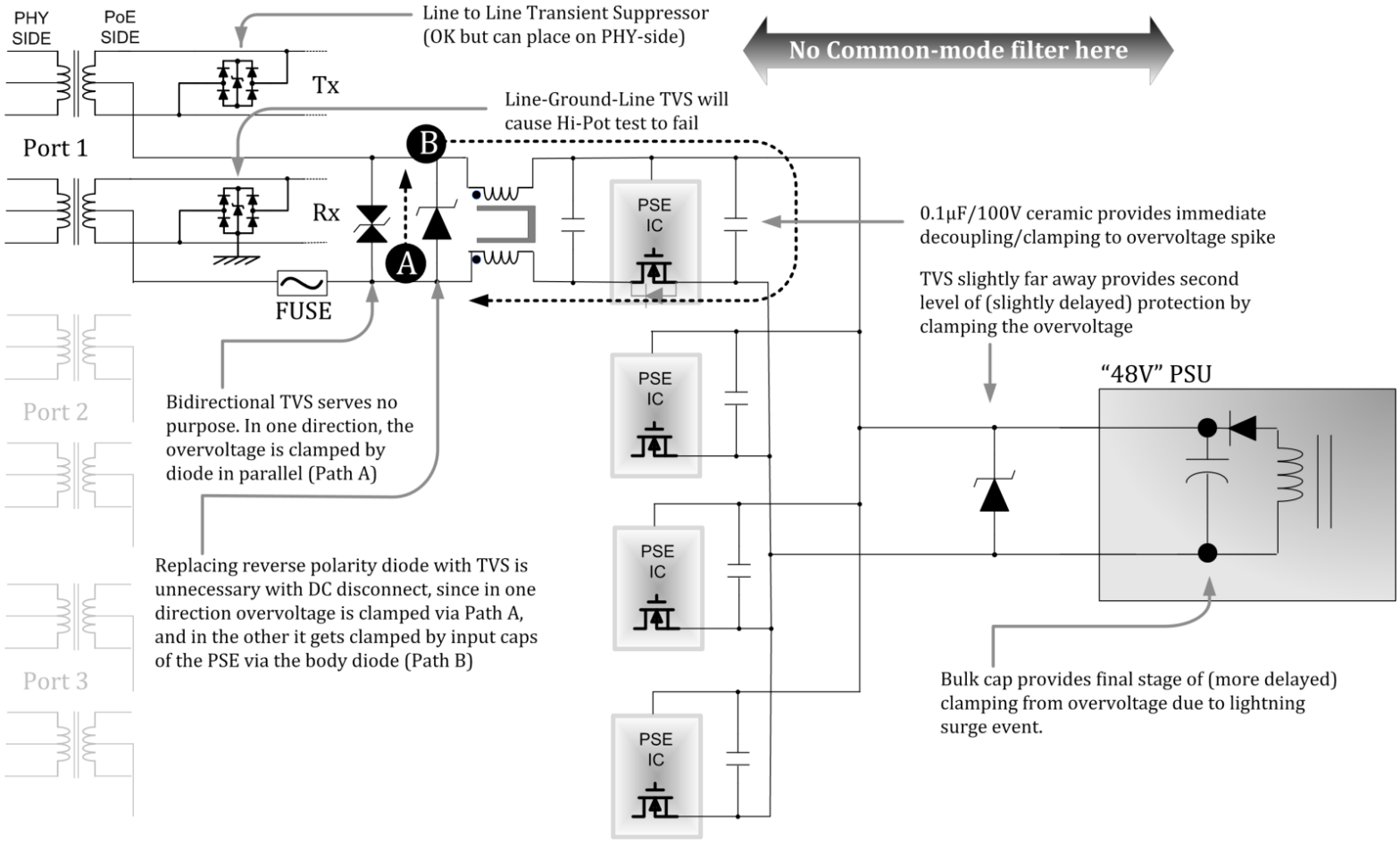

Figure 7: Surge Protection Devices

Microsemi
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PoE is an IntraBuilding Standard

PoE is an essential intra-building standard. There are some confusing references in IEEE802.3at to "Environment A" and "Environment B":

In Section 33.4.1.1, titled "Electrical isolation environments", and in Section 33.4.1.1.2:

There are two electrical power distribution environments to be considered that require different electrical isolation properties. They are as follows:

- Environment A: When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.

- Environment B: When a LAN crosses the boundary between separate power distribution systems or the boundaries of a single building….

…..

Environment B requirements: The attachment of network segments that cross Environment A boundaries requires electrical isolation between each segment and all other attached segments as well as to the protective ground of the NID.

Just above that, in Section 33.4.1, it says:

Conductive link segments that have differing isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of network interface devices (NID).

The truth is no one seems to really know how to maintain port-to-port isolation effectively or economically. Do we need separate 48V supplies for each port? In effect, PoE standard has remained Environment A (intrabuilding).

Keep in mind that even if a tiny section of the Ethernet cable goes out, for example to an IP camera mounted on the outside wall of the building, the environment is no longer Environment A. And technically speaking, we have equipment designed for Environment A operating in an environment it wasn't designed for. Furthermore, it is now far more intensely exposed to atmospheric discharges. Warranty should not apply in this case.

GR-1089 (Telcordia) Requirements

GR-1089-Core (1999) standard relates to testing of lightning and AC power fault surges in a telecommunications central office environment. It requires “primary protection” from surges and lightning strikes at the service entrance. But there is some “let-through” which is handled by “secondary protection”.

Primary protection is the first line of defense. It is required at a facility's (service) entrance. Several means are employed to implement it. Carbon blocks are the oldest type of overvoltage protective device, originally used to protect against overvoltage in telephone installations. They work by forming a spark gap with two pieces of carbon in close (3 to 6 mils) proximity. The gap flashes over at around 600V. One side is tied to earth and the other to the circuit being protected. Carbon blocks unfortunately degrade with each use, and the only indication that they are not working anymore is *equipment damage*. So gas discharge tubes are often used instead. These are sealed and rely on electrodes in a mixture of noble gases (argon, neon, and so on). The voltage across them collapses when they breakdown, allowing them to carry huge current with limited self-dissipation – thanks to the lowered voltage (dissipation is V × I). These are widely used for primary protection. Solid-state crowbar (thyristor-based) devices (similar to gas discharge tubes) are also used to clamp transient voltages. They have a fast response time, low capacitance, and high reliability. They are an excellent choice in protecting telecommunication lines. The three devices mentioned above take care of overvoltage conditions. Overcurrent conditions are sometimes handled by fuse links. But fuse links are not intended to provide a current limiting function for network equipment. That is the job of the secondary protection.

After being clamped by primary protection, some energy gets through anyway. So we need secondary protection. Secondary protection involves the use of overvoltage and overcurrent devices. Examples are (smaller) solid-state crowbar devices, gas discharge tubes, and metal oxide varistors (MOVs). Overcurrent devices are used to interrupt harmful currents, or to provide high impedance to the protected circuits. Examples are fuses, PTCs (positive temperature coefficient polymeric devices), power/line feed resistors, or flameproof resistors.

We must be clear that there will (soon) be no telecommunications network without primary and secondary protection. Therefore Bellcore (now Telcordia) developed a series of tests that go beyond the upper voltage and current limits equipment normally sees. The underlying philosophy is the same as the one we had declared in going well beyond EN61000-4-5 and CISPR24 requirements. This adds margins to the test requiring a robust

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piece of network equipment. The logics says that if a piece of network equipment can survive the Telcordia tests, it will survive in the field for many years.

Let us look at what all this specifically means in terms of protecting PoE equipment (inside the building) from surges. It turns out that GR-1089 is actually not much different than EN61000-4-5/CISPR24. In Section 4.5.9 under "Intrabuilding Lightning Surge Tests" it specifically mentions that a 8/20µs generator can be used as per the standard "IEEE C62.41", which is actually the underlying standard for EN 61000-4-5 too.

The differences between EN61000-4-5/CISPR24 and GR-1089 are:

a) GR-1089 standard asks for only ±800V (1 zap) with a 6Ω resistor, and the next level is ±1500V (1 zap) with a 12Ω limiting resistor.
b) In contrast, EN6100-4-5/CISPR24 asks for only 1kV minimum with 40Ω, and 5 zaps of positive polarity followed by 5 zaps of negative polarity.

Doing a mathematical analysis, with Z_{dut} = 6Ω and V_{dc} = 800, we get peak current as 84A. Then using Z_{dut} = 12Ω and V_{dc} = 1500, we get the peak current as 94A. This is significantly higher than EN standards. But in a similar fashion, we can calculate the bulk capacitor requirement in going from 51V to 58V to be 754µF (for a 94A peak). If we allow higher maximum voltages, up to 65V, we get 354µF, same as we got for EN6100-4-5. To support this without blowing up the TVS, we need to be able pick an 80V process for the PSE chip, or we should ensure really low ESR in the bulk cap of the PSU. We may need to parallel several 80V/100V bulk caps, and/or add ceramic caps in parallel at the output of the PSU. This will significantly reduce the effective ESR and the corresponding "ESR bump" which will get added on to the 65V assumed above. If we do all these, we can continue to stick to our previous 330µF recommendation. Basically, *this entails better design of the PSU, not the PSE.*

Once again however, *the best method is to control the Y-capacitance*. Since the charging currents are much higher in this case, we can actually use that to our advantage. With a higher charging current, the Y-cap will charge up much faster and will take up all the voltage across itself very quickly by the time the slower-rising surge voltage waveform peaks. That actually allows us to somewhat increase the maximum Y-capacitance, because we don't need it to charge up in less than 1µs – roughly the same target as for meeting the EN standards.

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Revision Level / Date	Para. Affected	Description
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