TN205

Surge Protection Application Note

8-Port PSE PoE Manager PD69208T4/M/4T4

November 2019

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 0.6

Revision 0.6 was published in October 2019. The following changes were made from the previous revision

- Update protection circuits for ITU-T.K21 - 2018
- Add support of IEC62368-1 ED 3
- Remove excessive information concerning standards
- Formatting updates

1.2 Revision 0.5

Revision 0.5 was published in July 2016. The following changes were made from the previous revision

- Replace the app schematic.
- Varistor instead of Sidactor
- Replace setup 1 and 8, port ON drawing.

1.3 Revision 0.4

Revision 0.4 was published in June 2016. The following changes were made from the previous revision

- Revised Figure 23

1.4 Revision 0.3

Revision 0.3 was published in March 2016. The following changes were made from the previous revision

- Add new Figures
- Add new components in the application

1.5 Revision 0.2

Revision 0.2 was published in March 2015. The following changes were made from the previous revision

1.6 Revision 0.1

Revision 0.1 was the initial release, published in February 2015. The following changes were made from the previous revision

2 Introduction

2.1 Scope

This document provides design guidelines to sustain high voltage/current surges per relevant immunity standards using Microsemi PD69208T4, PD69208M and PD69204T4 PoE managers. Note that throughout this document we have listed "PD69208", however all tests and schematics are applicable to all three Managers (PD69208T4, PD69208M and PD69204T4).

2.2 Overview

Surge immunity is a basic feature required within telecommunication systems in order to increase system reliability when exposed to a surge event. When designing surge protection, it is common to check if the required installation of the telecommunication cable is located indoor or outdoor. Surge protection is usually divided to two protection stages:

- Primary protection deals with high energy surge and is usually located between EUT (Equipment Under Test) and external cable subjected to surge event, however it can be implemented at the EUT front end. It is used mostly for outdoor cable installation.
- Secondary protection deals with lower surge energy and is usually located within the EUT front end. Secondary protection is used mostly for indoor cable installation and for residue energy from the primary protection circuit
- This design guide is intended to assist the designer to implement primary protection mechanisms for protection from outdoor surge events that is consistent with the listed standards.

Many standards around the world define different surge voltage levels, source impedance and maximum current Surge requirements are system requirements and need to be tested on a system level. This document contains recommendations for the system containing the PD69208 IC to enable the system to meet POE surge requirements of following standards. **It is critical that the system designer validate their solution via actual system level test prior to mass production or field deployment.**

- ITU-T K.21 – 2018
- IEC61000-4-5 - 2014
- EN55024 - 2010
- GR1089 Issue 6
- UL/EN/IEC 62368-1 ED3

Disclosure: an outdoor surge event in this document points to equipment that whose telecommunication cables are located outdoor but the equipment itself is located indoor. For equipment that is located totally outdoor additional regulations must be complied with such as waterproof, AC input line protection, etc.

3 Relevant Standards and Tests

#	Standard	Test circuit waveform	Enhanced level [+/-V]	Basic level [+/-V]	Tested channel condition	Coupling mode	Test Circuit
1	ITU-T K21 2018 Test 2.1.11	1.2/50-8/20 µs R1=10 Ω R2=10 Ω	6000V	2500V	Channel OFF	Differential Mode	Figure 1
2	ITU-T K21 2018 Test 2.1.8	1.2/50-8/20 µs R=10 Ω	6000V	2500V	Channel OFF	Common Mode	Figure 2
3	ITU-T K21 2018 Test 2.1.4a	10/700 µs R=25Ω	6000V	4000V	Channel ON and OFF	Common Mode	Figure 3
4	IEC61000-4-5 2014	1.2/50 µs	N/A	0.5kV	Channel ON and OFF	Common Mode	Figure 4
5				1.0kV			
6				2.0kV			
7				4.0kV			
8	EN55024 2010	10/700 µs	N/A	1.0kV	Channel ON and OFF	Common Mode	Figure 4
9				4.0kV			
10	GR-1089 Core 6 2011	1.2/50 µs R=6 Ω	N/A	800V	Channel OFF	Differential Port type 3b/5b	Figure 5

Table 1 Relevant Standards and Tests

Notes:

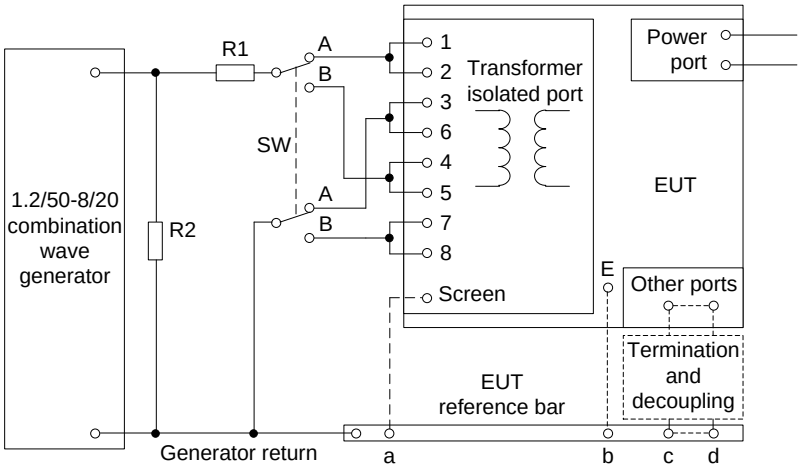
[1] – Port status during the test

- Criteria A – If the channel is ON, it stays on during the event.
- Criteria B – If the channel is ON, it is turned-off during the surge and automatically recovered.
- During all tests, the Criteria for the “neighbors” activating ports next to the tested port is A.

4 Test Circuits

4.1 ITU-T K21–2018

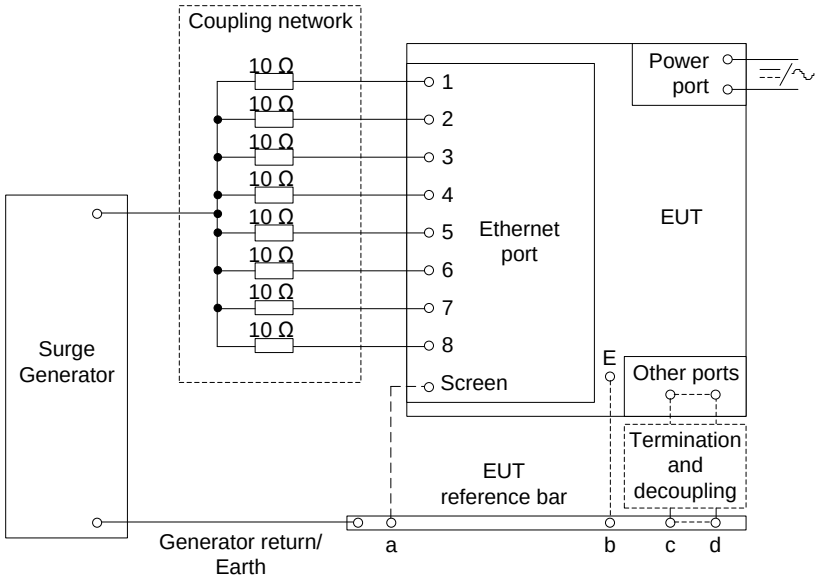
4.1.1 Test Circuit per ITU-T K.44 A.6.7-2 for Test Set #1 in Table 1



SW in position A: Test PoE Mode A powering terminals 1/2 - 3/6
SW in position B: Test PoE Mode B powering terminals 4/5 – 7/8
a=RJ45 screen cable connection
b=EUT protective or functional earth connection
c to d =Terminals of all other signal ports
1,2,3,4,5,6,7 and 8 are Ethernet RJ45 pin numbers
R=series current limiting resistor
R2=optional shunt resistor
Note- For power sourcing equipment (PSE), midspan power insertion equipment and powered device (PD) ports test in Switch (SW) positions A and B. If the PSE specifies the powering pairs, then the testing is only done on those pairs.

Figure 1 - PoE port powering pair transverse/differential surge test circuit

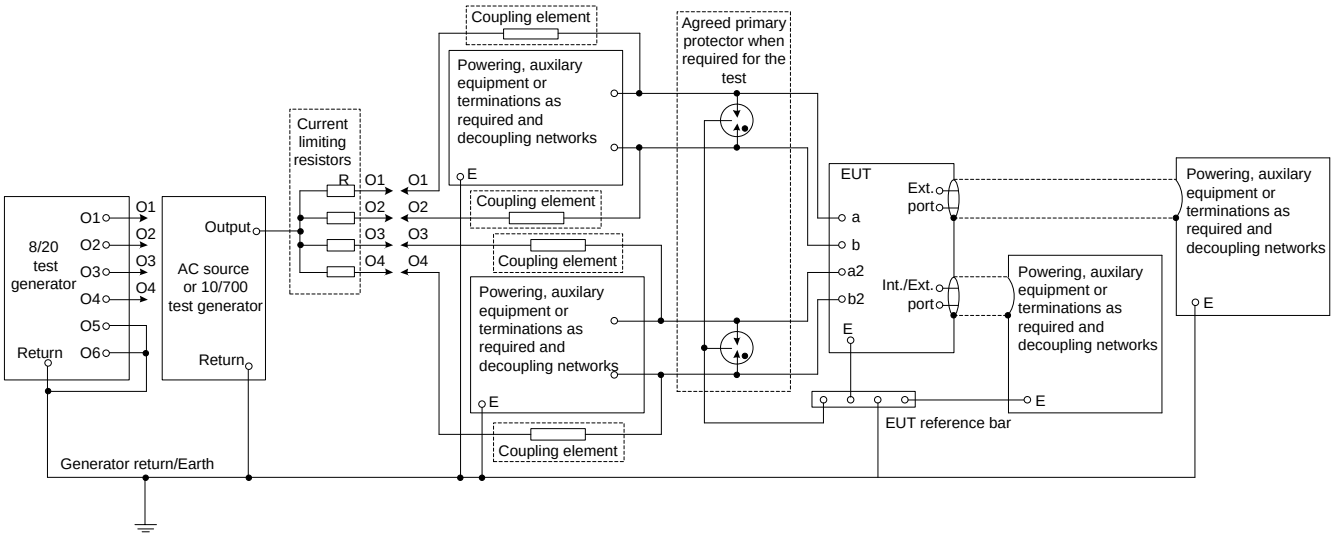
4.1.2 Test Circuit per ITU-T K.44 A.6.7-4 for Test Set #2 in Table 1



1,2,3,4,5,6,7 and 8 are Ethernet RJ45 pin numbers
a = RJ45 screen cable connection
b = EUT protective or functional earth connection
c to d = Terminals of all other signal ports

Figure 2 – Ethernet port longitudinal/common mode surge test circuit

4.1.3 Test Circuit per ITU-T K.44 A.6.1-4 for Test Set #3 in Table 1

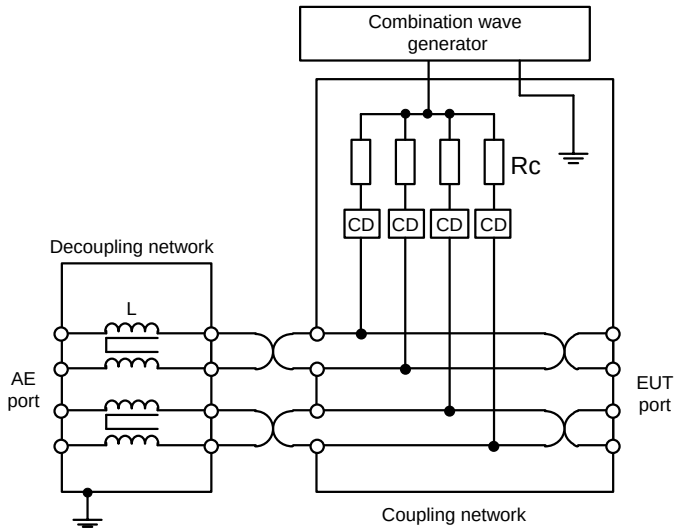


EUT earthing is as follows:
1) If the equipment has an earthing point, connect this point to the EUT reference bar;
2) If the equipment has a conductive case, but does not have an earthing point, connect the case to the EUT reference bar;
3) If the equipment has neither an earthing point nor conductive case, let the equipment float.

Figure 3 - Overvoltage or overcurrent on an external multiple symmetric pair ports to earth test circuit

4.2 IEC61000-4-5-2014

4.2.1 Test Set Up for Test Set #4, 5, 6, 7, 8 & 9 in Table 1



Calculation of coupling resistor values Rc:
Example for n = 4:
Rc = 4 X 40Ω = 160Ω
The coupling resistors values are selected so that their resistance in parallel is equivalent to 40Ω. A test on a four-line port for example, requires four resistors each of 160Ω
L with current compensation may include all 4 coils or only pairs to be effective.

Figure 4 – Example of coupling and decoupling network for unshielded symmetrical interconnection lines: lines-to-ground coupling

4.3 GR-1089 PoE Testing

4.3.1 Test Circuit for Test Set #10 in Table 1

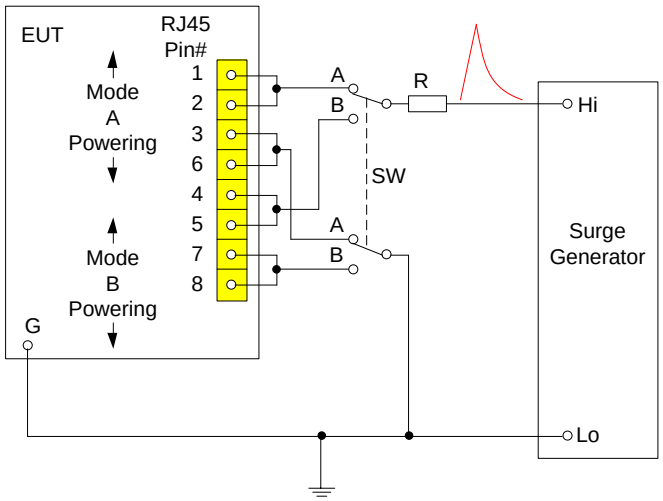


Figure 5 - Unshielded PoE ports- Metallic Test circuit.

Note: Testing is to be done on all PoE power feeding variants. For Power Sourcing Equipment (PSE) and Powered Device (PD) ports, test in both Switch (SW) positions A and B. For midspan power insertion equipment, test only in SW position B. Any unused conductors are left unconnected.

5 Surge Protection Circuit Design

5.1 Solution A (No RESET Allowed)

5.1.1 Application Circuit

The following circuit is intended to comply with the listed standards at Table 1 and not allow reset of the port under test nor adjacent ports.

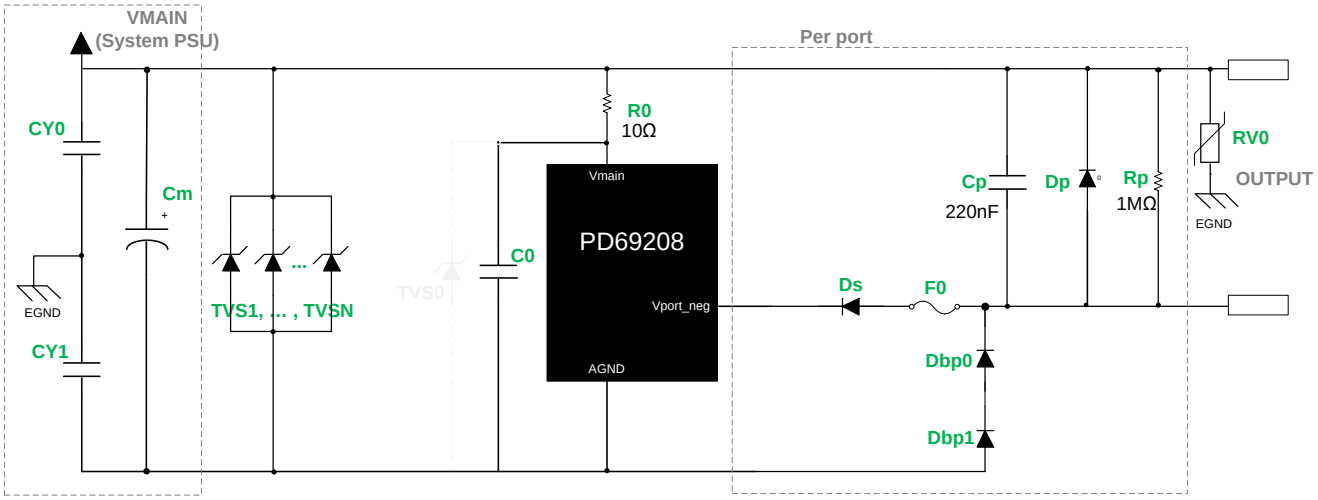


Figure 6 - Surge protection circuit for Solution A

Part ref.	Description	PCB Footprint	Ref. P/N[1]	QTY	
				Count	Per
Ds, Dp, Dbp0, Dbp1	Schottky Diode 1A, 100V	SMA	ST Microselectronics STPS1H100A	4	port
F0	Slow blow fuse 1.75A,0.2A^{2}s	1206	Bourns SF-1206SP175L-2-A9	1	port
RV0	Varistor 680VDC 10KA	T.H Disc 20mm	EPCOS B72220S2421K101	1	system
TVS1, …, TVSN	TVS 58V	SMC	Littelfuse 5.0SMDJ58A	See Table 3	system

Table 2 - Solution A Surge protection BOM

1 - Please see Section 7 for second source options.

5.1.2 TVS vs System Total Capacitance

The following Table shows the estimated number of TVS vs. total system capacitance and its equivalent ESR for the worst-case peak current expected on test 2 at Table 1. It is critical that the system designer validate the solution via system level test prior to mass production or field deployment.

	ESR [Ω]					
Cm [µF]	**0.010**	**0.025**	**0.05**	**0.1**	**0.2**	**0.5**
47	14	14	14	13	13	14
100	13	13	12	12	13	13
220	11	10	10	11	12	13
330	8	8	9	11	12	13
470	6	7	9	11	12	13
680	3	5	8	11	12	13
820	1	5	8	11	12	13
1000	1	4	8	11	12	13
1500	1	3	8	11	12	13
2000	1	3	7	10	12	13

Table 3 - Number of TVS vs. equivalent ESR and system capacitance Cm

5.1.3 Performance

The following drawings show the expected main current path for each type of surge event: DM (differential mode), CM (common mode), POS (positive polarity) and NEG (negative polarity).

5.1.3.1 Solution A with positive polarity differential surge

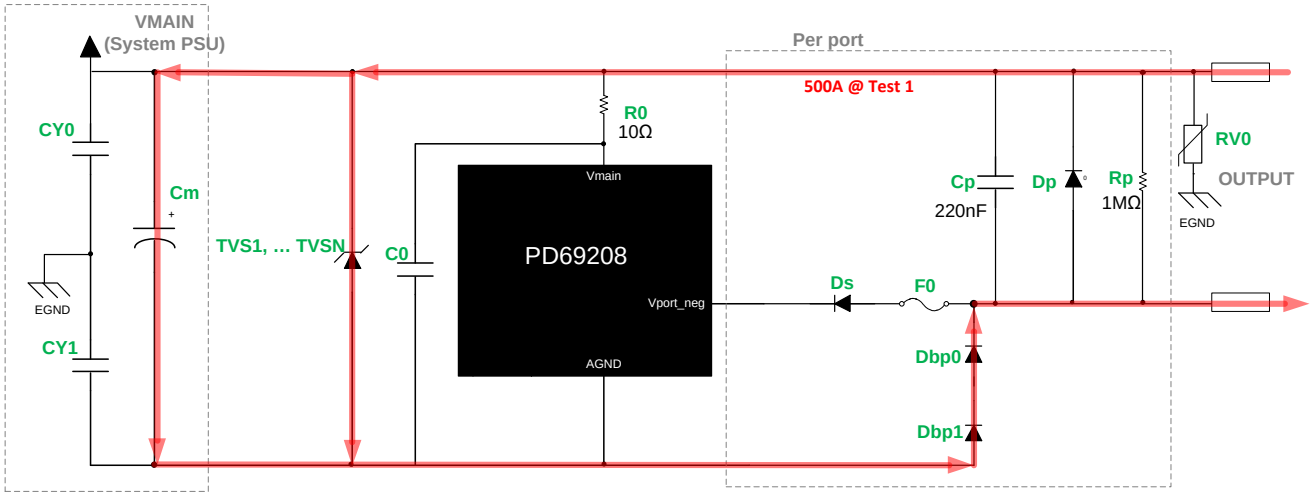


Figure 7 – main current path for solution A with positive polarity differential surge

Dbp1 is added as a backup to Dbp0, to prevent violation of UL single component failure requirement (i.e. if Dbp0 or Dbp1 fails, then the fuse F0 is not bypassed via the failed Schottky since a backup diode connected in serial with the failed part). The I^2t and size of the selected fuse F0 is relatively small since F0 isn't required to withstand the maximum surge current, which is blocked by Ds.

Rp - During detection, when no PD IC is connected the port, the output capacitor needs to be discharged between detection cycles. Usually this is done by the IC internal parallel resistance. But since Ds is blocking the discharge path an additional discharge resistor is required (Rp) and it should be of a value that doesn't affect PoE functionality.

The surge current goes from VMAIN to AGND through two parallel paths: VMAIN capacitors (Cm) and the TVS array TVS1-TVSN. By applying differential positive surge to the port, Cm is charged first to the clamping voltage of the TVS , then the TVS path become dominant. The higher the capacitance on VMAIN, the lower the expected current on the TVS array will be, since more energy is needed to charge higher capacitance to TVS clamp level (assuming low ESR).

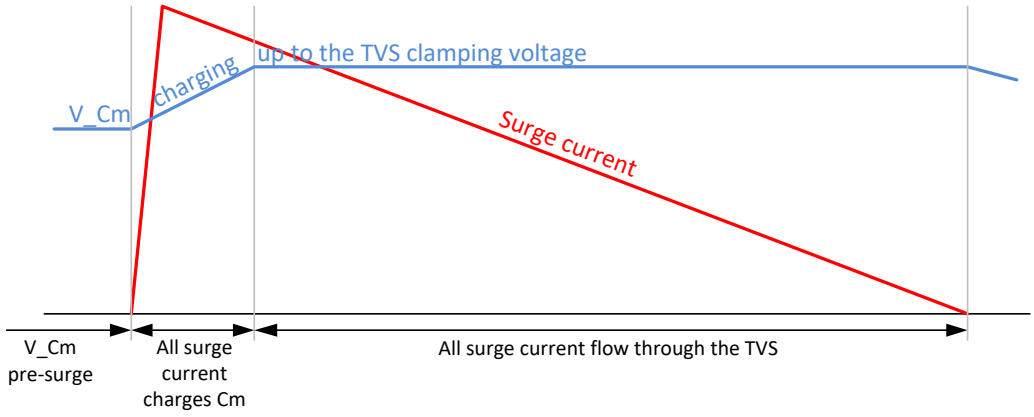


Figure 8 – surge current distribution on Cm and the TVS

The minimum recommended number of TVS units (per system) can be calculated as the TVS expected peak current divided by the TVS surge current rating, according to the TVS manufacturer. For example, if the expected current through the TVSs is 500A (assumes Cm ≤ 150µF), and TVS current rating is 53.5A (5.0SMDJ58A)

then the number of TVS parts should not be lower than 10 $[500A / 53.5A]$.

It is recommended to measure the actual TVS array peak current during the worst-case test in the final system, to evaluate the number of the TVS optimally. The worst-case current may be produced by common mode negative surge as described below, rather than the differential positive surge, due to lower equivalent resistance in the common mode setup.

Another example: if the system has significantly large total capacitance on Vmain (≥ 2mF) such that the voltage rise across the capacitor during the surge does not exceed the TVS clamping voltage or the power supply over voltage protection threshold (such as 85V latching threshold), then the TVS array on VMAIN becomes redundant, and it can be replaced by a single SMA TVS (such as SMAJ58A) in parallel with C0 (VMAIN pin capacitor).

5.1.3.2 Solution A with Negative polarity differential surge

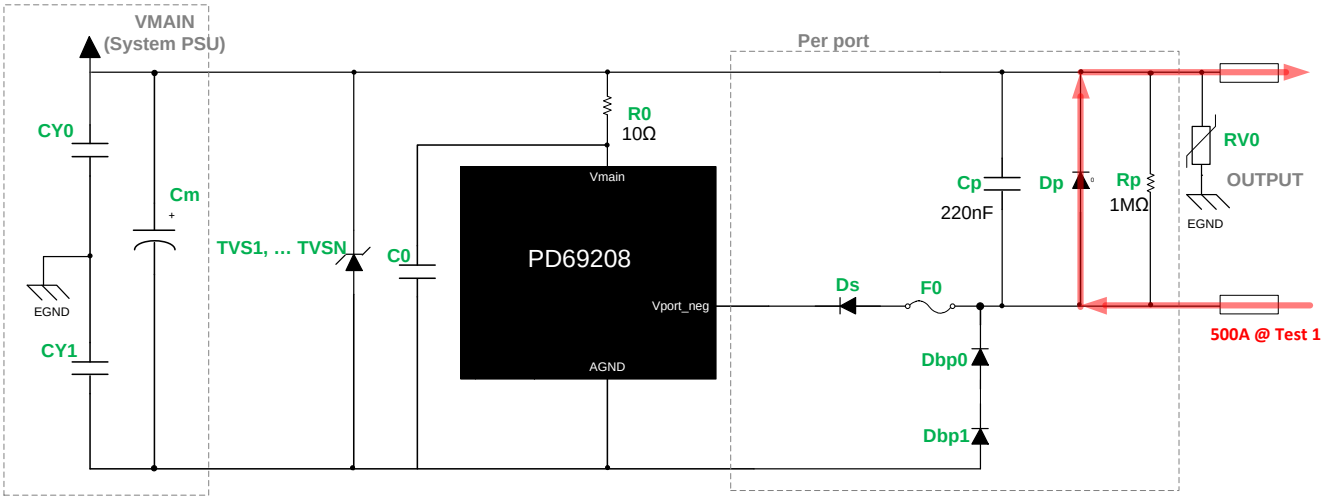


Figure 9 - main current path for solution A with Negative polarity differential surge

The surge returns to the generator through Dp.

5.1.3.3 Solution A with positive polarity common mode surge

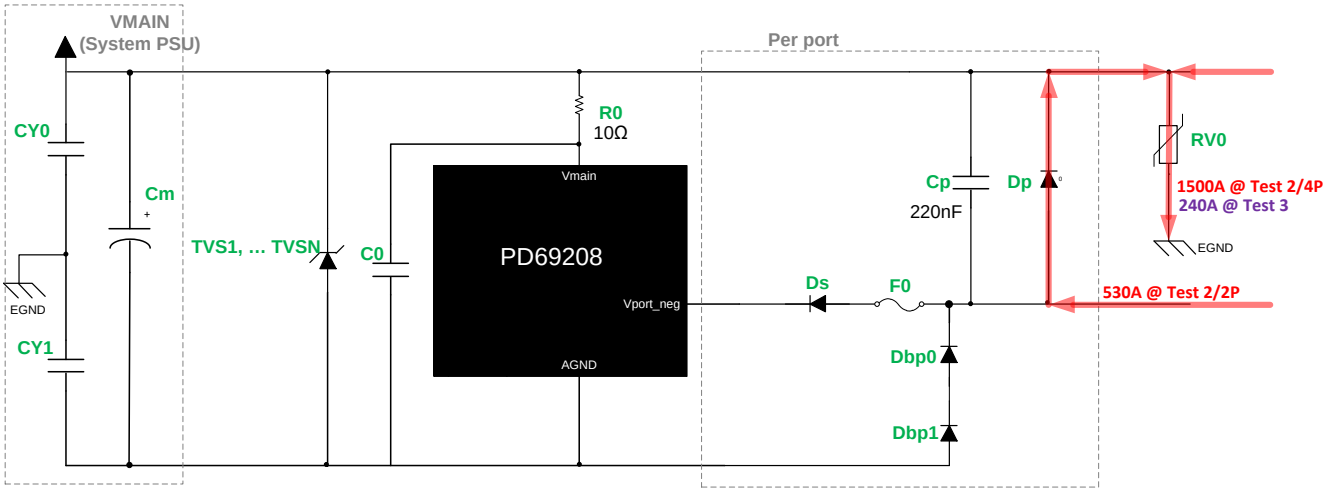


Figure 10 - main current path for solution A with positive polarity common mode surge

The positive common mode surge current returns to the common chassis through the varistor RV0. About half of the total surge current returns to the generator through Dp, similar to the negative differential surge test.

5.1.3.4 Solution A with negative polarity common mode surge

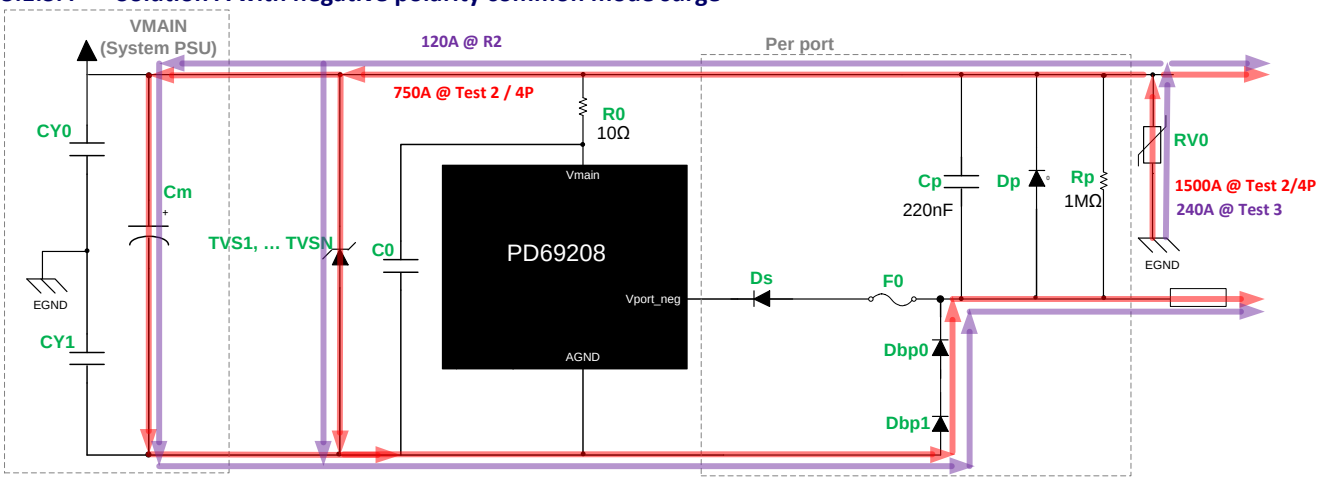


Figure 11 - main current path for solution A with negative polarity common mode surge

The negative common mode surge flows from the chassis through RV0. About half of the surge current, returns to the generator through Cm and the TVS array, similar to the positive differential surge, but current may be higher than the differential surge as the surge setup output impedance is lower.

Notes - Solution A:

[1] – Using a large Cm capacitance and low loads on the system ports may lead to a situation that the capacitance is charging during the surge to voltage level higher than the OVP threshold (58.5V) but have very slow discharging rate. This can lead to port shut down due to OVP. To avoid port shutdown by the chipset OVP a discharge circuitry can be considered. Please consult Microsemi for additional detail.

[2] - The system tested with CY0 = CY1 = 10nF / 2KV and Cm = 47µF x 3

[3] – Surge levels up to 1KV meets solution A pass criteria without external components

[4] – VMAIN clamped voltage by TVS1..N may get up to 80V under the surge current, meaning that the system power supply may be subjected to 80V. It is up to the designer to verify that the system PSU can handle this voltage from output components stress point of view and from over voltage protection.

5.2 Solution B (RESET Allowed)

5.2.1 Application Circuit

The following circuit is intended to comply with the listed standards.
If the port under surge was activated, it may reset and automatically recover. Any adjacent ports will not be effect by the surge. The system designers should validate to ensure acceptable performance prior to mass production or field deployment.

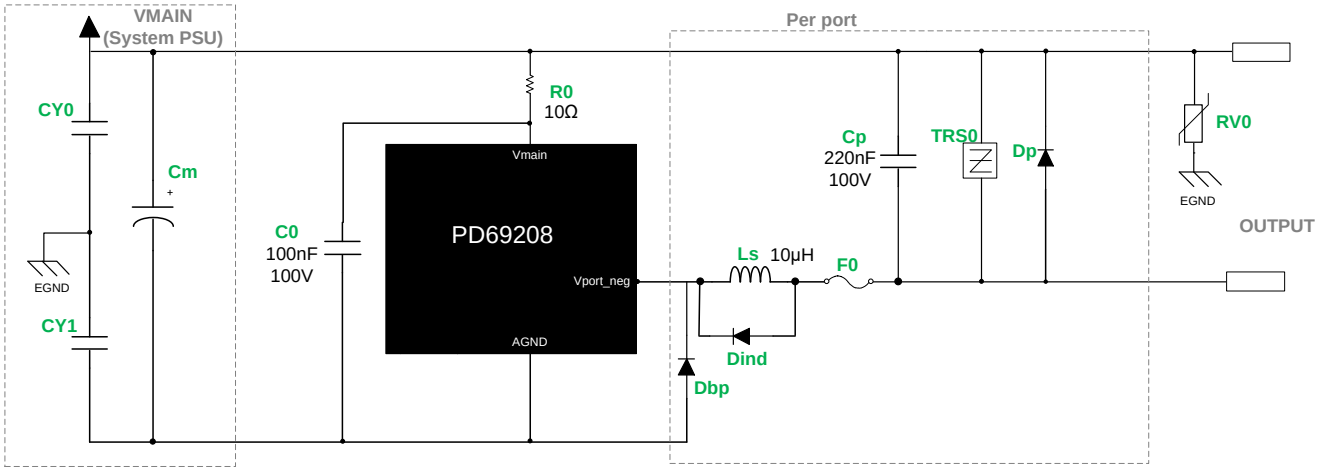


Figure 12 - Surge protection circuit for Solution B

Part ref.	Description	PCB Footprint / Size	Ref. P/N[1]	QTY	
				Count	Per
Dp, Dbp, Dind	Schottky Diode 1A, 100V	SMA	ST Microelectronics STPS1H100A	3	port
F0	Slow blow fuse 1.75A, 0.5A2s	1206	Bourns SF-1206SP175L-2-A9	1	port
RV0	Varistor 680VDC 10KA	T.H Disc 20mm	EPCOS B72220S2421K101	1	system
TRS0	Sidactor 58V	SMB	Littelfuse P0640SDLRP	1	port
Ls(2)	Inductor 10uH	Diameter 5.8mm / SMT	Bourns SDR0604-100ML	1	port

Table 4 - Solution B Surge protection BOM

1 - Please see Section 7 for second source options.

5.2.2 Performance

The following drawing show expected main current path for each type of surge event: DM (differential mode), CM (common mode), POS (positive polarity) and NEG (negative polarity).

5.2.2.1 Solution B with positive polarity differential mode surge

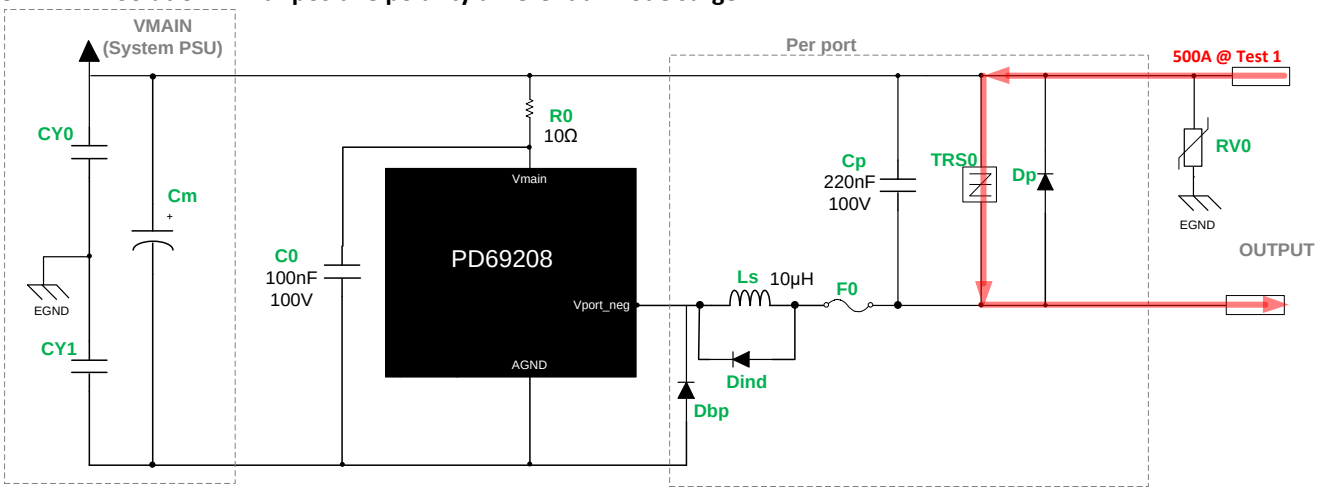


Figure 13 - main current path for solution B with positive polarity differential mode surge

The inductor Ls expedites the triggering of SIDACtor TRS0, by breaking the parallel connection between Cm and Cp (where Cm >> Cp). Once TRS0 is in a crowbar state, it becomes the return path of the surge and the port will shut down following the surge by PD69208 internal I_{LIM} protection, since the triggered TRS0 is reflected to the PD69208 port as a short-circuit condition. When the surge current is over and the port is shutdown the SIDACtor reset to its off-state, and the port is able to recover automatically.

D_{ind} clamps the induced voltage across Ls during normal operation. The low DCR inductor reduces normal operation power loss significantly respect to the serial diode at solution A.

Since the fuse F0 is not part of the dominant surge path (TRS0), the fuse not required to withstand the surge current and relatively low I^2t fuse can be used.

Dbp bypasses the PD69208 isolating MOSFET body-diode, to handle low-voltage surges where the induced voltage across Ls may not reach TRS0 breakdown voltage.

5.2.2.2 Solution B with negative polarity differential mode surge

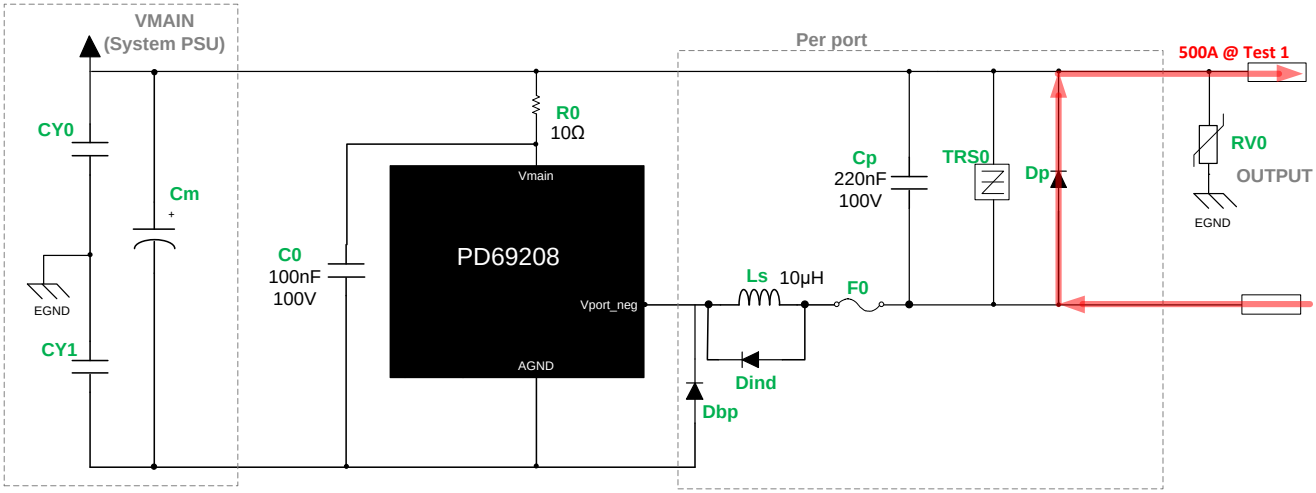


Figure 14 - main current path for solution B with negative polarity differential mode surge

The surge returns to the generator through Dp.

5.2.2.3 Solution B with positive polarity common mode surge

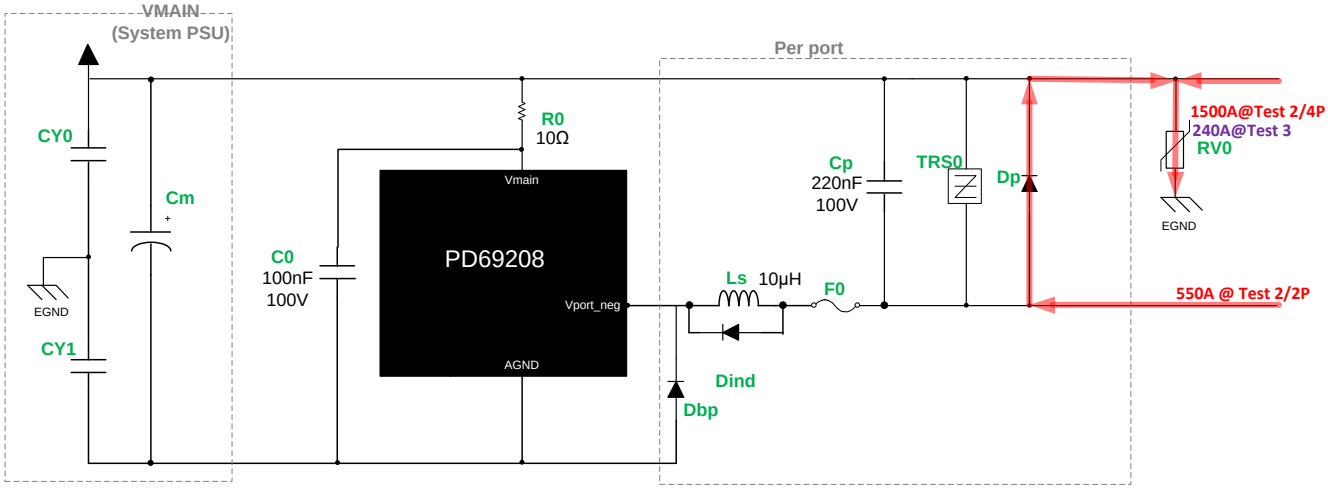


Figure 15 - main current path for solution B with positive polarity common mode surge

The positive common mode surge current returns to the common chassis through the varistor RV0. About half of the total surge current returns to the generator through Dp, similar to the negative differential surge test.

5.2.2.4 Solution B with positive negative common mode surge

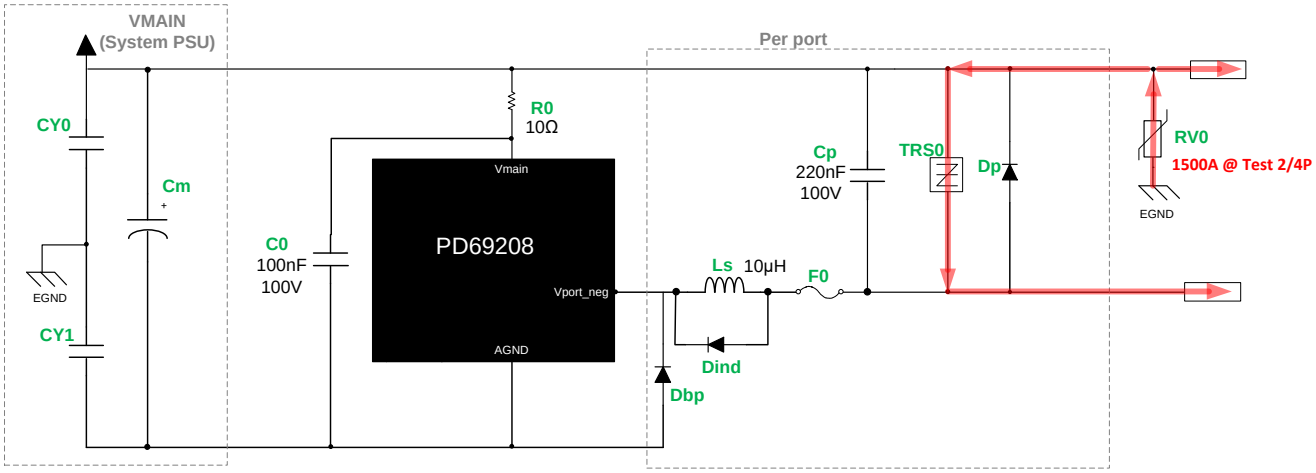


Figure 16 - main current path for solution B with positive negative common mode surge

The negative common mode surge is directed from the chassis through RV0. About half of the total surge current is returned to the generator through TRS0, in a similar way to positive differential surge, but may be higher than the differential surge case.

Notes – solution B:

[1] The system tested with CY0 = CY1 = 10nF / 2KV and Cm = 47µF x 3 (1 per IC). The solution verified for Cm up to 2500µF.

6 IEC62368-1 ED3

6.1 Fuses per Port

Fuses per port are not needed in circuits with a total power level of up to 3 kW. This is because PD69208 is a UL 2367 (category QVRQ2) recognized component and fulfills Limited Power Source (LPS) requirements of the latest editions of IEC60950-1 and EN60950-1. However, IEC62368-1 ED 3 (released in October 2018 and becomes effective December 2020) requires per port fuses for a system power supply greater than 250 W.

According to the latest release of the hazard-based safety standard **UL/EN/IEC 62368-*1*** *ED3 "Audio/video, information and communication technology equipment – Part 1: Safety requirements"* the compliance with Limited Power Source (LPS) requirements is achieved by using an IC current limiter PD69208/4 that limits the output current in accordance with limits specified in the Table .

Microsemi recommends use of the Bourns SF-1206SP175L-2-A9 fuse.

Output voltage Uoc		Output current Isc	Apparent power S
Vac	**Vdc**	**A**	**VA**
Uoc ≤ 30	Uoc ≤ 30	≤ 8.0	≤ 100
-	30 < Uoc ≤ 60	≤150/Uoc	≤100

Table 5 - Limits for inherently limited power sources.

7 BOM considerations

The system designers may replace any protection component by other equivalent component based on cost or evaluability. The following table show few options for the main protection components. Option 1 is the Microsemi recommended option. Options 2 and 3 are provided as a courtesy to customers, please consult Microsemi prior to use of Option 2 or 3.

Critical: It is up to the system designer to ensure acceptable performance with any protection component or solution prior to mass production or field deployment.

Solution	Component	Description	Option 1	Option 2	Option 3
A	Ds, Dp, Dbp0, Dbp1	Schottky Diode 1A, 100V	ST Microelectronics STPS1H100A	ON Semiconductor MBRA1H100T3G	
	F0	Slow blow fuse 1.75A,0.2A^{2}s	Bourns SF-1206SP175L-2-A9		
	RV0	Varistor 680VDC 10KA	EPCOS B72220S2421K101	Littelfuse V20E420P	Brightking 681KD20J
	TVS1, …, TVSN	TVS 58V	Littelfuse 5.0SMDJ58A	Bourns 5.0SMDJ58A	Brightking 5.0SMDJ58A
B	Dp, Dbp, Dind	Schottky Diode 1A, 100V	ST Microelectronics STPS1H100A	ON Semiconductor MBRA1H100T3G	
	F0	Slow blow fuse 1.75A, 0.5A^{2}s	Bourns SF-1206SP175L-2-A9		
	RV0	Varistor 680VDC 10KA	EPCOS B72220S2421K101	Littelfuse V20E420P	Brightking 681KD20J
	TRS0	Sidactor 58V	Littelfuse P0640SDLRP	Bourns TISP4070J3BJR	
	Ls$^{(2)}$	Inductor 10uH	Bourns SDR0604-100ML		

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