Microsemi IGLOO2 FPGA Evaluation Kit Test Report

CONTENTS

1 SCOPE

This document provides information relevant to performance tests executed on the Microsemi IGLOO2 FPGA Evaluation kit in conjunction with the Ultra Communications X80-Q Fury Transceiver.

2 RELATED DOCUMENTS

170-0018	X80-Q Fury Transceiver Data Sheet
51700121-0/6.13	IGLOO2 FPGA Datasheet

3 OVERVIEW

The IGLOO2 FPGA Chip (Figure 1) has been embedded with high-speed SERDES functionality at data rates up to 5 Gbps. Tests involving eye measurements and bit error rate (BER) sensitivity were carried out in an effort to demonstrate the effectiveness of the Microsemi device in conjunction with the Ultra Communications X80-Q Fury Transceiver (Figure 2).

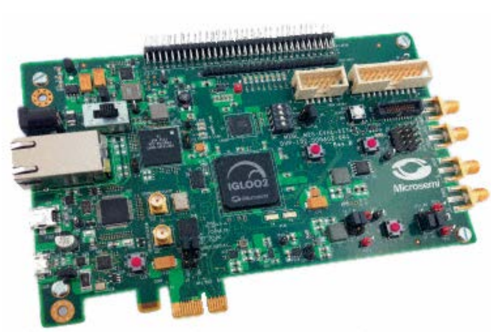


Figure 1: IGLOO2 FPGA Chip with Evaluation Board

Figure 2: X80-Q Fury Transceiver

4 TEST SETUP

Eye diagram acquisitions and loopback tests were executed to observe the signal integrity of the IGLOO2 FPGA device at 5 Gbps. The BER sensitivity setup involving the Microsemi IGLOO2 FPGA and Ultra Communications X80-Q Fury Transceiver evaluation boards along with an optical attenuator can be seen in figure 3. An error counter found in the Microsemi GUI was used for BER calculation. Eye diagrams were attained by connecting the positive lane of the transmission signal to an Agilent DCA Infiniium Oscilloscope, either with or without the inclusion of the X80-Q Transceiver evaluation board.

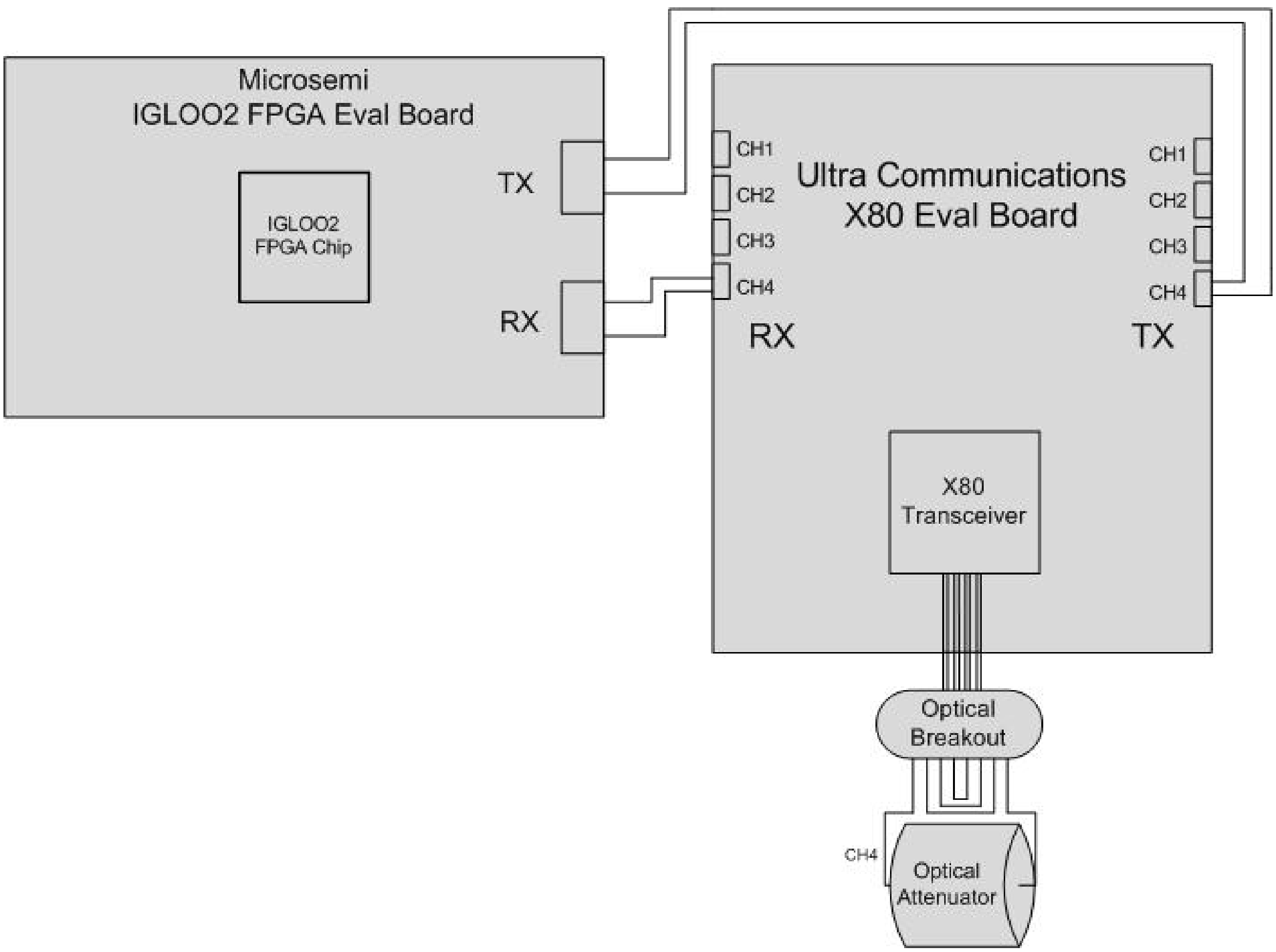


Figure 3: Test Setup Diagram

The Fury transceiver evaluation board was configured with the following settings:

Channel 4 TX Parameters	**Value**	**RX Parameters**	**Value**
TX_IT: Top Current at '1' Level	11.0 mA	RX_RL: Load Resistance	0 d
TX_IM: Modulation Current	10.0 mA	RX_CML, be <2.0>: Pre-Emphasis	3 d
TX_IP: Pre-emphasis	3.0 mA	RX_CML, bo 3.0>: Output Amplitude	13 d
TX_ID: Duty Cycle	0 d	IREF_AGC: photocurrent when AGC engaged	300 µA
Avg. Current, I_{AVG}:	6.0 mA	IREF_VE: Reference Current	398.4 µA

5 TEST RESULTS

5.1 Eye Diagram Tests

All eye diagrams recorded were in the pattern PRBS7, which could be set by the Microsemi GUI. Measurements were taken from the positive terminal, while a termination was connected to the negative terminal. A constant value of 250 waveforms were collected for each measurement. The first acquisition, shown in Figure 4, depicts an eye resulting from a direct connection from lane 2 of the IGLOO2 evaluation board to an oscilloscope.

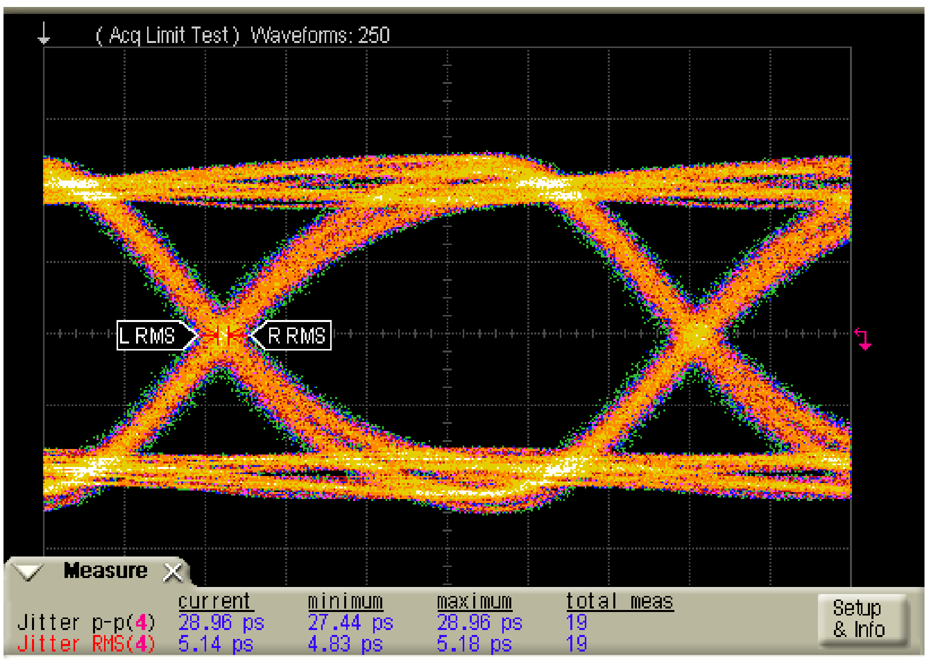


Figure 4: Eye Acquisition 1, Microsemi board to oscilloscope

This acquisition shows an RMS Jitter Value of 5.14 ps, and a Peak to Peak jitter value of 28.96 ps. Another acquisition of the same signal, shown in Figure 5, shows a standard fiber channel mask in place, formatted according to the crossing points and hi/low levels of the eye.

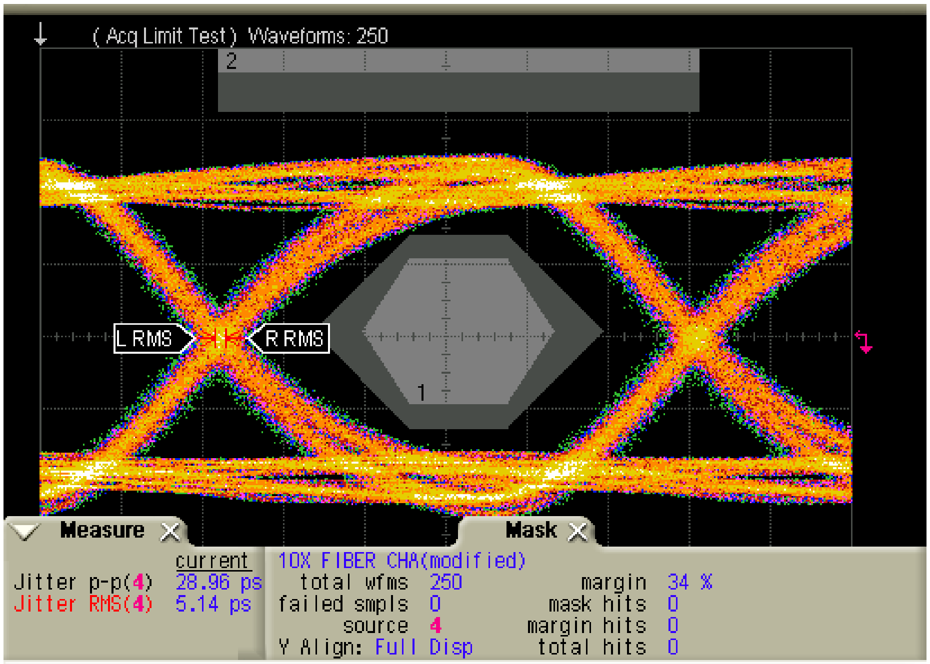


Figure 5: Eye Acquisition 1 with standard fiber mask

This standard fiber channel mask depicts a margin of 34% with zero failing points, suggesting acceptable signal integrity. This value designates how much larger the customized eye mask could be before touching the data points along the waveform. A mask margin indicates the amount of stress the signal can handle before compromising signal integrity by breaching the eye mask, an industry-standard indicator of signal quality.

Figure 6 depicts the optical fiber along the breakout cable routed to the oscilloscope.

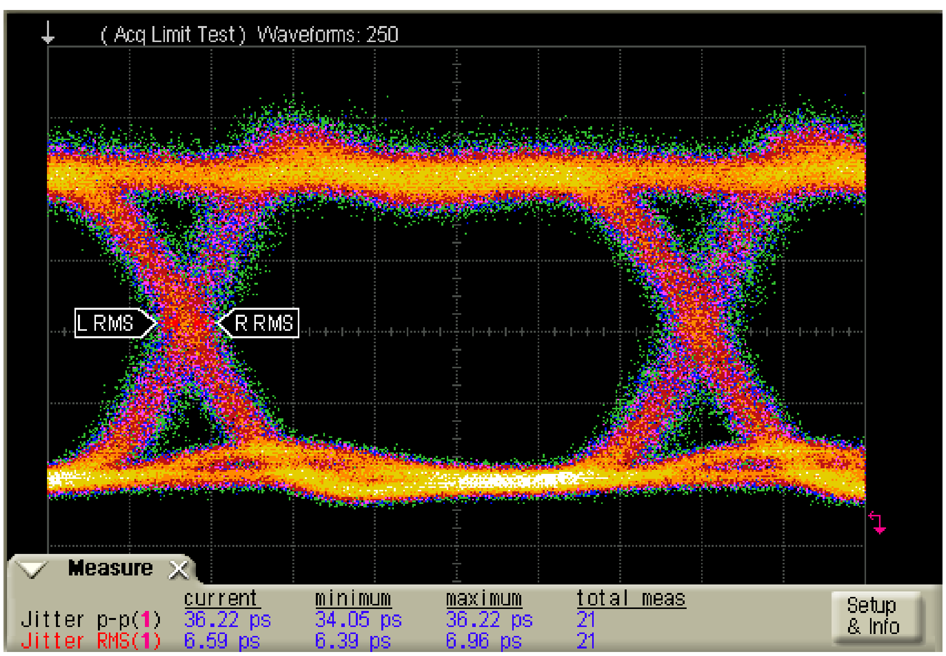


Figure 6: Eye Acquisition 2, signal from optical fiber breakout cable

The optical eye acquisition, taken from the optical breakout cable connected to the X80-Q transceiver indicates peak-to-peak and RMS jitter values of 36.22 ps and 6.59 ps respectively. This laser signal yielded a TX power level of -2.54 dBm and an extinction ratio of 9.54 dB.

The third eye acquisition, shown in Figure 6, was taken from the hardware setup shown in Figure 3, minus the attenuating device. The RX output from the Fury Transceiver evaluation board was routed to the oscilloscope as opposed to being looped back to the IGLOO2 device.

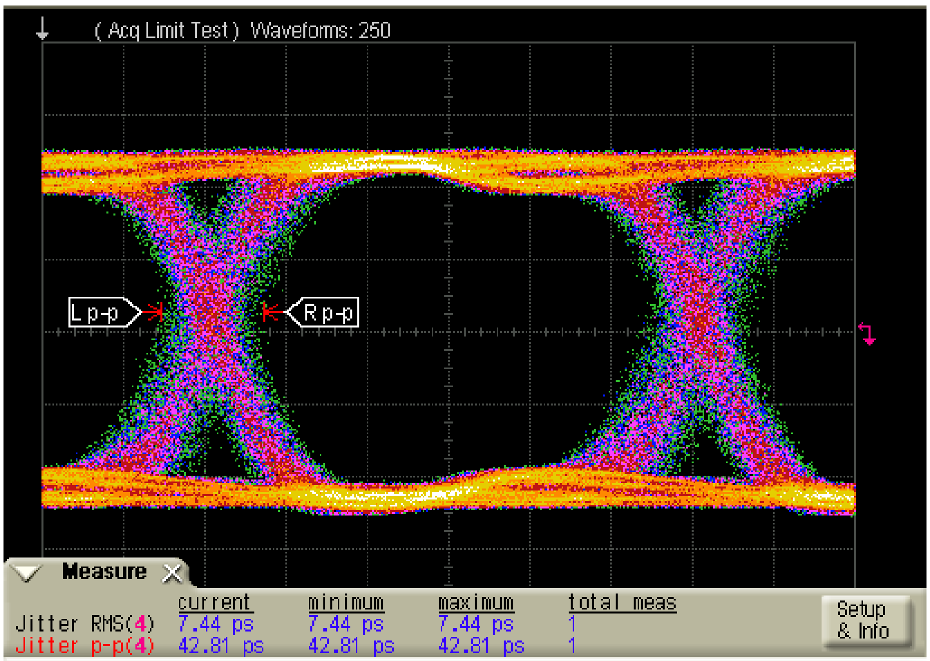


Figure 7: Eye Acquisition 3, oscilloscope signal from Microsemi board, X80-Q Transceiver and optical breakout cable

An increase in the Peak-to-Peak and RMS Jitter values to 42.81 ps and 7.44 ps respectively was observed. It shows that jitter by the optical breakout cable and copper cables was contributed to the system.

The eye acquisition shown in Figure 7 is the same as the previous acquisition with the same standard mask originally applied in Figure 5.

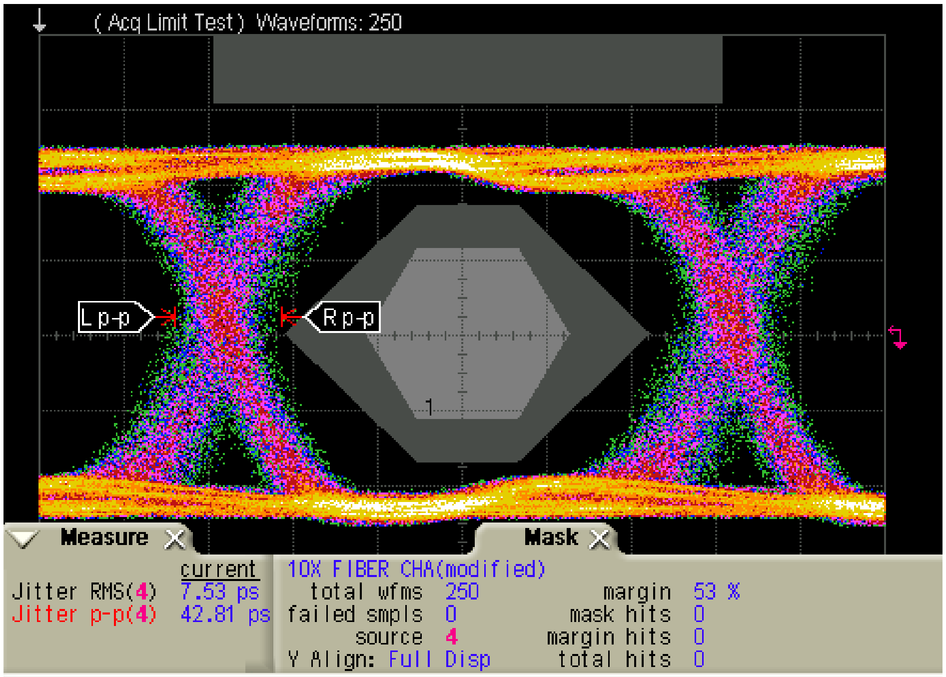


Figure 8: Eye Acquisition 3 with standard fiber mask

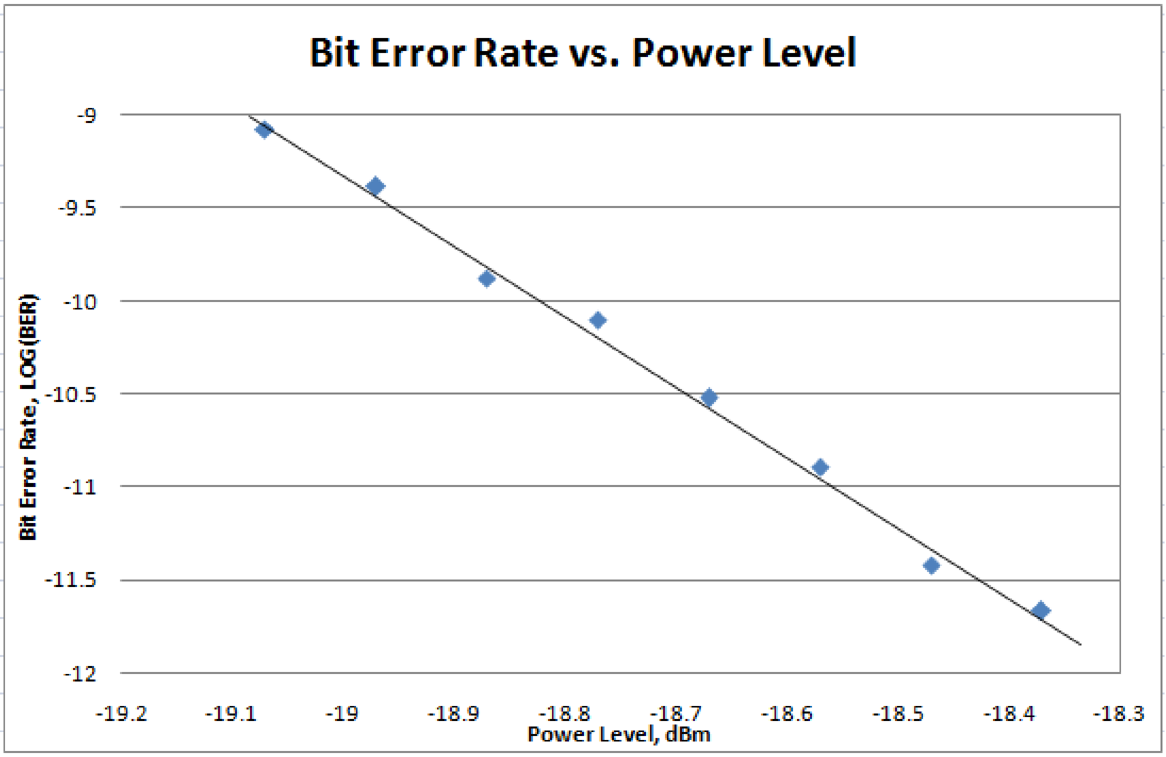
This eye acquisition demonstrated a greater mask margin than that of fig. 5 with zero failing points. A 53% margin is due to the very healthy output driver found in the Fury transceiver system along with the option to set a pre-emphasis magnitude on the X80-Q Transceiver GUI, indicated in the table on page 3.

5.2 Loopback Tests

The graphical user interface provided with the Microsemi evaluation kit has the capability to count errors when the transmission signal is in loopback mode. The tests that were carried out in this section had to do with the sensitivity of the Bit Error Rate of the signal as it was given increasing magnitudes of attenuation along the optical breakout cable (figure 3). The provided industry-standard BER for the IGLOO2 FPGA device, 10e-12, is subject to change as the attenuation level crosses a certain threshold.

Loopback Attenuation Results:

Average Power Level (dBm)	Real Bit Error Rate
-18.37	2.14E-12
-18.47	3.78E-12
-18.57	1.28E-11
-18.67	3.00E-11
-18.77	8.00E-11
-18.87	1.33E-10
-18.97	4.13E-10
-19.07	8.43E-10



This data suggests that the IGLOO2 device is capable of maintaining acceptable signal integrity for a substantial amount of noise from attenuation and detecting a rising number of errors for an increasing attenuation level. An extinction ratio of 9.54 dB and an average power level of -2.54 dBm along the optical line with no external attenuation indicates a usable link margin of around 17 dB for BER tests with the IGLOO2 FGPA device.

6 FINAL REMARKS

In the signal processing industry, reliable FPGA devices play an important role in establishing high speed serial links. High-reliability FPGAs and optical transceivers complement the growing need for high speed serial links for avionic and space applications. Performance tests indicate that Microsemi's offering of a low cost, high speed SERDES device in the form of the IGLOO2 FPGA Evaluation Kit along with Ultra Communication's durable X80-Q transceiver module demonstrate industry-standard signal integrity at speeds of up to 5Gbps per lane.

More information on the IGLOO2 FPGA device can be found at this address:

http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga