Rad-Tolerant Current Mode PWM Controller

Description

The SGR1846 is fit, form and function compatible to the SG1846 with the addition of guaranteed performance after radiation exposure to Total Ionizing Dose (TID), Enhanced Low Dose Rate Sensitivity (ELDRS), and Single Event Latch-up (SEL) conditions. The SGR1846 control IC provides the required features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The advanced performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include, inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double-pulse suppression, dead-time adjust capability, and a ±1% trimmed bandgap reference.

Features

- Automatic Feed-forward Compensation
- Programmable Pulse by pulse Current Limiting
- Automatic Symmetry Correction in Push-pull Configuration
- Enhanced Load Response Characteristics
- Parallel Operation Capability for Modular Power Systems
- Differential Current Sense Amplifier with Wide Common-mode Range
- Double Pulse Suppression
- 200 mA Totem-pole Outputs
- ± 1% Bandgap Reference
- Under-Voltage Lockout
- Soft-start and Shutdown Capability
- 500kHz Operation

High Reliability Features - SGR1846

- Rad-tolerance: (Test data available)
- TID to a Minimum of 100krad(Si)
- ELDRS to a Minimum of 50krad(Si)
- SEL Immunity to 87MeV-cm^2/mg

Block Diagram

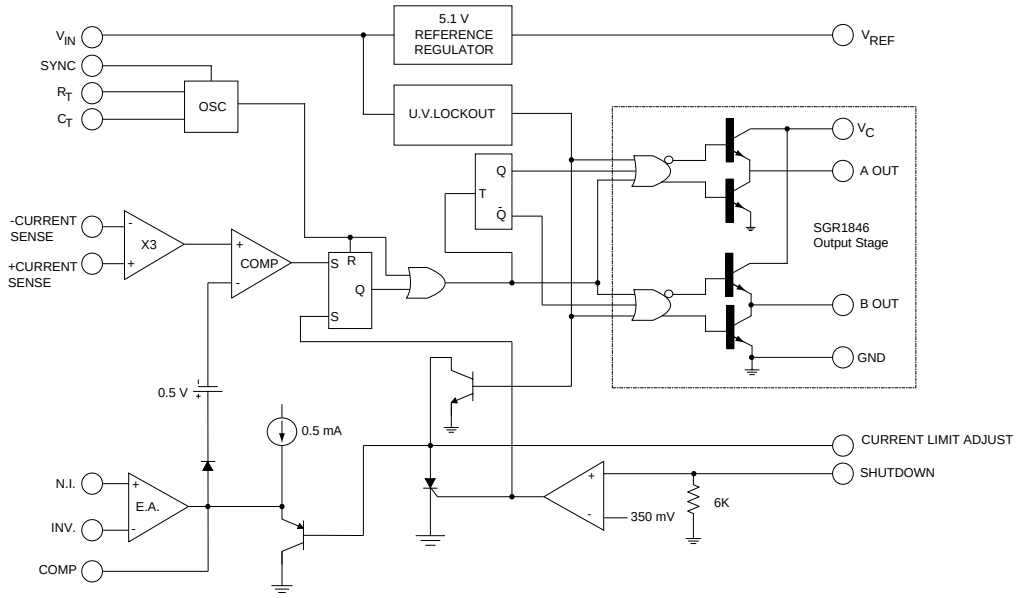
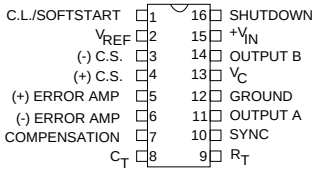
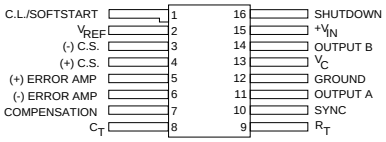
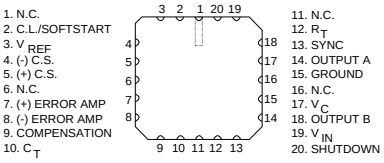


Figure 1 · Block Diagram

Connection Diagrams and Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type	Connection Diagram
-55°C to 125°C	J	16-PIN CERAMIC DIP PACKAGE	SGR1846J-EV*	Hermetic	
			SGR1846J		
	F	16-PIN CERAMIC FLAT PACK[2]	SGR1846F-EV*		
			SGR1846F		
	L	20-PIN CERAMIC LEADLESS CHIP CARRIER[2]	SGR1846L-EV*		
			SGR1846L		

* EV is Microsemi's "Equivalent V" flow that follows MIL-PRF-38535 requirements for Class V processing.

Absolute Maximum Ratings

Parameter	Value	Units
Supply Voltage ($+V_{IN}$)	40	V
Collector Supply Voltage(V_C)	40	V
Analog Inputs (Pins 3, 4, 5, 6, and 16)	-0.3V to $+V_{IN}$	V
Logic Input	-0.3V to 5.5V	V
Source/Sink Load current (continuous)	200	mA
Source/Sink Load Current (peak, 200 ns)	500	mA
Reference Load Current	30	mA
Soft Start Sink Current	50	mA
Sync Output Current	5	mA
Error Amplifier Output Current	5	mA
Oscillator Charging current (Pin 9)	5	mA
Operating Junction Temperature Hermetic (J, L, F Packages)	150	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10 Seconds)	300	°C
RoHS Peak Package Solder Reflow Temp. (40 sec. max. exp.)	260 (+0, -5)	◦C

Notes:
1. *Values beyond which damage may occur.*
2. *Consult factory for product availability.*

Thermal Data

Parameter	Value	Units
J Package:		
Thermal Resistance-Junction to Case, θ_{JC}	30	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	80	°C/W
F Package:		
Thermal Resistance-Junction to Case, θ_{JC}	70	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	115	°C/W
L Package:		
Thermal Resistance-Junction to Case, θ_{JC}	35	°C/W
Thermal Resistance-Junction to Ambient, θ_{JA}	120	°C/W

Notes:
1. *Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.*
2. *The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/PCBoard system. All of the above assume no ambient airflow.*

Recommended Operating Conditions

Parameter	Value	Units
Supply Voltage Range	8 to 40	V
Collector Supply Voltage Range	4.5 to 40	V
Source/Sink Output Current (continuous)	100	mA
Source/Sink Output Current (peak 200ns)	200	mA
Reference Load Current	0 to 10	mA
Oscillator Frequency Range	1 to 500	kHz
Oscillator Timing Resistor (R_T)	2 to 100	kΩ
Oscillator Timing Capacitor (C_T)	1 to 100	nF
Operating Ambient Temperature Range		
SGR1846	-55 to 125	°C

Note: *Range over which the device is functional.*

Electrical Characteristics

Unless otherwise specified, these specifications apply over the operating ambient temperatures for SGR1846 with -55°C ≤ T_A ≤ 125°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Symbol	Parameter	Test Condition	SGR1846			Units
			Min	Typ	Max	
Reference Section						
V_{REF}	Output Voltage	T_J = 25°C, I_O = 1mA	5.05	5.10	5.15	V
V_{REG}	Line Regulation	V_{IN} = 8V to 40V		5	20	mV
I_{REG}	Load Regulation	I_L = 1mA to 10mA		3	15	mV
	Temperature Stability[1]			0.4		mV/°C
	Total Output Variation[1]	Line, Load and Temperature	5.00		5.20	V
	Output Noise Voltage[1]	10Hz ≤ f ≤ 10kHz. T_J = 25°C		100		µV
	Long Term Stability[1]	T_J = 125°C, 1000Hrs.		5		mV
$VREF_{ISC}$	Short Circuit Output Current	V_{REF} = 0V	-10	-45		mA
Oscillator Section[6]						
OSC	Initial Accuracy	T_J = 25°C	39	43	47	kHz
OSC_{VS}	Voltage Stability	V_{IN} = 8V to 40V		1	2	%
OSC_{TS}	Temperature Stability[1]	Over Operating Range		1		%
VOH	Sync Output High Level		3.9	4.35		V
VOL	Sync Output Low Level			2.3	2.5	V
VIH	Sync Input High Level	Pin 8 = 0V	3.9			V
VIL	Sync Input Low Level	Pin 8 = 0V			2.5	V
IIL	Sync Input Current	Sync Voltage = 5.25V, Pin 8 = 0V		1.2	1.5	mA
Error AMP Section						
EA_{VOS}	Input Offset Voltage			0.5	5	mV
EA_{IIB}	Input Bias Current		-1	-0.6		µA
EA_{IOS}	Input Offset Current			40	250	nA
EA_{CM}	Common Mode Range	V_{IN} = 8V to 40V	0		V_{IN}-2V	V
EA_{AV}	Open Loop Voltage Gain	V_O = 1.2V to 3V, V_{CM} = 2V	80	105		dB
EA_{UGB}	Unity Gain Bandwidth[1]	T_J = 25°C	0.7	1.0		MHz
EA_{CMRR}	CMRR	V_{CM} = 0V to 38V, V_{IN} = 40V	75	100		dB
EA_{PSRR}	PSRR	V_{IN} = 8V to 40V	80	105		dB
EA_{SNK}	Output Sink Current	V_{ID} = - 15mV to -5V, $V_{PIN\ 7}$ = 1.2V	2	6		mA
EA_{SRC}	Output Source Current	V_{ID} = 15mV to 5V, $V_{PIN\ 7}$ = 2.5V		-0.5	-0.4	mA
EA_{VOH}	High Level Output Voltage	R_L = 15kΩ (Pin 7)	4.3	4.6		V
EA_{VOL}	Low Level Output Voltage	R_L = 15kΩ (Pin 7)		0.7	1	V

Symbol	Parameter	Test Condition	SGR1846			Units
			Min	Typ	Max	
Current Sense Amplifier Section						
CS_{AV}	Amplifier Gain[2 &3]	$V_{PIN\ 3}$ = 0V, Pin 1 Open	2.5	2.75	3.0	V
	Maximum Differential[3]	Pin 1 Open R_L = 15kΩ (Pin 7)				
	Input Signal[2] ($V_{PIN\ 4}$ - $V_{PIN\ 3}$)		1.1	1.2		V
	Input Offset Voltage[2]	$V_{PIN\ 1}$ = 0.5V, Pin 7 Open		5	25	mV
CS_{CMRR}	CMRR	V_{CM} = 1V to 12V	60	83		dB
CS_{PSRR}	PSRR	V_{IN} = 8V to 40V	60	84		dB
CS_{IIB}	Input Bias Current[2]	$V_{PIN\ 1}$ = 0.5V, Pin 7 Open	-10	-2.5		µA
CSI_{OC}	Input Offset Current[2]	$V_{PIN\ 1}$ = 0.5V, Pin 7 Open		0.08	1	µA
CS_{CM}	Input Common Mode Range		0		V_{IN} -3	V
	Delay to Outputs[1]	T_J = 25°C		200	500	ns
Current Limit Adjust Section						
	Current Limit Offset Voltage[2]	$V_{PIN\ 3}$ = 0, $V_{PIN\ 4}$ = 0V, Pin 7 Open	0.45	0.5	0.55	V
CL_{IIB}	Input Bias Current	$V_{PIN\ 5}$ = V_{REF}, $V_{PIN\ 6}$ = 0V	-30	-10		µA
Shutdown Terminal Section						
SD	Threshold Voltage		250	350	400	mV
	Input Voltage Range		0		V_{IN}	V
SD_{LC}	Minimum Latching Current					
	($I_{PIN\ 1}$)[4]		3.0	1.5		mA
	Maximum Non-Latching Current					
	($I_{PIN\ 1}$)[5]			1.5	0.8	mA
SD_{DELAY}	Delay to Outputs[1]	T_J = 25°C		300	600	ns
Output Section						
	Collector Emitter Voltage		40			V
	Collector Leakage Current	V_C = 40V			200	µA
	Output Low Level	I_{SINK} = 20mA		0.1	0.4	V
		I_{SINK} = 100mA		0.4	2.1	V
	Output High Level	I_{SOURCE} = 20mA	13	13.5		V
		I_{SOURCE} = 100mA	12	13.5		V
	Rise Time[1]	C_L = 1nF, T_J = 25°C		50	300	ns
	Fall Time[1]	C_L = 1nF, T_J = 25°C		50	300	ns
Under-Voltage Lockout Section						
	Start-Up Threshold			7.7	8.0	V
	Threshold Hysteresis			0.75		V
Total Standby Current						
IQ	Supply Current			17	21	mA

Notes:

1. *These parameters, although guaranteed over the recommended operating conditions, are not tested in the production.*
2. *Parameter measured at trip point of latch with $V_{PIN\ 5} = V_{REF}$, $V_{PIN\ 6} = 0V$.*
3. *Amplifier gain defined as : $G = \frac{\Delta V_{PIN7}}{\Delta V_{PIN4}}$; $V_{PIN\ 4}$ = 0V to 1.0V*
4. *Current into Pin 1 guaranteed to latch circuit in shutdown state.*
5. *Current into Pin 1 guaranteed not to latch circuit in shutdown state.*
6. *R_T = 10kΩ, C_T = 4.7nF*

Characteristic Curves

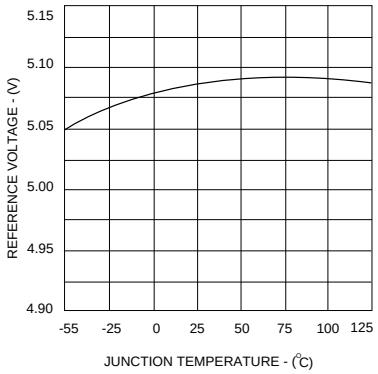


Figure 2 · Reference Voltage Vs. Temperature

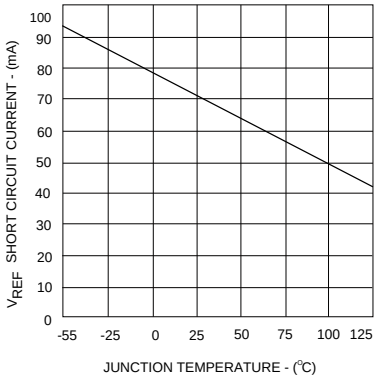


Figure 3 · V_{REF} Short Circuit Current Vs. Temperature

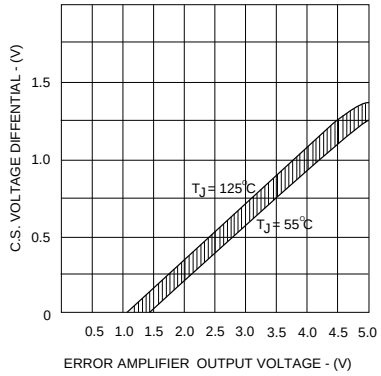


Figure 4 · Current Sense Threshold Vs. Error Amplifier Output

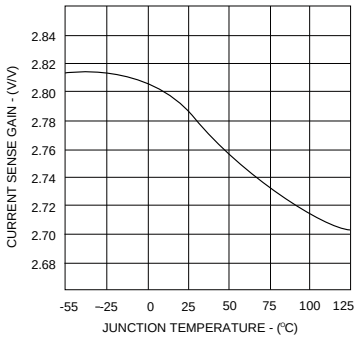


Figure 5 · Current Sense Gain Vs. Temperature

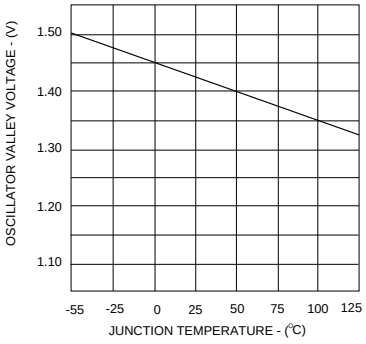


Figure 6 · Oscillator Valley Voltage Vs. Temperature

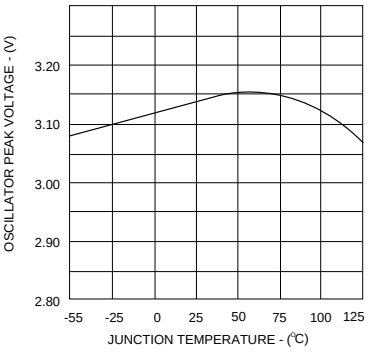


Figure 7 · Oscillator Peak Voltage Vs. Temperature

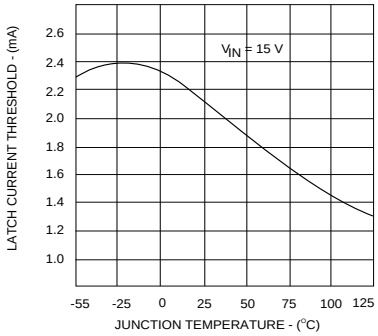


Figure 8 · Minimum SCR Latch Current

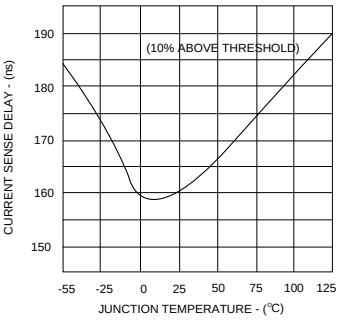


Figure 9 · Current Sense Delay Vs. Temperature

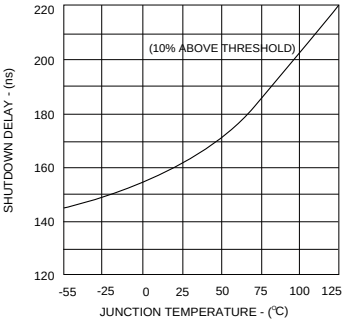


Figure 10 · Shutdown Delay To Output Vs. Temperature

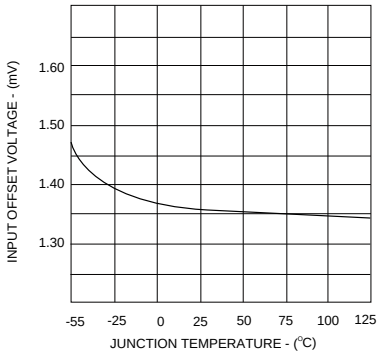


Figure 11 · Error Amplifier Input Offset Voltage Vs. Temperature

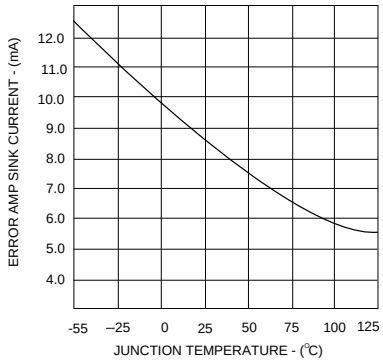


Figure 12 · Error AMP Sink Current Vs. Temperature

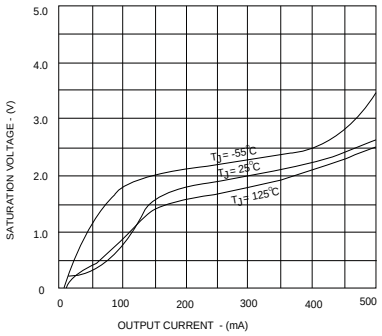


Figure 13 · Output Transistor Saturation Voltage Vs. Output Current (Skin Transistor)

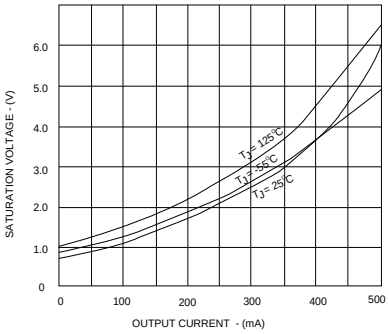


Figure 14 · Output Transistor Saturation Voltage Vs. Output Current (Source Transistor)

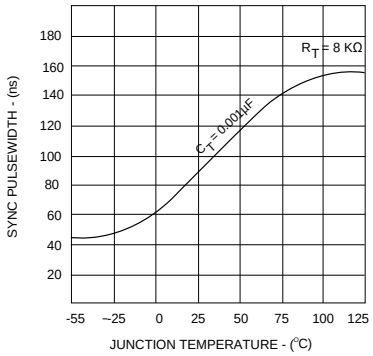


Figure 15 · Sync Pulsewidth Vs. Temperature

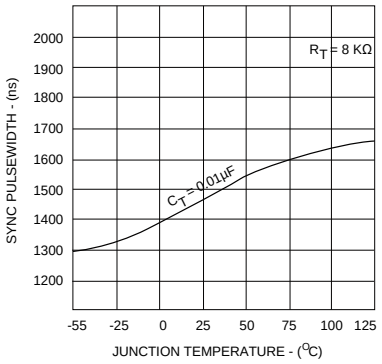


Figure 16 · Sync Pulsewidth Vs. Temperature

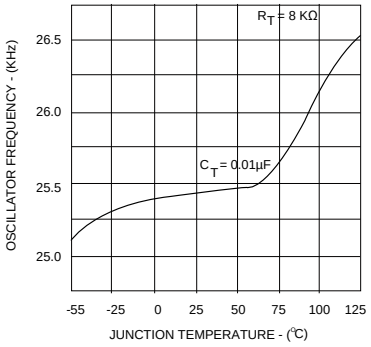


Figure 17 · Oscillator Frequency Vs. Temperature

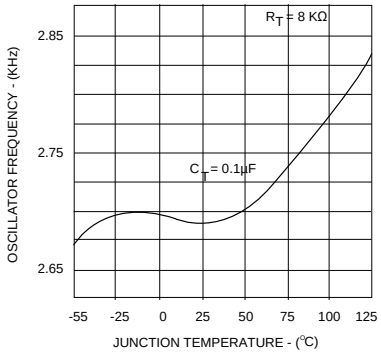


Figure 18 · Oscillator Frequency Vs. Temperature

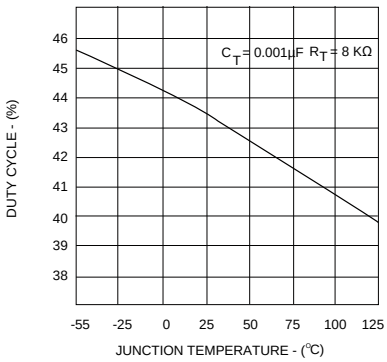


Figure 19 · Duty Cycle Vs. Temperature

Application Information

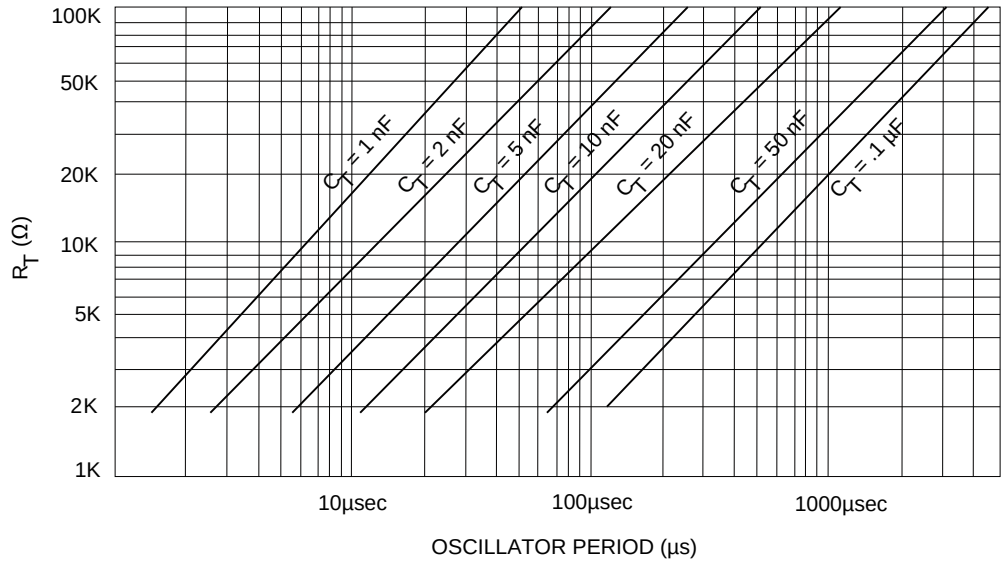


Figure 20 · Oscillator Frequency Curves

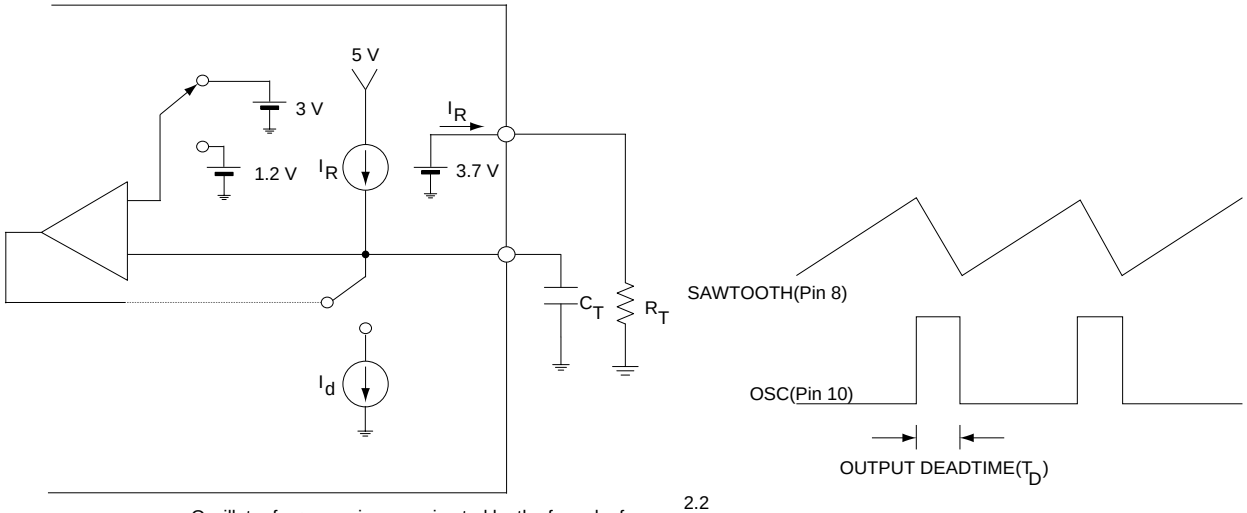


Figure 21 · Oscillator Circuit

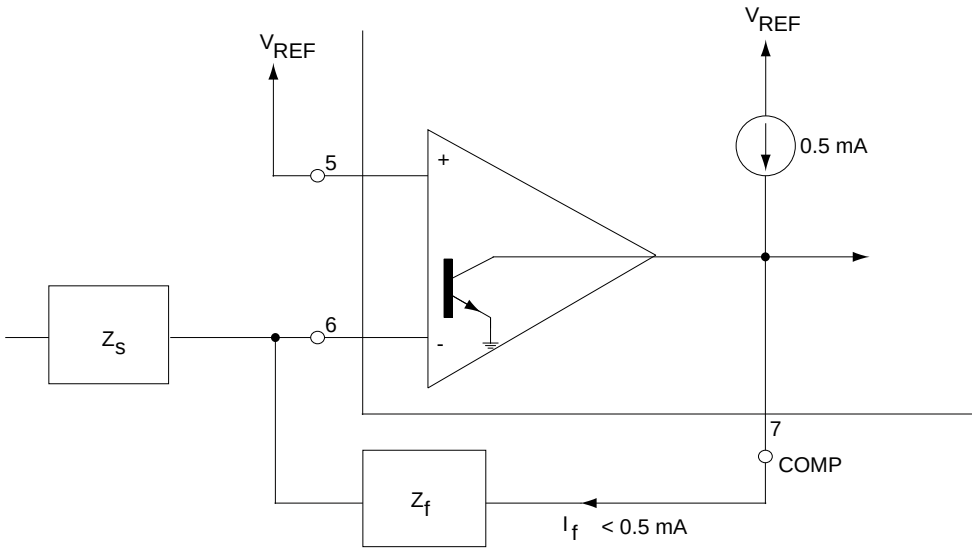


Figure 22 · Error AMP Output Configuration (Error amplifier can source up to 0.5 mA)

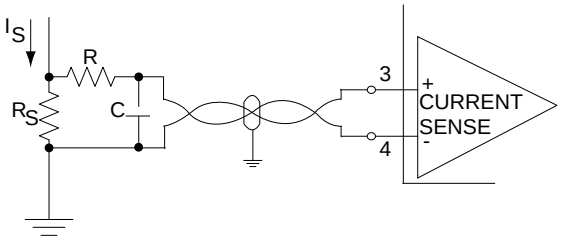


Figure 23 · Current Sense AMP Connections

A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise free switching.

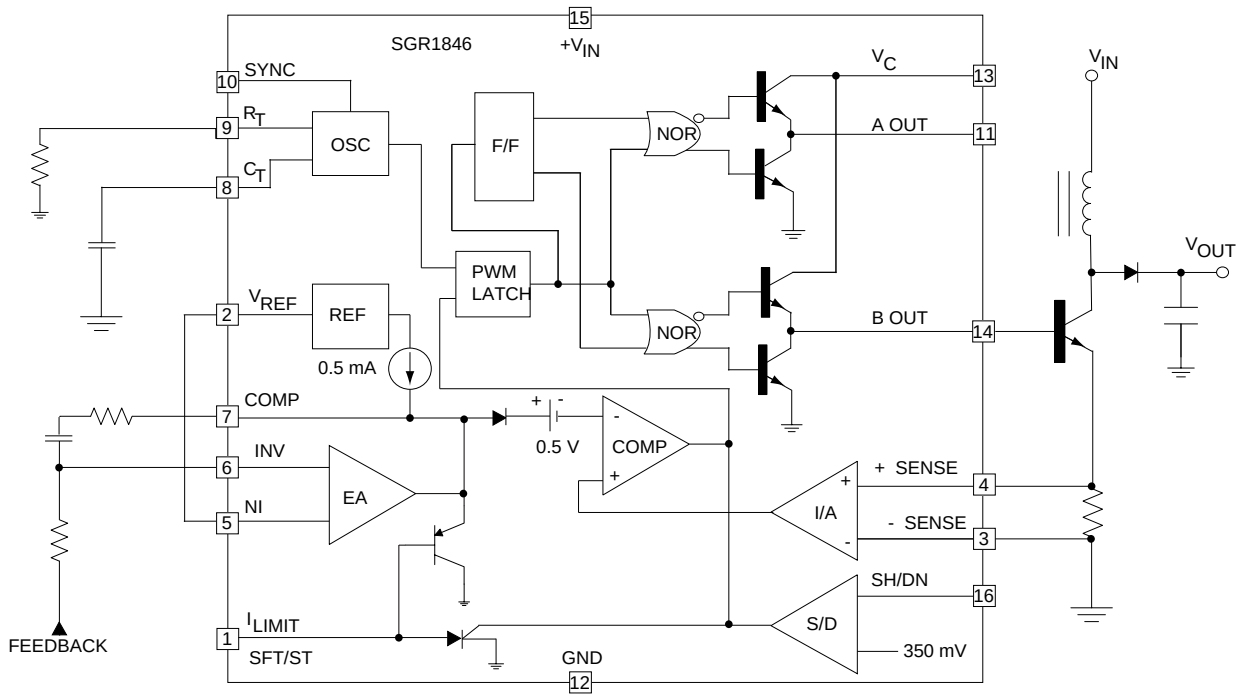


Figure 24 · Single Ended Boost Configuration

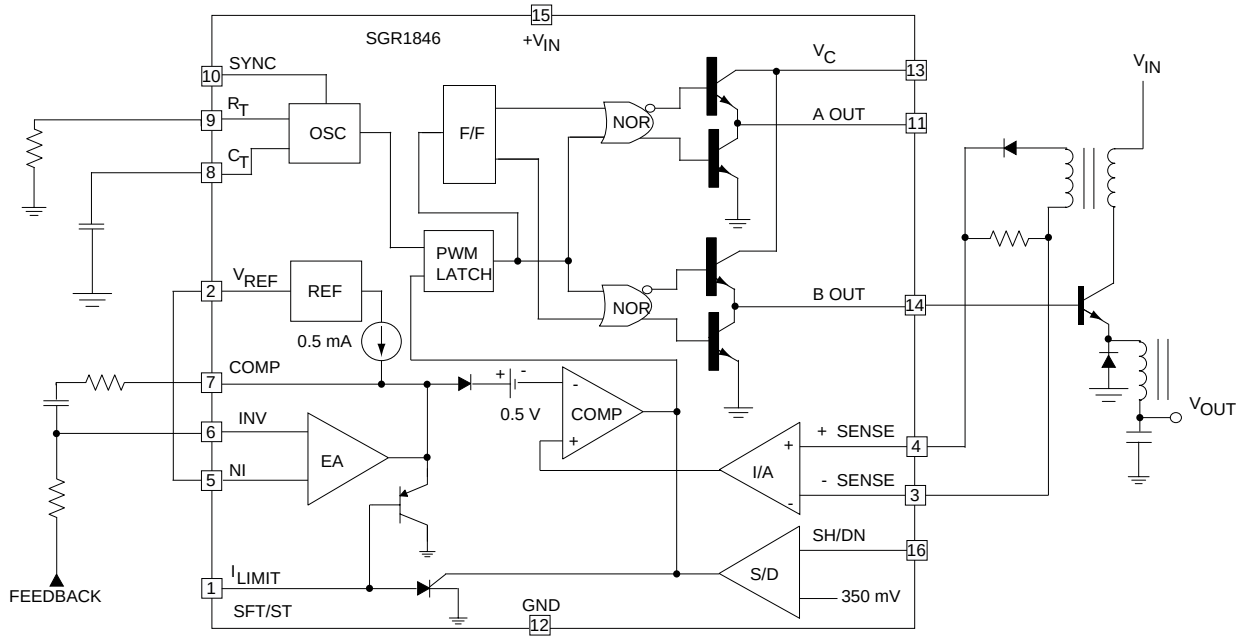


Figure 25 · Buck Converter with Current Sense Winding

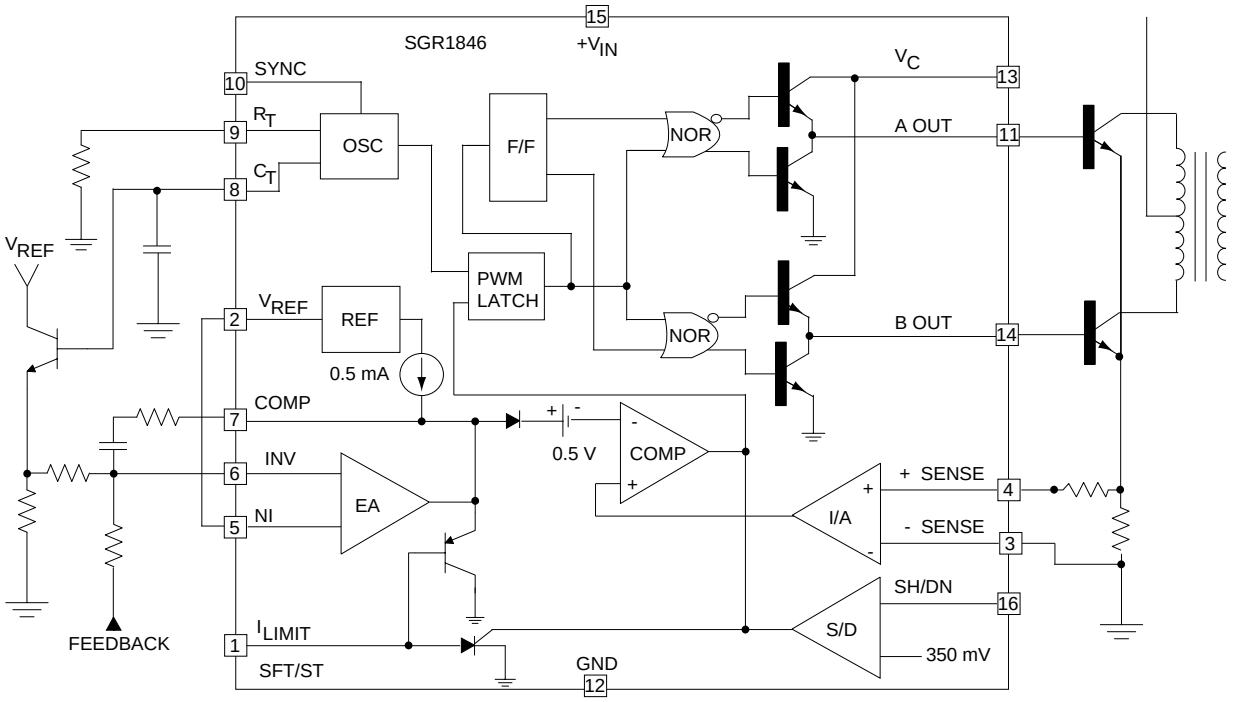


Figure 26 · Push/Pull Converter with Slope Compensation

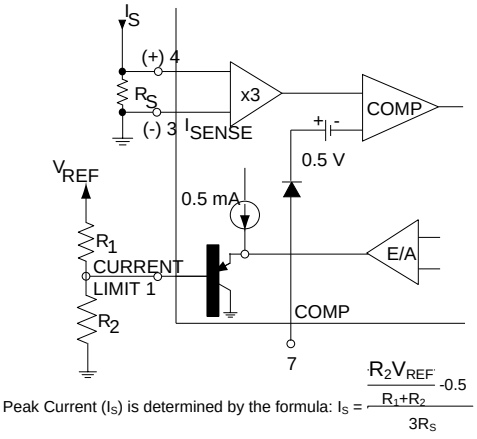


Figure 27 · Pulse by Pulse Current Limiting

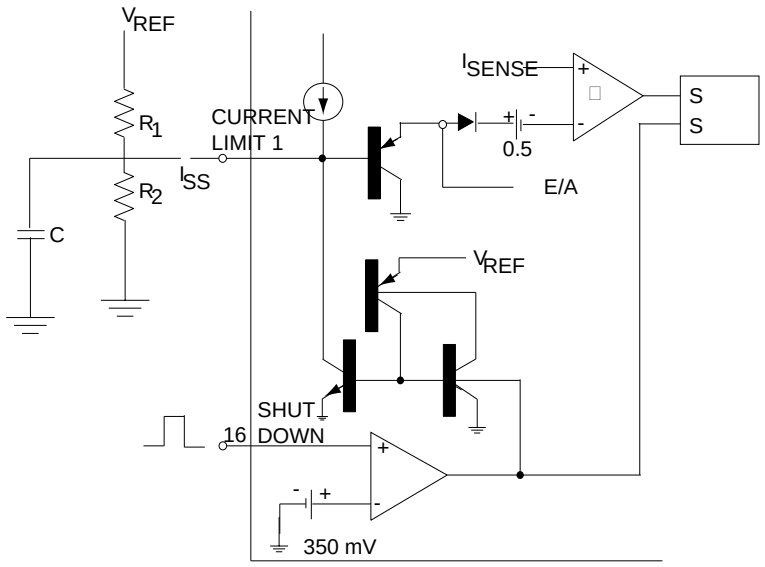


Figure 28 · Soft Start and Shutdown/Restart Functions

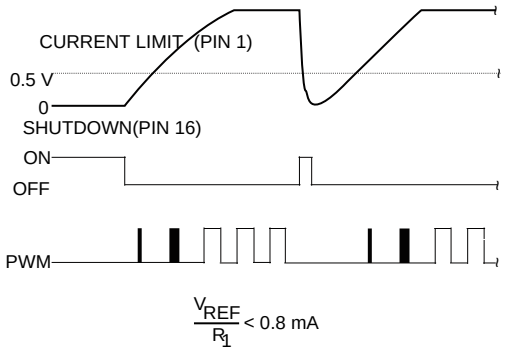


Figure 29 · Shutdown with Auto-Restart

If $\frac{V_{REF}}{R_1}$ < 0.8 mA, the shutdown latch commutates.
when I_{SS} < 0.8 mA, a restart cycle will be initiated.

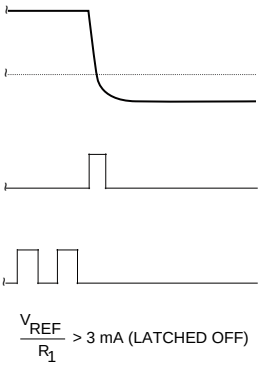
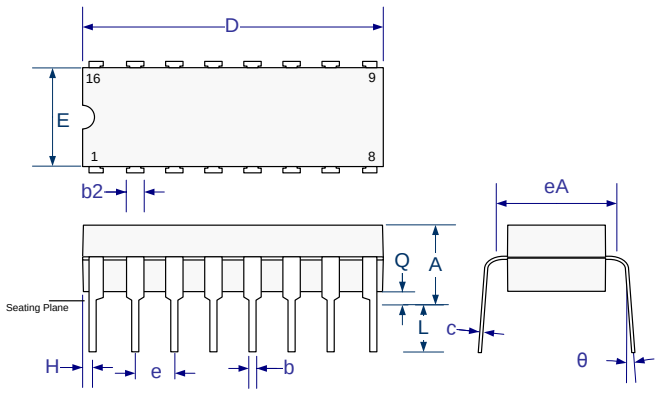


Figure 30 · Shutdown without Auto-Restart (Latched)

If $\frac{V_{REF}}{R_1}$ > 3 mA, the device will latch off until power is recycled.

PACKAGE OUTLINE DIMENSIONS

Controlling dimensions are in inches, metric equivalents are shown for general information.

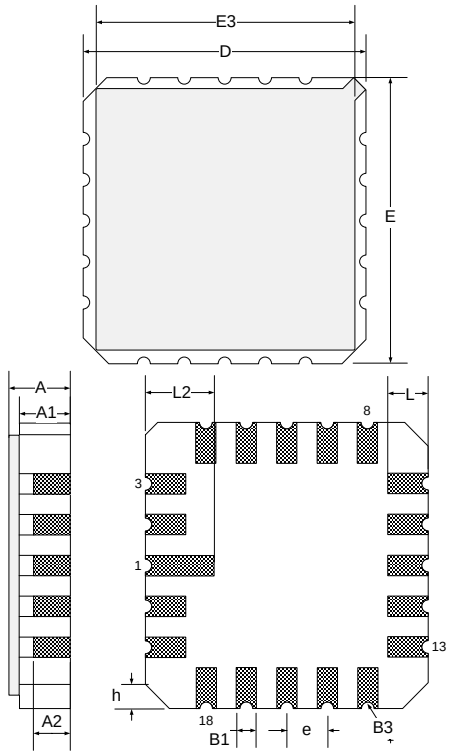


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		5.08		0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	19.30	19.94	0.760	0.785
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	5.08	0.125	0.200
α	-	15°	-	15°
Q	0.51	1.02	0.020	0.040

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 31 · J 16-Pin Ceramic Dual Inline Package Dimensions



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
D/E	8.64	9.14	0.340	0.360
E3	-	8.128	-	0.320
e	1.270 BSC		0.050 BSC	
B1	0.635 TYP		0.025 TYP	
L	1.02	1.52	0.040	0.060
A	1.626	2.286	0.064	0.090
h	1.016 TYP		0.040 TYP	
A1	1.372	1.68	0.054	0.066
A2	-	1.168	-	0.046
L2	1.91	2.41	0.075	0.95
B3	0.203R		0.008R	

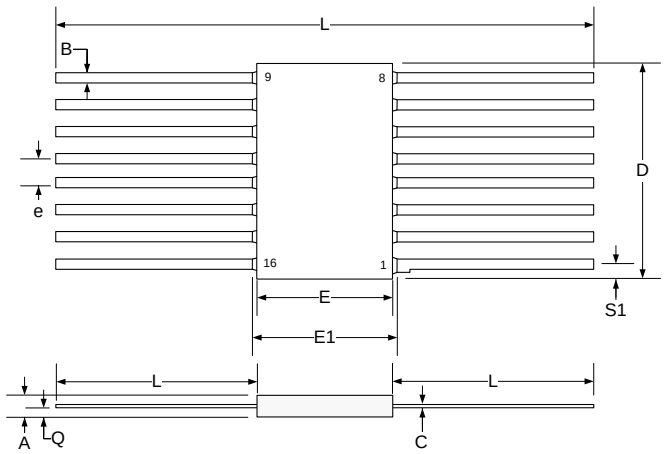
Note:

All exposed metalized area shall be gold plated 60 micro-inch minimum thickness over nickel plated unless otherwise specified in purchase order.

Figure 32 · L 20-Pin Ceramic Leadless Chip Carrier (LCC) Package Outline Dimensions

PACKAGE OUTLINE DIMENSIONS

Controlling dimensions are in inches, metric equivalents are shown for general information.



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.65	1.91	0.057	0.067
b	0.38	0.48	0.010	0.019
c	0.102	0.152	0.004	0.006
D	-	11.18	-	0.290
E	6.22	6.74	0.238	0.252
E1	-	7.62	-	0.272
e	1.27 BSC		0.050 BSC	
L	6.35	9.40	0.250	0.370
Q	0.51	1.02	0.020	0.040
S1	0.20		0.008	

Note:

1. Lead No. 1 is identified by tab on lead or dot on cover.
2. Leads are within 0.13mm (.0005") radius of the true position (TP) at maximum material condition.
3. Dimension "e" determines a zone within which all body and lead irregularities lie.

Figure 33 · F 16-Pin Ceramic Flatpack Package Dimensions

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