Characterization Report
CR0025: SmartFusion2 SoC FPGA and IGLOO2 FPGA for XAUI

Microsemi
Power Matters.

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Updated Overview section. For more information, see Overview, page 2.
- Updated XAUI Electrical Compliance Testing section. For more information, see XAUI 802.3 Electrical Compliance Testing, page 3.
- Updated table heading. For more information, see Table 6, page 8.
- Updated table heading. For more information, see Table 7, page 8.
- Deleted the Near-end Value column. For more information, see Table 9, page 12
- Added a Conclusion to section Return Loss. For more information, see Conclusion, page 16

1.2 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Overview

The Microsemi SmartFusion®2 SoC field programmable gate array (FPGA) and IGLOO®2 FPGA device family provides a fully embedded 10 Gigabit Attachment Unit Interface (XAUI). The XAUI is an interface specialized to 10 Gigabit Ethernet optical modules and system backplanes. It supports four SerDes transmit and four SerDes receive channels for 8B/10B encoding. XAUI is commonly used as backplane in networking switches to connect line cards to switch cards. This embedded XAUI block is part of the SerDesIF module, which supports four lanes of SerDes with data rates supported up to 3.125 Gbps. The number of SerDesIF modules on the SmartFusion2 SoC FPGA and IGLOO2 FPGA depends on the device size. The smaller devices support a single SerDesIF with one XAUI interface. The larger devices support up to four SerDesIF modules for a total of four XAUI interfaces. XAUI performance is available on –1 speed grade devices in all temperature grades of SmartFusion2 SoC FPGA and IGLOO2 FPGA products. For more information on the SmartFusion2 SoC FPGA and IGLOO2 FPGA device family can be found on the SmartFusion2 SoC FPGA and IGLOO2 FPGA Product Page at www.microsemi.com.

2.1 Scope

This test report provides a summary of completed SmartFusion2 SoC FPGA and IGLOO2 FPGA tests to meet compliance with the XAUI standards specified by IEEE 802.3ae 10 Gigabit Ethernet Task Force. The tests were conducted to analyze voltage, temperature, and process variations for XAUI electrical validation.

3 XAUI 802.3 Electrical Compliance Testing

XAUI electrical testing was completed based on IEEE Standard 802.3-2008 http://standards.ieee.org/getieee802/download/802.3-2008_section4.pdf. This document details physical layer specifications required to meet the 10 GBs sublayer requirements. This report highlights the procedures and conditions tested within the Microsemi factory to validate the device's performance against the XAUI specifications.

3.1 Transmitter Testing

All tests were performed over process, voltage, and temperature variations at the 3.125 GBs data rate to cover XAUI speeds per XAUI specification on M2S050-FG896 sample units. De-embedding mathematically removes the effects of unwanted portions of the PCB routing that would impede on the measured data by subtracting their contribution. This produces a portrayal of the devices actual performance.The S-Parameter de-embedding for Tx was applied during the Near-End measurements to remove board trace impairments. The following tables show the XAUI 802.3 test specifications for Near-End and Far-End tests.

Table 1 • **Transmitter Near-End Tests**

Parameter	IEEE 802.3 Definition	Specification Value	Units
XAUI Baud	Verify that the Baud rate of the device is within the conformance limits specified in 47.3.3.	3.125 GBaud ±100ppm	GBaud ppm
XAUI Unit Interval	Verify the serial bit rate per 47.3.3	320	pS
Driver single-ended output swing maximum absolute test (Tx+ and Tx–)	Verify that the single-ended output swing of the device is within the conformance maximum and minimum limits specified in Clause 47.3.3.2.	2.3	V
Driver single-ended output swing minimum absolute test (Tx+ and Tx–)		–400	mV
Transmitter differential return loss (output impedance)	Confirm the output impedance is within the limits of Clause 47.3.3.4.	< 3	dB

Table 2 • **Transmitter Far-End Tests**

Parameter	IEEE 802.3 Definition	Specification Value	Units
Driver output amplitude test	Verify that the driver differential output amplitude of the device is within the conformance limits specified in Clause 47.3.3.2.	800–1600	mVp-p
Driver eye template test	Verify that the devices transmitter meets the specified eye template requirements, Clause 47 (multiple sub-clauses).	Complies to all eye mask parameters including rise and fall times	
Total jitter test	To verify that the device conforms to the jitter requirements specified in Clause 47.3.3.5.	< 500	mUI
Deterministic jitter test		< 370	mUI

3.2 Receiver Testing

XAUI receiver electrical tests conform to the XAUI specification. All receiver tests were performed over process, voltage, and temperature variations at the 3.125 GBs data rate to cover XAUI speeds per XAUI specification on M2S050-FG896 units. To provide the correct amount of ISI, the receive test includes running the signal through several inches of board trace connected through SMP connectors. This ensures the signal, measured at the DUT, is stressed enough to meet XAUI requirements.

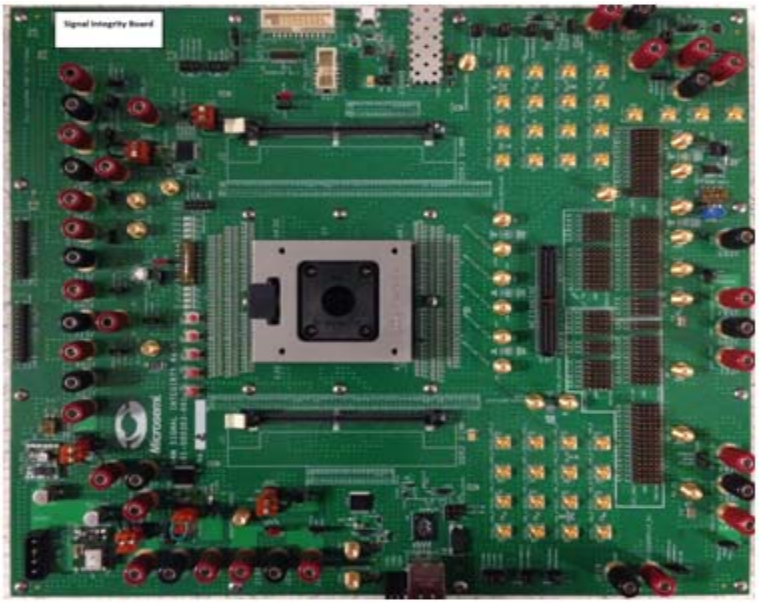
Table 3 • **Receiver Tests**

Parameter	IEEE 802.3 Definition	Specification Value	Units
Jitter tolerance margin	Verify XAUI Compliance Interconnect definition specified in Clause 47.4.1, for the purpose of this test suite, by stressing the input receiver.	0.65 Tj amplitude 0.37 DJ minimum 0.55 RJ minimum	UIp-p
Receiver coupling	AC coupled as defined in Clause 47.3.4.4	Included for all tests	
Sinusoidal jitter(Sj)		As needed to achieve Tj 650 mUIp-p	
Receiver input return loss	Verify the receiver's differential mode input impedance is within the limits of Clause 47.3.4.5.	> 10	
	Verify the receiver's common mode input impedance is within the limits of Clause 47.3.4.5.	> 6	

3.3 Microsemi Test Boards

Testing is performed on the Microsemi Signal Integrity Board (SI) that is equipped with a test socket and provides connections to vary power supply conditions. To ensure the integrity of the characterization measurements, special attention is given to the signal integrity of the high-speed serial channels. Detailed analysis ensures the board performs as designed. The transmitter (Tx) and receiver (Rx) signal paths for each SerDes are carefully routed to high-bandwidth SMP connectors to ensure good signal integrity and performance. The PCB channel is measured and de-embedded when performing tests.

Figure 1 • **SmartFusion2 SoC FPGA and IGLOO2 FPGA Signal Integrity Board**



3.4 Device Testing Samples

Testing was conducted on a sample of devices representing process variations across silicon fabrication. These devices were separated from a larger group of devices representing the worse-case corners to report the results. The results are correlated as presented in the data as worst-case.

4 Electrical Device Testing

Bench test equipment was used for both Rx jitter and Tx jitter and amplitude measurements.

4.1 Electrical Testing Equipment/Software

- Agilent DSA91304A, 13GHz Real-Time Scope or DSO93204A 32Ghz Real-Time Scope
- Agilent N5431A XAUI Automation Test Application, Version 1.24 or newer
- Tektronix BERTScope BSA125C with BERTScope GUI
- Tektronix BERTScope DPP125B, Digital Pre-emphasis Processor
- Tektronix BERTScope CR12500A, Clock Recovery Module
- Agilent E3648A 100W Dual Output Power Supply
- Agilent N6701A Power Supply Mainframe
- Four individually controlled P/S Modules
- Silicon Thermal, Temperature Control Unit
- Silicon Thermal Chiller CH400
- Silicon Thermal Linear Power Supply PS190-L
- Silicon Thermal Temperature Controller LB190-L
- Silicon Thermal 31x31(mm) Thermal Head Adapter
- SMA-to-SMA cables
- SMA-to-SMP cables
- Microsemi Engineering. Signal Integrity Board
- Agilent 11742A DC blocks
- Stanford Research Systems CG635 2.05 GHz Synthesized Clock Source

4.2 Electrical Testing Environment

Device electrical testing was conducted by the Microsemi factory using variations on power supply voltages and temperatures. Minimum voltage (Vmin) and maximum voltage (Vmax) were varied by ±5% of the typical voltage (Vtyp) supply for the supplies related to the XAUI and SerDes blocks of the device. The devices were also tested at the industrial temperature limits (-40ºC to +125ºC).

Table 4 • **Temperature Specifications**

Specification	Temperature Range
Military temperatures	–55°C to 125°C
Industrial temperatures	–40°C to 100°C
Commercial temperatures	0°C to 85°C

The following table shows the testing conditions for power supply and temperature tests.

Table 5 • **Power Supply and Temperature Test Conditions**

Voltage and Temperature Matrix						
Voltage Dependencies	**1.2 V VDD Range**					
xDDR_PLL_VDDA	3.15 V	3.3 V	3.45 V	3.15 V	3.3 V	3.45 V
CCC_xyz_PLL_VDDA	2.375 V	2.5 V	2.625 V	3.15 V	3.3 V	3.45 V
SERDES_x_PLL_VDDA	2.375 V	2.5 V	2.625 V	3.15 V	3.3 V	3.45 V
SERDES_x_L[0:3]VDDAPLL	2.375 V	2.5 V	2.625 V	2.375 V	2.5 V	2.625 V
SERDES_x_L[0:3]VDDAIO	1.14 V	1.2 V	1.26 V	1.14 V	1.2 V	1.26 V
SERDES_x_VDD	1.14 V	1.2 V	1.26 V	1.14 V	1.2 V	1.26 V
VDD (core supply)	1.14 V	1.2 V	1.26 V	1.14 V	1.2 V	1.26 V

Table 5 • **Power Supply and Temperature Test Conditions**

Voltage and Temperature Matrix						
Voltage Dependencies	**1.2 V VDD Range**					
Temperatures	–55ºC	–55ºC	–55ºC	–55ºC	–55ºC	–55ºC
	–40ºC	–40ºC	–40ºC	–40ºC	–40ºC	–40ºC
	0ºC	0ºC	0ºC	0ºC	0ºC	0ºC
	25ºC	25ºC	25ºC	25ºC	25ºC	25ºC
	85ºC	85ºC	85ºC	85ºC	85ºC	85ºC
	100ºC	100ºC	100ºC	100ºC	100ºC	100ºC
	125ºC	125ºC	125ºC	125ºC	125ºC	125ºC

5 XAUI Test Results

The following tables are a summary of the test results.

Table 6 • **Transmitter Testing**

	IEEE 802.3 Specification		SmartFusion2 and IGLOO2 Device		
Test	**Parameter**	**Specifications**	**Worst Case Test Results**	**Unit**	**Pass/Fail**
Baud rate	Within range	–100.000 Bd ppm <= VALUE <= 100.000 Bd ppm	–4.8	ppm	Pass
Driver single-ended output swing maximum absolute test (Tx+) (near-end)	Maximum	VALUE <= 2.300 V	209	mV	Pass
Driver single-ended output swing minimum absolute test (Tx+) (near-end)	Minimum	VALUE >= –400 mV	–230	mV	Pass
Driver single-ended output swing maximum absolute test (Tx-) (near-end)	Maximum	VALUE <= 2.300 V	206	mV	Pass
Driver single-ended output swing minimum absolute test (Tx-) (near-end)	Minimum	VALUE >= –400 mV	–231	mV	Pass
Driver output amplitude test (far-end)	Within range	0.200 V <= VALUE <= 1.600 V	674	mV	Pass
Driver eye template test (far-end)	N/A	Zero mask failures	N/A	N/C	Pass
Total jitter test (far-end)	Maximum	VALUE <= 550 mUI	168	mUI	Pass
Deterministic jitter test (far-end)	Maximum	VALUE <= 370 mUI	135	mUI	Pass
Differential return loss	Maximum	VALUE < 3	< 3	dB	Pass

Table 7 • **Receiver Testing**

	IEEE 802.3 Specification		SmartFusion2 and IGLOO2 Devices		
Test	**Parameter**	**Specifications**	**Worst Case Test Results**	**Unit**	**Pass/Fail**
Total jitter (Tj)	Maximum	650 mUIp-p	< 650	mUI	Pass
Deterministic jitter (Dj)	Maximum	370 mUIp-p	< 370	mUI	Pass
Deterministic + random jitter (Dj+Rj)	Maximum	550 mUIp-p	< 550	mUI	Pass
Sinusoidal jitter (Sj)		As needed to achieve Tj 650 mUIp-p		mUI	Pass
Differential return loss	Minimum	> 10	> 10	dB	Pass

Table 7 • **Receiver Testing**

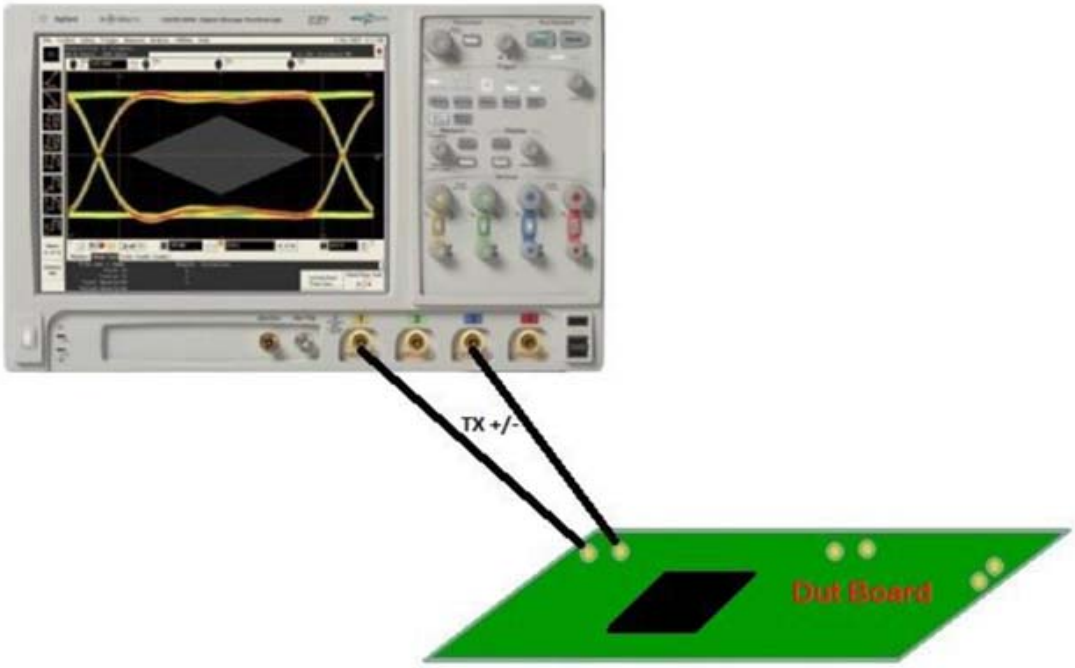
	IEEE 802.3 Specification		SmartFusion2 and IGLOO2 Devices		
Test	**Parameter**	**Specifications**	**Worst Case Test Results**	**Unit**	**Pass/Fail**
Common mode return loss	Minimum	> 6	> 6	dB	Pass

5.1 XAUI Transmitter Tests

The characterization has been performed in accordance with XAUI specification for Near-End and Far-End measurements. The transmitter Near-End jitter is measured at a load terminated driver output. The XAUI RefCLK is taken from the external clock source generator. The signal is driven from a test signal source generating a CJPAT test pattern. CJPAT is a binary pattern sequence that exposes a receiver's CDR to large instantaneous phase jumps. The pattern alternates between repeating low-transition density patterns with repeating high-transition density patterns.

A sample of devices was tested over voltage and temperature and represents the worst case condition for the transmitter tests. The worst test condition identified was temperature = –55ºC and voltage at Vmax.

Figure 2 • **Transmitter Test Setup**



The total and deterministic jitter are shown in the following illustrations.

Figure 3 • **Total Jitter Histogram**

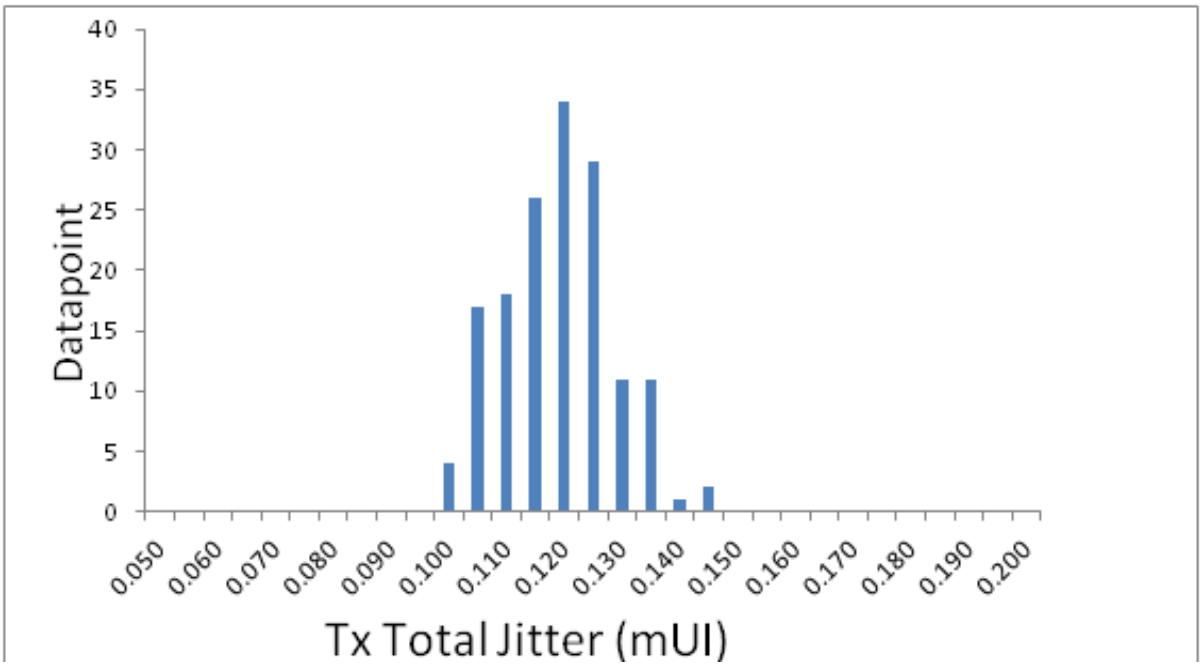


Figure 4 • **Deterministic Jitter Histogram**

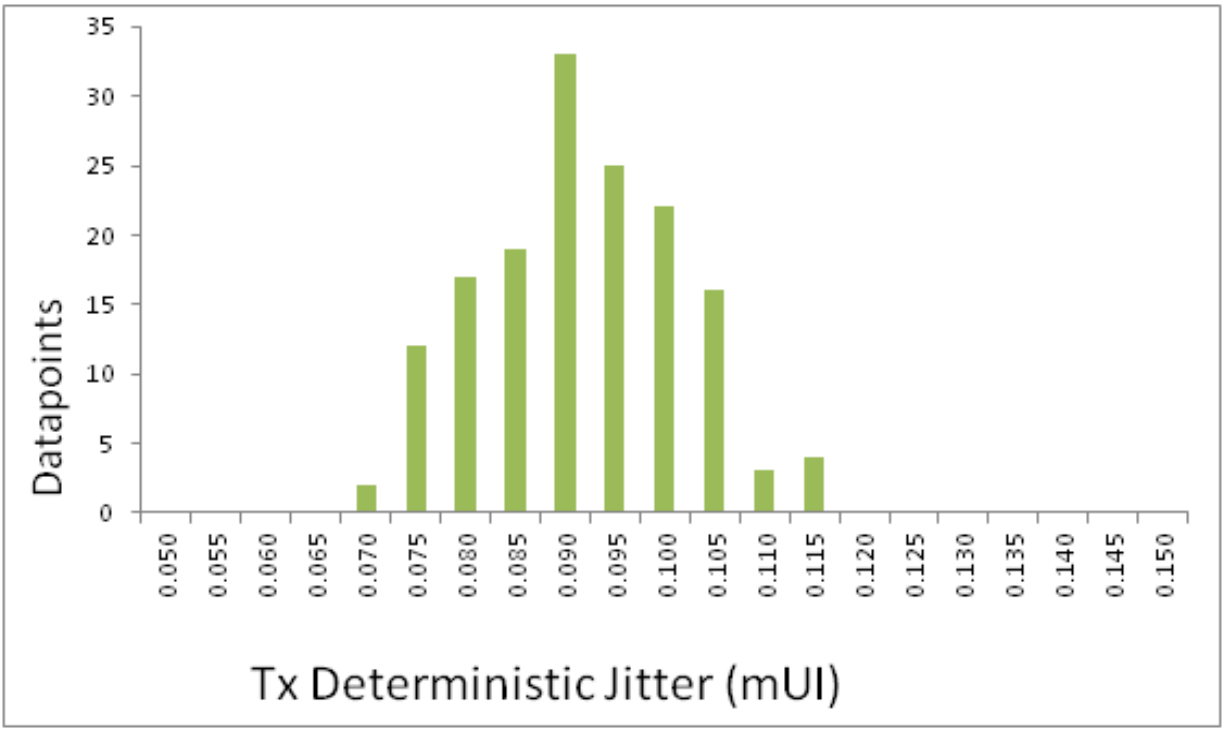


Table 8 • **Worse Case Transmit Jitter Summary**

Jitter	Min	Max	Mean	Interval
Total jitter	97	141	117	mUI

Table 8 • **Worse Case Transmit Jitter Summary**

Jitter	Min	Max	Mean	Interval
Deterministic jitter	67	115	90	mUI

The following illustration shows the XAUI jitter decomposition of transmitter using CJPAT.

Figure 5 • **Jitter Decomposition of Transmitter**

Figure 6 • **Transmit Eye Mask**

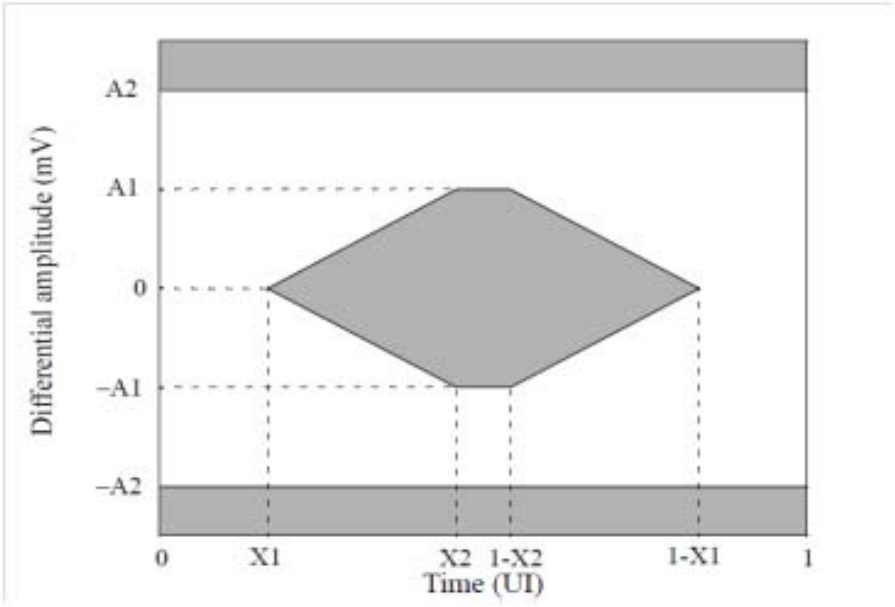
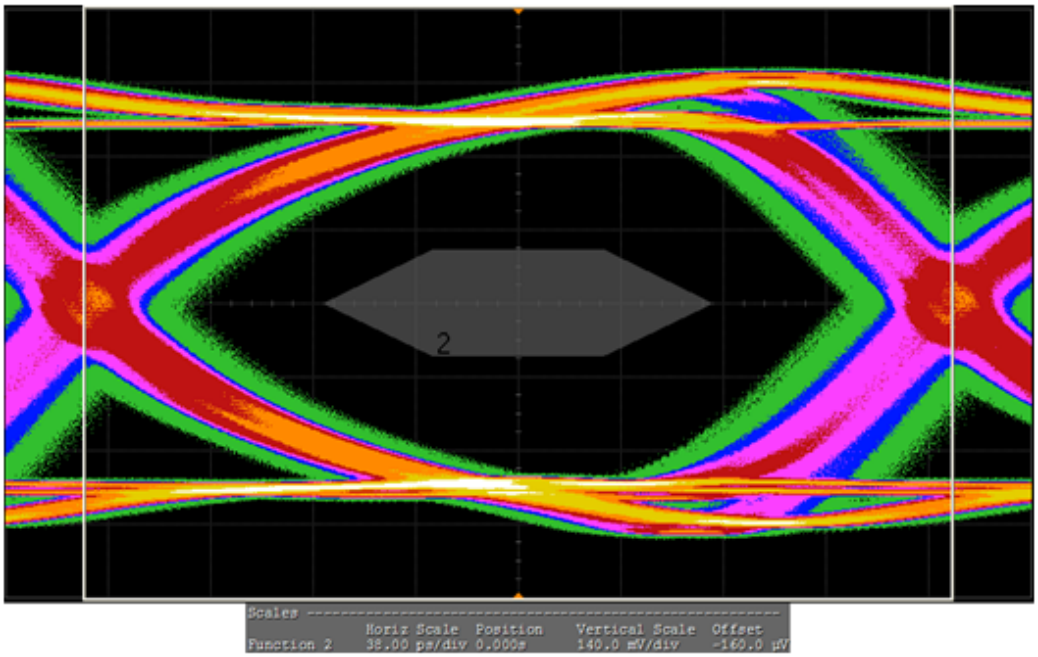


Table 9 • **Transmit Eye Intervals**

Symbol	Far-End Value	Units
X1	0.275	UI
X2	0.400	UI
A1	100	mV
A2	800	mV

The following illustration shows the transmit eye diagram with Far-End mask.

Figure 7 • **Transmit Eye Diagram**



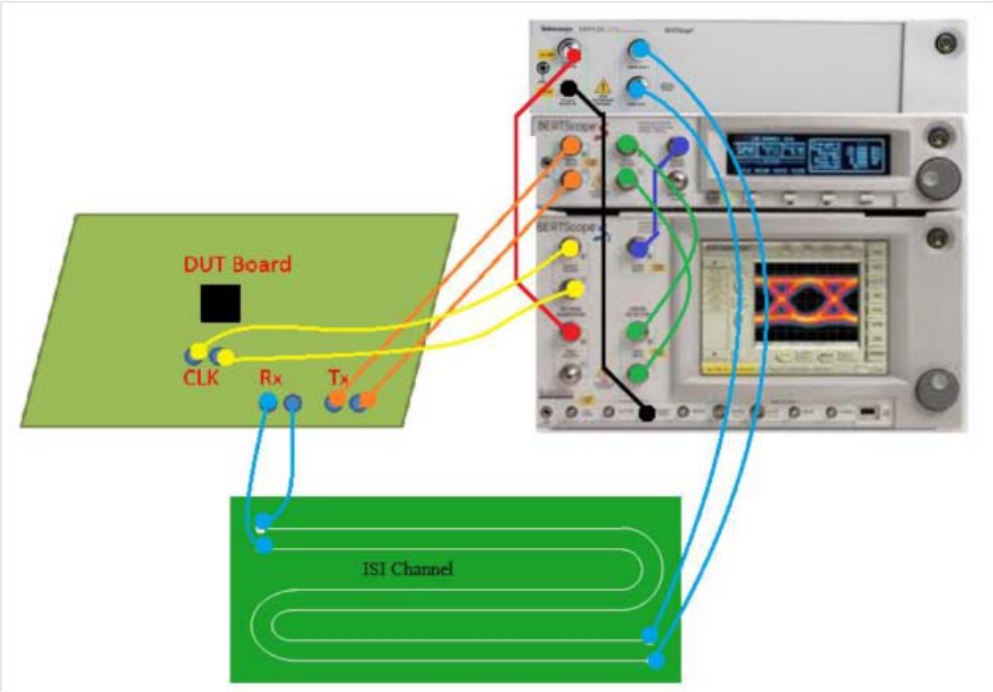
5.2 XAUI Receiver Setup and Testing

A XAUI Compliance Channel setup is used for the XAUI receiver testing per Clause 47.3.4.2. The objective of the test is to provide a stressed input signal to the device and still have the receiver operate with a bit-error rate (BER) of better than 10–12.

The BERTScope, DPP, and clock recovery are interconnected together to provide a necessary signal generator for XAUI receiver testing. The XAUI receiver channel is pre-conditioned with a calibrated setup including a 55" (ISI) backplane trace that is combined with a test board trace between SMP and DUT's package to generate required 370 mUI of Dj. This setup guarantees calibration of the XAUI Compliant Stressed Eye to the Rx package balls of the device.

The XAUI receiver setup uses Common RefCLK topology by having RefCLK driven by the BERTScope.

Figure 8 • **XAUI Receiver Test Setup**



Note: ISI Channel = 55 inches

Figure 9 • **Stress Input Signal**

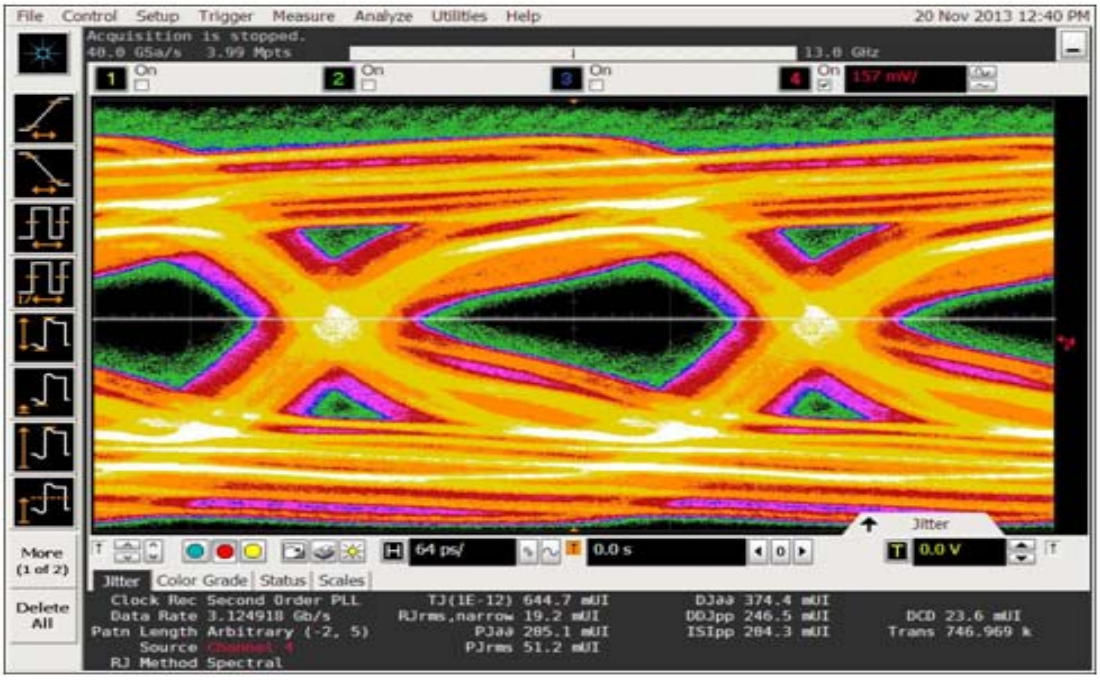


Table 10 • **Stressed Input Eye Jitter Components**

Jitter Measurement	Value	Unit
Data rate	3.1249	Gb/s

Table 10 • **Stressed Input Eye Jitter Components**

Jitter Measurement	Value	Unit
TJ(1E-12)	644.7	mUI
RJ-rms	19.2	mUI
PJ-rms	51.2	mUI
DDJ-pp	246.5	mUI
ISI-pp	284.3	mUI
DCD	23.6	mUI

The stressed input signal must meet the Far-End eye mask while introducing the required jitter components. Figure 7, page 12 shows the stressed eye and the reported jitter components. The signal is driven from a test signal source generating a CJPAT test pattern. CJPAT is a binary pattern sequence that exposes a receiver's CDR to large instantaneous phase jumps. The pattern alternates repeating low-transition density patterns with repeating high-transition density patterns. The purpose of the test is to feed in a jitter signal while observing the receiver's lock status, stability, and data BER. The receiver must be AC coupled, and the input is measured at the pin of the receiver.

Additional sinusoidal jitter is added from the BERTScope tester and swept as a function of frequency to the point where the device starts to fail. The BER is compared to a jitter tolerance mask where jitter is applied to the stressed input channel. Figure 8, page 13 plots the results of the sample devices in comparison to the XAUI specified mask.

Figure 10 • **Single Tone Sinusoidal Jitter Mask**

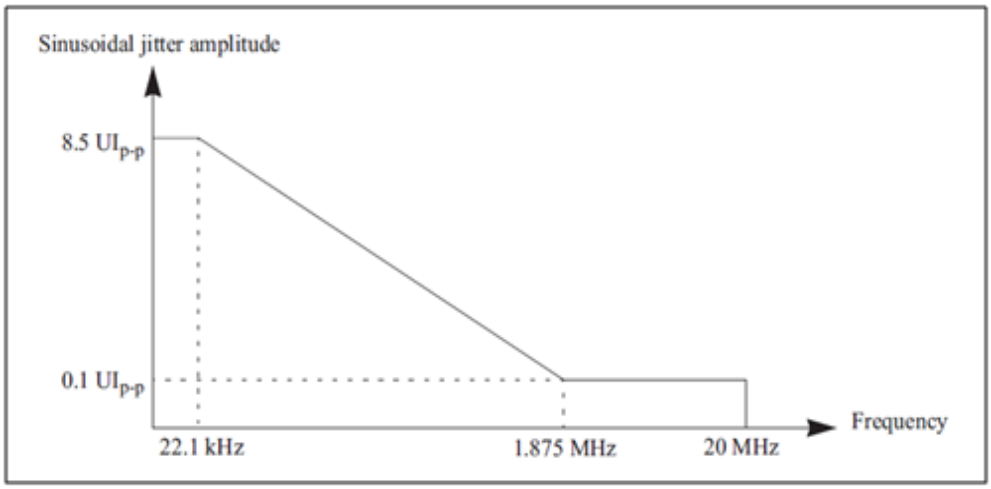
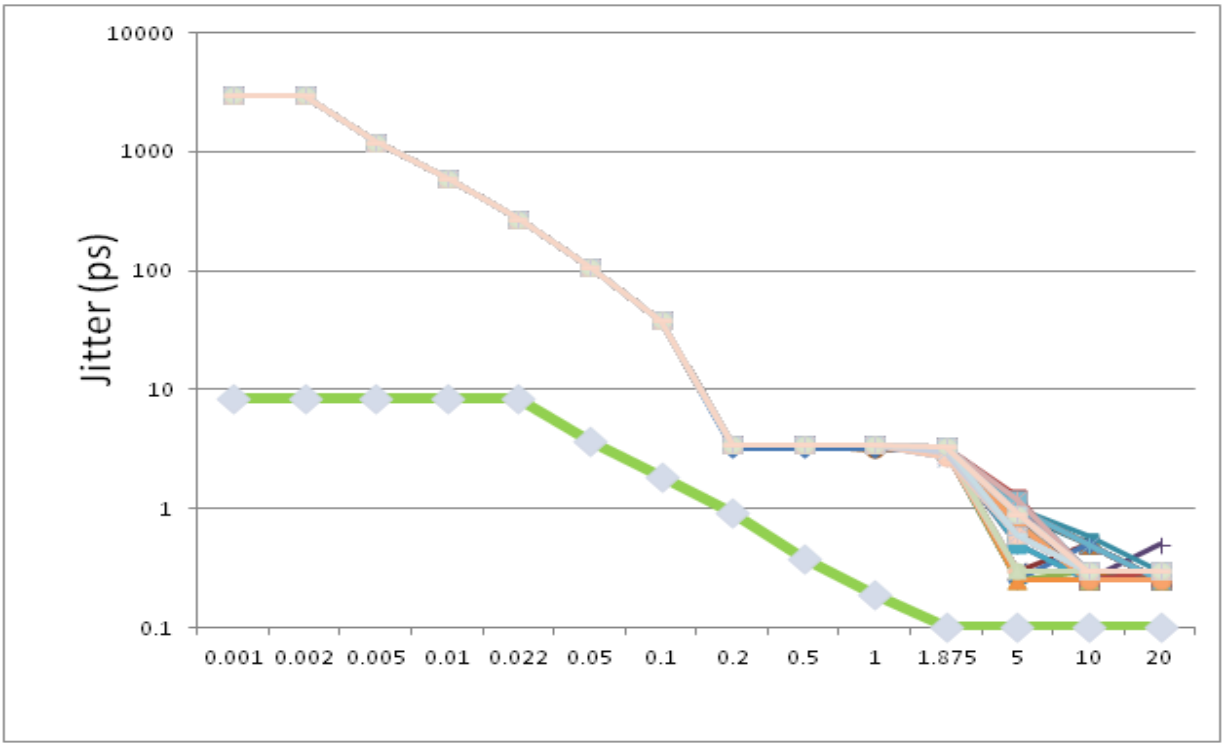


Figure 11 • **Sinusoidal Jitter Tolerance Test Plot**



5.2.1 Return Loss

The primary effect of return loss relates to the amount of signal being transferred to the receiver causing closure of the eye. Multiple reflections, caused by the finite return loss of driver in conjunction with the channel, introduce additional amplitude distortion as well as jitter. Return loss measurements of the SmartFusion2 SoC FPGA and IGLOO2 FPGA include the contributions from the on-chip, off-chip, and package components of both the receiver and the transmitter. The receiver tests included AC coupling capacitors. The tests used frequency domain return loss measurements, where the loss is measured while sweeping the frequency from 100 MHz to 5 GHz.

Figure 12 • **Tx Return Loss Plot**

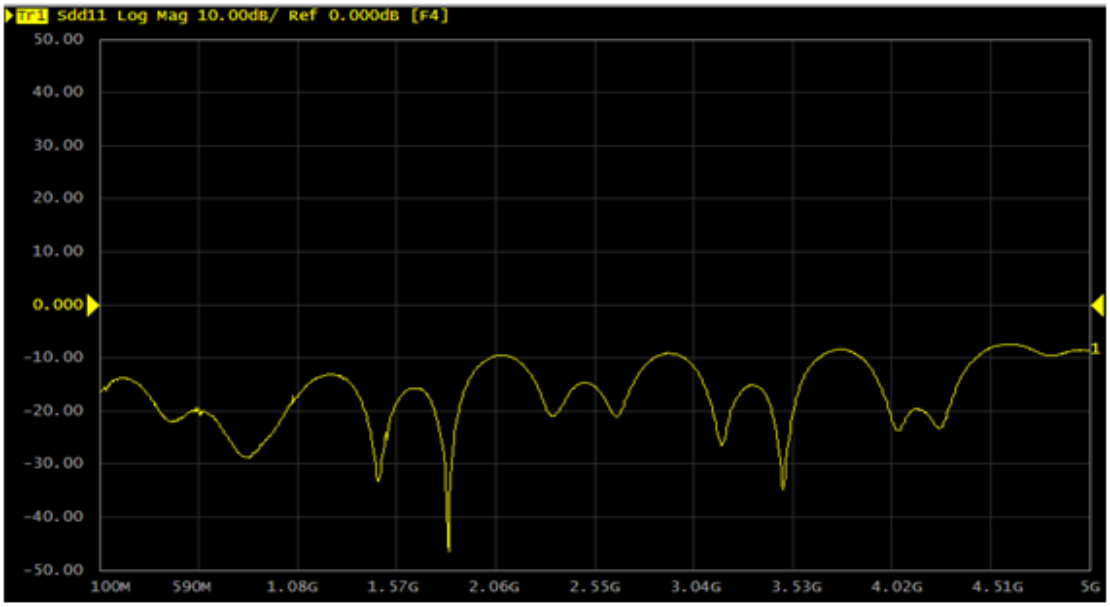
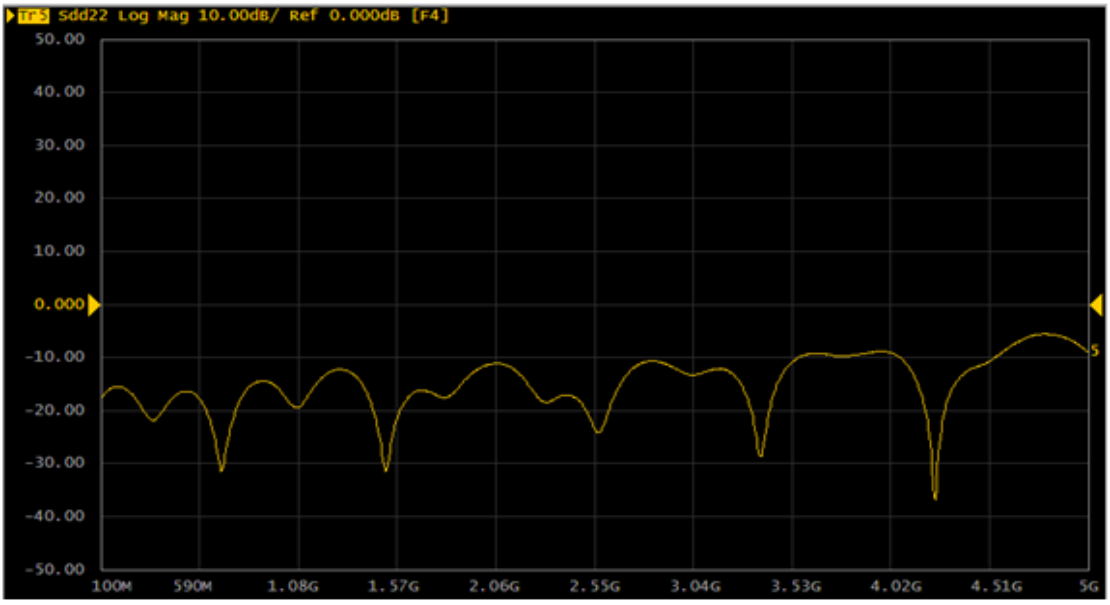


Figure 13 • **Rx Return Loss**



Conclusion

The test results demonstrate the capabilities of the SmartFusion2 SoC FPGA and the IGLOO2 FPGA XAUI solution. XAUI systems require high reliability requiring devices to be robust. The report provides a baseline summary of the thorough testing performed by the Microsemi factory to assure users that the device will meet the performance and functional requirements in their customized XAUI application.