Figures

Figure 1. Demo Design Files Top-Level Structure .................................................. 8
Figure 2. IGL2_MDDR_Demo SmartDesign .......................................................... 9
Figure 3. MDDR_Demo_0 SmartDesign Component ............................................. 10
Figure 4. UART_IF_0 SmartDesign Component ................................................... 12
Figure 5. AXI_LPDDR_Simulation SmartDesign Testbench ............................... 13
Figure 6. DO File Settings ................................................................................... 14
Figure 7. Waveforms Settings ............................................................................. 14
Figure 8. Invoking Organize Stimulus Files Window .......................................... 15
Figure 9. Organize Stimulus Files Window .......................................................... 15
Figure 10. Transcript Window ............................................................................ 16
Figure 11. Single Write and Read Operation ....................................................... 17
Figure 12. 16-Beat AXI Burst Write and Read ..................................................... 17
Figure 13. IGLOO2 Evaluation Kit ....................................................................... 18
Figure 14. USB Serial 2.0 Port Properties ........................................................... 19
Figure 15. FlashPro New Project .......................................................................... 20
Figure 16. FlashPro Project Configuration ............................................................ 21
Figure 17. FlashPro Program Passed ................................................................... 22
Figure 18. IGL2_MDDR_Demo Utility ................................................................. 23
Figure 19. IGL2_MDDR_Demo- Connection Status ............................................ 24
Figure 20. Single Write Operation ....................................................................... 25
Figure 21. Clear Data Field .................................................................................. 25
Figure 22. Single Read Operation ....................................................................... 26
Figure 23. Burst Write Operation ........................................................................ 27
Figure 24. Burst Read Operation ......................................................................... 27
Figure 25. System Builder - Memories - MDDR Tab .......................................... 28
Figure 26. System Builder MDDR Configuration – General Tab ....................... 29
Figure 27. System Builder MDDR Configuration – Memory Initialization Tab .... 30
Figure 28. System Builder MDDR Configuration – Memory Timing Tab ............ 31
Figure 29. USB 3.0 Serial Port Properties ............................................................ 32
Figure 30. Read Error ......................................................................................... 33
Figure 31. Non 64-bit Aligned Address ............................................................... 34
Figure 32. Converted 64-bit Aligned Address ...................................................... 35
Tables

Table 1. Design Requirements ................................................................. 7
Table 2. IGLOO2 FPGA Evaluation Kit Jumper Settings ................................. 18
1 Preface

1.1 Purpose
This demo guide is for IGLOO®2 field programmable gate array (FPGA) devices. It provides instructions on how to use the corresponding reference design.

1.2 Intended Audience
This demo guide is intended for:
• FPGA designers
• System-level designers

1.3 References
The following documents are referred in this demo guide:
• UG0446: SmartFusion2 and IGLOO2 FPGA High Speed DDR Interfaces User Guide
• UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide
• IGLOO2 System Builder User Guide
• UG0478: IGLOO2 Evaluation Kit User Guide
• CoreUART Handbook

Refer to the following web page for a complete and up-to-date listing of IGLOO2 device documentation:
2 Interfacing IGLOO2 FPGA with External LPDDR Memory through MDDR Controller

2.1 Introduction

This demo shows that the high-performance memory subsystem (HPMS) double data rate (DDR) controller accessing the external DDR synchronous dynamic random access memory (SDRAM) memories in the IGLOO2 devices.

This demo has two parts:

- Demo using simulation
- Demo using the IGLOO2 Evaluation Kit

In the demo design, AXI master in the FPGA fabric accesses the low power DDR (LPDDR) memory present in the IGLOO2 Evaluation Kit board using the microcontroller/memory subsystem double data rate (MDDR) controller. A utility, IGL2_MDDR_Demo is provided along with the demo deliverables. Using the utility, you can drive the AXI master logic. AXI master converts the commands from the utility to AXI transactions for the MDDR controller to perform the read/write operations on the LPDDR memory.

2.2 Design Requirements

Table 1 shows the design requirements.

<table>
<thead>
<tr>
<th>Design Requirements</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Hardware Requirements</strong></td>
<td></td>
</tr>
<tr>
<td>IGLOO2 Evaluation Kit:</td>
<td>Rev C or later</td>
</tr>
<tr>
<td>- FlashPro4 programmer</td>
<td></td>
</tr>
<tr>
<td>- 12 V adapter</td>
<td></td>
</tr>
<tr>
<td>- USB A to Mini-B cable</td>
<td></td>
</tr>
<tr>
<td>Host PC or Laptop</td>
<td>Any 64-bit Windows Operating System</td>
</tr>
<tr>
<td><strong>Software Requirements</strong></td>
<td></td>
</tr>
<tr>
<td>Libero® System-on-Chip (SoC)</td>
<td>v11.8 SP2</td>
</tr>
<tr>
<td>FlashPro programming software</td>
<td>v11.8 SP2</td>
</tr>
<tr>
<td>Microsoft .NET Framework 4</td>
<td></td>
</tr>
<tr>
<td>Host PC Drivers</td>
<td>USB to UART drivers</td>
</tr>
</tbody>
</table>
2.3 Demo Design

2.3.1 Introduction

The demo design files are available for download from the following path in the Microsemi website: http://soc.microsemi.com/download/rsc/?f=m2gl_dg0534_liberov11p8sp2_df

Design files include:

- Demo_Utility
- Libero_project
  - IGL2_MDDR_Demo
- Programming_file
- Source_files
- readme.txt

*Figure 1* shows the top-level structure of the design files. For further details, refer to the *readme.txt* file.

*Figure 1 • Demo Design Files Top-Level Structure*

```
<download_folder>
  IGL2_MDDR_Demo_DF
    Demo_Utilty
    Libero_project
      IGL2_MDDR_Demo
    Programming_file
    Source_files
    readme.txt
```

In the demo design, AXI master implemented in the FPGA fabric accesses the LPDDR memory present in the IGLOO2 Evaluation Kit board using the MDDR controller. The AXI master logic communicates to the MDDR controller via CoreAXI interface and the DDR_FIC interface. The read/write operations initiated by the *IGL2_MDDR_Demo* utility are sent to the UART_IF block using the UART protocol. AXI master receives the address and data from the UART_IF block.

During a write operation, the UART_IF block sends the address and data to the AXI master logic. During a read operation, the UART_IF block sends the address to the AXI master and stores the read data in TPSRAM. When the read operation is complete, the read data is sent to the host PC via UART.
Figure 2 shows the top-level view of demo design.

In this demo design, the following blocks are configured:

- MDDR controller is configured for LPDDR memory available in the IGLOO2 Evaluation Kit board. The LPDDR memory is a Micron® DRAM (Part Number: MT46H32M16LF).
- DDR_FIC is configured for AXI bus interface.
- Both AXI clock and LPDDR clock are configured for 160 MHz.
- CoreUART IP has the following configuration:
  - Baud Rate: 115200
  - Data Bits: 8
  - Parity: None
- TPSRAM IP has the following configuration:
  - Write port depth: 256
  - Write port width: 64
  - Read port depth: 2048
  - Read port width: 8
Refer to "Appendix: Configuring MDDR Controller" on page 28 for more information on how to configure the DDR controller.

### 2.3.2 Features

The IGLOO2 MDDR demo design has the following features:

- Single AXI read/write transactions
- 16-beat burst AXI read/write transactions
- LPDDR memory model simulation using SmartDesign testbench
- Design validation using the IGLOO2 Evaluation Kit board that has the LPDDR memory
- Initiation of the read/write transactions using IGL2_MDDR_Demo utility

### 2.3.3 Description

The demo design consists the following SmartDesign components:

- **MDDR_Demo_0**: This SmartDesign handles the data transactions between the MDDR controller and LPDDR SDRAM.
- **UART_IF_0**: This SmartDesign handles the communication between the host PC and the IGLOO2 Evaluation Kit board.

*Figure 3 shows the MDDR_Demo_0 and UART_IF_0 connection.*

#### Figure 3 • IGL2_MDDR_Demo SmartDesign

### 2.3.3.1 MDDR_Demo_0

MDDR_Demo_0 consists the MDDR_Demo_sb_0 subsystem generated using the system builder and the AXI_IF_0 master logic. The AXI_IF_0 master logic is an RTL code that implements the AXI read and write transactions. It receives the read/write operations, burst length (RLEN and WLEN), address and data as inputs. Based on inputs received, it communicates with the LPDDR memory through the MDDR controller.
Figure 4 shows the MDDR_Demo_0 SmartDesign component.

**Figure 4 • MDDR_Demo_0 SmartDesign Component**

### 2.3.3.2 UART_IF_0

The UART_IF_0 SmartDesign component handles the UART communication between host PC demo utility and the AXI master logic. The COREUART_0 IP receives the UART signals from the host PC user interface. The UART_IF_FSM_0 is a wrapper for COREUART_0, collects the data from COREUART_0 IP and converts the data to the relevant AXI_IF_0 master signals.

For a single write operation, the UART_IF_FSM_0 wrapper receives the address and data from the demo utility. For a burst write operation, the address and data are received from the demo utility and the subsequent incremental data are provided by the UART_IF_FSM_0 wrapper.

For a burst read operation, UART_IF_FSM_0 collects the address from the demo utility and sends that to the AXI_IF_0 master logic. It then receives the read data from the AXI_IF_0 master logic and stores it in the TPSRAM_0. After completion of the read burst transactions, the UART_IF_FSM_0 wrapper fetches the stored data from the TPSRAM_0 and sends it to the COREUART IP.
2.4 Running the Demo Using Simulation

The demo design can be simulated using SmartDesign testbench and LPDDR memory model (MT46H32M16LF with 512 Mb density).

The simulation is set to run the following:

- Single AXI write and read operation
- 16-beat AXI burst write and read operation
Figure 6 shows the AXI_LPDDR_Simulation SmartDesign testbench. The AXI_testbench provides the read/write operations, burst length, address, and data to the MDDR_Demo_0 SmartDesign component.

To run the simulation, ensure that the following files are present in the Libero SoC project:

- dram.v
- dram_parameters.vh
- AXI_testbench.v

The default location of the files is:

<Download folder>\IGLOO2_MDDR_Demo_DF\Libero_project\IGL2_MDDR_Demo\stimulus
2.4.1 Simulation

Simulation setup configuration can be set properly by using the following steps:

1. Launch the Libero SoC software.
2. Browse the IGL2 MDDR Demo project provided in the design file.
3. Go to Project > Project Settings > Simulation Options.
4. Ensure that the DO File tab has the configuration, as shown in Figure 7.

Figure 7 • DO File Settings

5. Ensure that the Waveforms tab has the configuration, as shown in Figure 8.

Figure 8 • Waveforms Settings

6. Go to Design Flow tab.
7. Right-click Simulate under Verify Pre-Synthesized Design and select Organize Input Files > Organize Stimulus Files..., as shown in Figure 9.
8. Ensure the **Organize Stimulus files** window has the configuration, as shown in Figure 10.

**Figure 10** • Organize Stimulus Files Window
2.4.2 Running the Simulation

The following steps describe how to run the simulation:

1. Right-click Simulate under Verify Pre-Synthesized Design.
2. Click Open Interactively.
3. Simulation run time is 900 µs, as shown in Figure 7 on page 14.

Figure 11 shows the transcript window of the simulation.

![Transcript Window](image)
Figure 12 shows the single AXI write and AXI read operation.

**Figure 12 • Single Write and Read Operation**

Figure 13 shows the 16-beat AXI burst write and read operation.

**Figure 13 • 16-Beat AXI Burst Write and Read**
2.5 Setting Up the Hardware Demo

The following steps describe how to setup the hardware demo:

1. Connect the jumpers on the IGLOO2 Evaluation Kit, as shown in Table 2.

Table 2 • IGLOO2 FPGA Evaluation Kit Jumper Settings

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Pin (From)</th>
<th>Pin (To)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>J22</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J23</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J24</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J8</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J3</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
</tbody>
</table>

**CAUTION:** Ensure that the power supply switch SW7 is switched OFF while connecting the jumpers.

2. Connect the Power supply to the J6 connector, switch ON the power supply switch, SW7.
3. Connect the FlashPro4 programmer to the J5 connector of the IGLOO2 Evaluation Kit board.
4. Connect the Host PC USB port to the IGLOO2 Evaluation Kit board J18 USB connector using the USB mini-B cable.

*Figure 14* shows the board setup for running the IGLOO2 MDDR demo on the IGLOO2 Evaluation Kit.

*Figure 14* • IGLOO2 Evaluation Kit
5. Ensure that the USB to UART bridge drivers are automatically detected. This can be verified in the Device Manager of the host PC. The FTDI USB to UART converter enumerates four COM ports. For USB 2.0, note down the USB Serial Converter D COM port number to use it in the GUI. Figure 15 shows the USB 2.0 Serial port properties. As shown in Figure 15, COM10 is connected to USB Serial Converter D. Refer to “Appendix: Finding Correct COM Port Number when Using USB 3.0” on page 32 for finding the correct COM port in USB 3.0.

Figure 15 • USB Serial 2.0 Port Properties

6. If the USB to UART bridge drivers are not installed, download and install the drivers from www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip.
2.6 Programming the Demo Design

The following steps describe how to program the demo design:

1. Download the demo design from the following link: [http://soc.microsemi.com/download/rsc/?f=m2gl_dg0534_liberov11p8sp2_df](http://soc.microsemi.com/download/rsc/?f=m2gl_dg0534_liberov11p8sp2_df)
2. Switch ON the power supply switch SW7.
3. Launch the FlashPro software.
4. Click New Project.
5. In the New Project window, type the project name as IGL2_MDDR_Demo.
6. Click Browse and navigate to the location where you want to save the project.
7. Select Single device as the Programming mode.
8. Click OK to save the project.

*Figure 16 • FlashPro New Project*
2.6.1 Setting Up the Device

The following steps describe how to configure the device:

1. Click **Configure Device** on the FlashPro GUI.
2. Click **Browse** and navigate to the location where *IGL2_MDDR_Demo.stp* file is located, and select the file. The default location is:
   
   `<download_folder>\IGLOO2_MDDR_Demo_DF\Programming_file`

3. Click **Open**. The required programming file is selected and is ready to be programmed in the device.

*Figure 17 • FlashPro Project Configuration*
2.6.2 Programming the Device

Click PROGRAM to start programming the device. Wait until the Programmer Status is changed to RUN PASSED, as shown in Figure 18.

*Figure 18 • FlashPro Program Passed*

2.6.3 Running the Hardware Demo

The IGLOO2 MDDR demo comes with a utility, IGL2_MDDR_Demo, that runs on the host PC to communicate with the IGLOO2 Evaluation Kit. The UART protocol is used as the underlying communication protocol between the host PC and IGLOO2 Evaluation Kit.
Figure 19 shows initial screen of the IGL2_MDDR_Demo utility.

**Figure 19 • IGL2_MDDR_Demo Utility**

The IGL2_MDDR_Demo utility consists the following sections:

- **Serial Port Configuration**: Displays the serial port. Baud rate is fixed at 115200
- **Data Transfer Type**: Single or Burst
- **LPDDR SDRAM**: Provides Address and Data
- **LPDDR Burst Read**: Displays the Burst Read Values for the corresponding address
- **C**: Clears the existing data

### 2.6.4 Steps to Run GUI

The following steps describe how to run the GUI:

1. Launch the utility. The default location is: 
   
   `<download_folder>\IGLOO2_MDDR_Demo_DF\Demo_Utility\IGL2_MDDR_Demo.exe`

2. Select the appropriate COM port from drop down menu. In this case, it is COM 10.
3. Click **Connect**. The connection status along with the COM Port and Baud rate is shown in the left bottom corner of the screen.
2.6.5 Performing Single Data Transfer

For a single write or read operation, the AXI master logic is configured to transfer a burst length of 1 (that is, 8 bytes). For a write operation, the utility sends a 32-bit address and 64-bit (8 bytes) data. The data is then written to the LPDDR SDRAM. For a read operation, the utility sends a 32-bit address and receives 64-bit data from LPDDR and is displayed in the utility.

The following steps describe how to perform a single data transfer:

1. Select **Single (8-bytes)** as **Data Transfer Type**.
2. A 64-bit aligned address is required in the address field. Enter a 32-bit HEX Address in the range 0x00000000 - 0x03FFFFF8. When a non 64-bit aligned address is provided, the GUI converts it to 64-bit aligned address and performs the write/read. Refer to "Appendix: Performing Write/Read Operation when Non 64-bit Aligned Address is Provided" on page 34 to perform write/read when non 64-bit aligned address is provided.
3. In the **Data** field, enter a 64-bit data in HEX format.
4. Click **Write**. The entered data is written to the LPDDR memory.

---

**Figure 20** shows the connection status of the utility.

**Figure 20** • IGL2_MDDR_Demo- Connection Status
Figure 21 shows the **Address** and **Data** values entered for a Single Write operation.

**Figure 21 • Single Write Operation**

5. To verify the write operation, perform a read operation to the same address where the data is written.

6. Press **C** to clear the data present in the **Data** field. **Figure 22** highlights the Clear button, C.

**Figure 22 • Clear Data Field**

7. Click **Read** to read the data from the LPDDR SDRAM.
Figure 23 shows the data read from the LPDDR SDRAM.

**Figure 23**  •  Single Read Operation

8. Compare the read and write data. The write and read data being same establishes that the write and read operations to the LPDDR SDRAM were successful.

### 2.6.6 Performing Burst Data Transfer

For a burst write or read operation, the AXI master logic is configured to transfer a burst length of 16 (that is, 128 bytes). In this demo, 16 transfers of 16-bit burst operations are implemented (16 transfers × 16-bit burst data = 2048 bytes data). For a write operation, the utility sends a 32-bit initial address and 64-bit (8 bytes) initial data. After the initial write operation, incremental data is written. For a read operation, the utility sends a 32-bit address and receives 2048 bytes of data from the LPDDR SDRAM and the data is displayed in the utility.

The following steps describe how to perform a burst data transfer:

1. Select **Burst (2048-bytes)** as **Data Transfer Type**.
2. A 64-bit aligned address is required in the address field. Enter a 32-bit HEX Address in the range 0x00000000 - 0x03FFFFF8. When a non 64-bit aligned address is provided, the GUI converts it into 64-bit aligned address and performs the write/read operation. Refer to "Appendix: Performing Write/Read Operation when Non 64-bit Aligned Address is Provided" on page 34 to perform write/read when non 64-bit aligned address is provided.
3. In the **Data** field, enter a 64-bit data in HEX format.
4. Click **Write**. The entered data is written to the Address location specified in the Address filed and then the data is incremented by 1 and written to the next address location. This is repeated 256 times to write all the 2048 bytes of data.
Figure 24 shows the **Address** and **Data** values entered for a Burst Write operation.

**Figure 24 • Burst Write Operation**

5. To verify the write operation, perform a read operation to the same address where the data is written.
6. Click **Read**. All the 2048 bytes of data written to the LPDDR is read, and the read data is displayed on the **LPDDR Burst Read** panel.

**Figure 25 shows the burst read data.**

**Figure 25 • Burst Read Operation**

7. Click **Exit** to exit the utility.

### 2.7 Conclusion

This demo shows how to perform read/write operations to LPDDR SDRAM using the IGLOO2 MDDR controller. Options are provided to simulate the design using a SmartDesign testbench and validate the design on the IGLOO2 Evaluation Kit using a GUI interface.
3 Appendix: Configuring MDDR Controller

This section describes how to configure the MDDR controller registers using Libero SoC. The configuration options for MDDR are available at the MDDR tab of the Memories tab in system builder. Figure 26 shows the MDDR tab.

The IGLOO2 Evaluation Kit has the LPDDR memory from Micron. All values provided here are from the Micron datasheet, part number, MT46H32M16LF.

Note: The Automotive Mobile Low-Power DDR SDRAM Datasheet is available to download it from Micron website.

Figure 26 • System Builder - Memories - MDDR Tab
3.1 MDDR Configuration Tab

When using an external memory, the memory controller must wait for the memory to initialize (settling time) before accessing it. The IGLOO2 Evaluation Kit uses the LPDDR memory. Therefore, the DDR controller has to wait at least 200 us. Provide 200 as the value for the field, DDR memory settling time (us).

Note: All the values provided here are from the Micron datasheet. The parameters can be configured according to the user’s requirements.

3.1.1 General

This section shows the configurations of the General tab:

- Memory Type: LPDDR
- Data Width: 16
- Address Width (bits):
  - Row: 16
  - Bank: 2
  - Column: 10

Figure 27 shows the General tab after configuration parameters are set.

Figure 27 • System Builder MDDR Configuration – General Tab
3.1.2 Memory Initialization

This section shows the configurations of the Memory Initialization tab:

- Burst length: 8
- Burst Order: Sequential
- Timing Mode: 1T
- CAS Latency: 3
- Self Refresh Enabled: NO
- Auto Refresh Burst Count: Single
- Powerdown Enabled: YES
- Stop the Clock: NO
- Deep Powerdown enabled: NO
- Powerdown Entry Time: 320

Figure 28 shows the Memory Initialization tab after configuration parameters are set.

Figure 28 • System Builder MDDR Configuration – Memory Initialization Tab
### 3.1.3 Memory Timing

This section shows the configurations of the Memory Timing tab:

- Time To Hold Reset before INIT: 0
- MRD: 4
- RAS (Min): 8
- RAS (Max): 8192
- RCD: 6
- RP: 7
- REFI: 3104
- RC: 12
- XP: 3
- CKE: 3
- RFC: 79
- FAW: 0

Figure 29 shows the Memory Timing tab after configuration parameters are set.

*Figure 29 • System Builder MDDR Configuration – Memory Timing Tab*
Appendix: Finding Correct COM Port Number when Using USB 3.0

FTDI USB to UART converter enumerates the four COM ports. In USB 3.0, the four available COM ports are in Location 0. Figure 30 shows the USB 3.0 Serial port properties.

Figure 30 • USB 3.0 Serial Port Properties

To find out the correct COM port, program the IGLOO2 Evaluation Kit board with the provided programming file. Connect each available COM port and click Write. If a wrong COM port is selected, the GUI displays the read error. Try with all four available COM ports until the read error message disappears.
Figure 31 shows the **Read Error** message.

**Figure 31 • Read Error**
Appendix: Performing Write/Read Operation when Non 64-bit Aligned Address is Provided

When a non 64-bit aligned address is provided in the GUI, the GUI converts it into the 64-bit aligned address (0x0, 0x8, 0x10, 0x18, 0x20, 0x28, 0x30, 0x38 ...) and performs the write/read operation.

1. Enter the non 64-bit aligned 32-bit address in HEX format.
2. Enter the 64-bit data in HEX format.
3. Click **Write** to perform the write operation. GUI converts the address into 64-bit aligned address and performs the write operation.
Figure 33 shows the GUI pop-up information message and converted 64-bit aligned address.

**Figure 33** Converted 64-bit Aligned Address
## Revision History

The following table shows important changes made in this document for each revision.

<table>
<thead>
<tr>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revision 7 (February 2018)</td>
<td>Updated the document for Libero v11.8 SP2 software release.</td>
</tr>
<tr>
<td>Revision 6 (March 2016)</td>
<td>Updated the document for Libero v11.7 software release changes (SAR 76992).</td>
</tr>
<tr>
<td>Revision 5 (November 2015)</td>
<td>Changed MDDR_CLK: DDR_FIC_CLK ratio to 1:1 and updated Figure 6 on page 13, Figure 12 on page 17, and Figure 13 on page 17 (SAR 73229).</td>
</tr>
<tr>
<td>Revision 4 (October 2015)</td>
<td>Updated the document for Libero v11.6 software release changes (SAR 72065).</td>
</tr>
<tr>
<td>Revision 3 (March 2015)</td>
<td>Updated the document for Libero SoC v11.5 (SAR 65209).</td>
</tr>
<tr>
<td>Revision 2 (August 2014)</td>
<td>Updated the document for Libero SoC v11.4</td>
</tr>
<tr>
<td>Revision 1 (March 2014)</td>
<td>Initial release</td>
</tr>
</tbody>
</table>
7  Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

7.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

7.2 Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

7.3 Technical Support


7.4 Website


7.5 Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

7.5.1 Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

7.5.2 My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.
7.5.3 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

7.6 ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech@microsemi.com. Alternatively, within My Cases, select Yes in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.