DG0538
Demo Guide
SmartFusion2 SerDes XAUI

Microsemi
Power Matters.™

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

50200538. 2.0 3/17

Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Updated the demo guide for Libero v11.8 software release changes.
- Removed running the design section as M2S050 device kit is discontinued.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document.

2 SmartFusion2 SerDes XAUI

SmartFusion®2 System-on-Chip (SoC) FPGAs have embedded high-speed SerDes blocks that can handle data rates from 1 Gbps to 5 Gbps. The SerDes module integrates several functional blocks to support multiple high-speed serial protocols within the FPGA. XAUI is a standard for extending the 10 Gb media independent interface (XGMII) between the media access control (MAC) and PHY layer of 10 Gb Ethernet (10 GbE). SmartFusion2 high-speed serial block implements hardened XAUI.

2.1 Design Requirements

The following table lists the hardware, software, and IP requirements for this demo design.

Table 1 • **Design Requirements**

Requirement	Version
Operating system	Windows 7/8 (64-bit)
Software	
Libero® System-on-Chip (SoC)	v11.8
FlashPro Programming	v11.8
IP	
SERDES_IF	1.2.210
OSC	2.0.101
FCCC	2.0.101
COREUART	5.6.102

2.2 Prerequisites

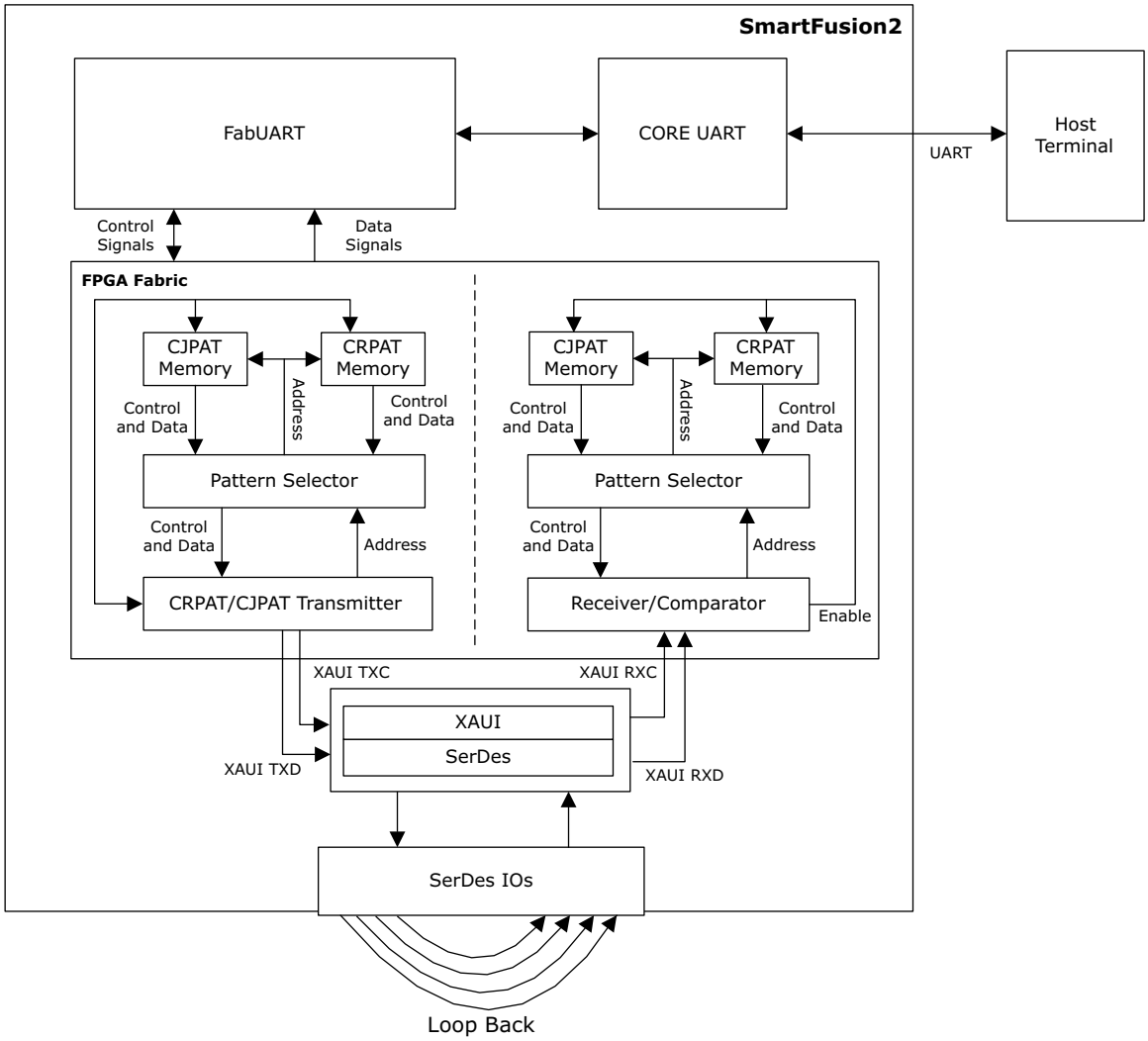
Before you start:

1. Download the design files from the following link:
   http://soc.microsemi.com/download/rsc/?f=m2s_dg0538_liberov11p8_df
2. Download and install Libero SoC software on the host PC.
3. Start Libero SoC software, and in the **Project** menu, click **Open Project**.
4. Browse the SF2_XAUI_Demo Libero project folder and open the `SF2_XAUI_Demo.prjx` file. The SmartFusion2 SerDes XAUI project opens.
5. Open the **Design Hierarchy** window and double-click the **SF2_XAUI_Demo** component.
   The SmartDesign page opens on the right pane and displays the high-level design. You can view the design blocks and IP cores instantiated for the SerDes XAUI design.

2.3 Demo Design

This demo design demonstrates transmitting continuous random test pattern (CRPAT) and continuous jitter test pattern (CJPAT) over the SmartFusion2 high-speed SerDes interface. SerDes is configured for 3.125 Gbps operational speed. The system block diagram for the design implemented in a SmartFusion2 device is as shown in the following figure.

Figure 1 • **SerDes XAUI Demo Design Top-Level Block Diagram**



CRPAT_MEM: this block implements the IEEE 802.3ae CRPAT and generates a continuous stream of identical patterns, separated by minimum inter-packet gap (IPG).The CRPAT is intended to provide broad spectral content and minimal peaking used for the measurement of jitter at either a component or system level.

Each packet in the CRPAT consists of eight octets of PREAMBLE/SFD, followed by 1488 data octets (124 repetitions of the 12-octet modified RPAT sequence), plus four CRC octets, followed by a minimum IPG of 12 octets of IDLE.

CJPAT_MEM: this block implements the IEEE 802.3ae CJPAT.The CJPAT is intended to expose a receiver CDR to large instantaneous phase jumps. The pattern alternates repeating low-transition density patterns with repeating high-transition density patterns. The repeating code-group durations should be longer than the time constants in the receiver clock recovery circuit. This assures that the clock phase has followed the systematic pattern jitter and the data sampling circuitry is exposed to large systematic phase jumps. This stresses the timing margins in the received eye.

Pattern selector: this module is used for selection of either CRPAT or CJPAT to be sent onto the transmitter of XAUI. This selection input is driven from the host terminal through the GUI.

Transmitter: sends the pattern along with control signals onto the SerDes interface. The data is fed onto the transmitter from the pattern selector block. The transmitter sends 64 bits of data signals onto the TXD interface and eight bits of control signals onto the TXC interface of the SerDes.

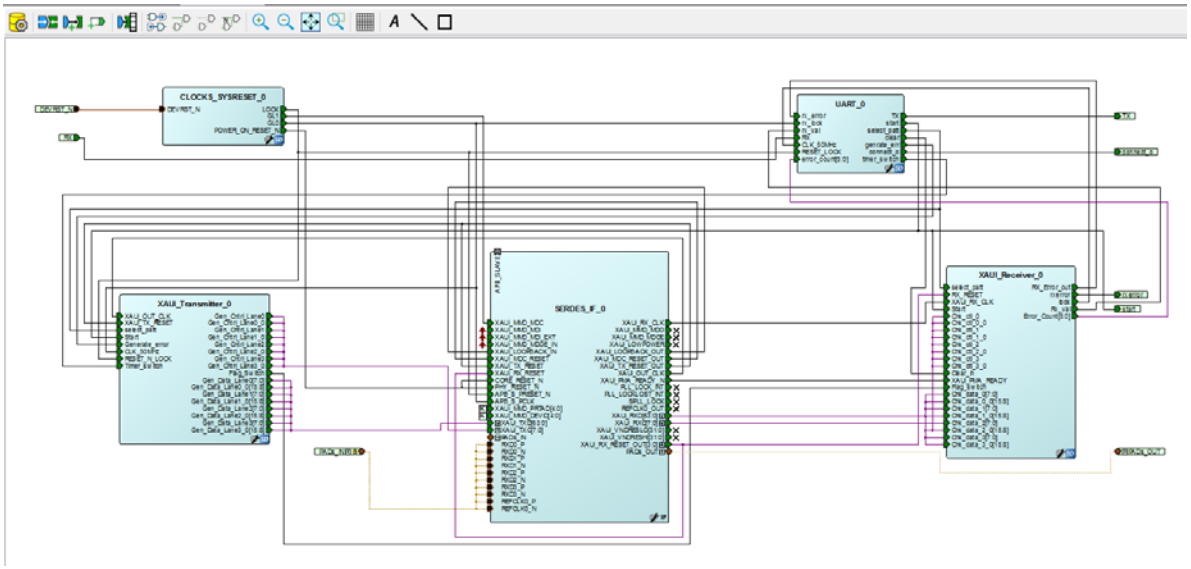
Receiver: this block checks for corresponding CRPAT or CJPAT sequences depending on the pattern selection done and sent over the SerDes interface. If the received sequence does not match with the one transmitted by the transmitter, the receiver indicates an error. The receiver also implements an error counter which is incremented for each error in the received pattern.

Debounce: this logic is written for detecting the stable pulse from GUI. On detecting a stable pulse, the logic raises a flag which is used to initiate the XAUI demo.

2.3.1 Design Implementation

The following figure shows the Libero SoC software design implementation of the SerDes XAUI.

Figure 2 • **SerDes XAUI Design**



2.3.2 IP Configuration

The following IPs and macros need to be configured before simulating the demo design:

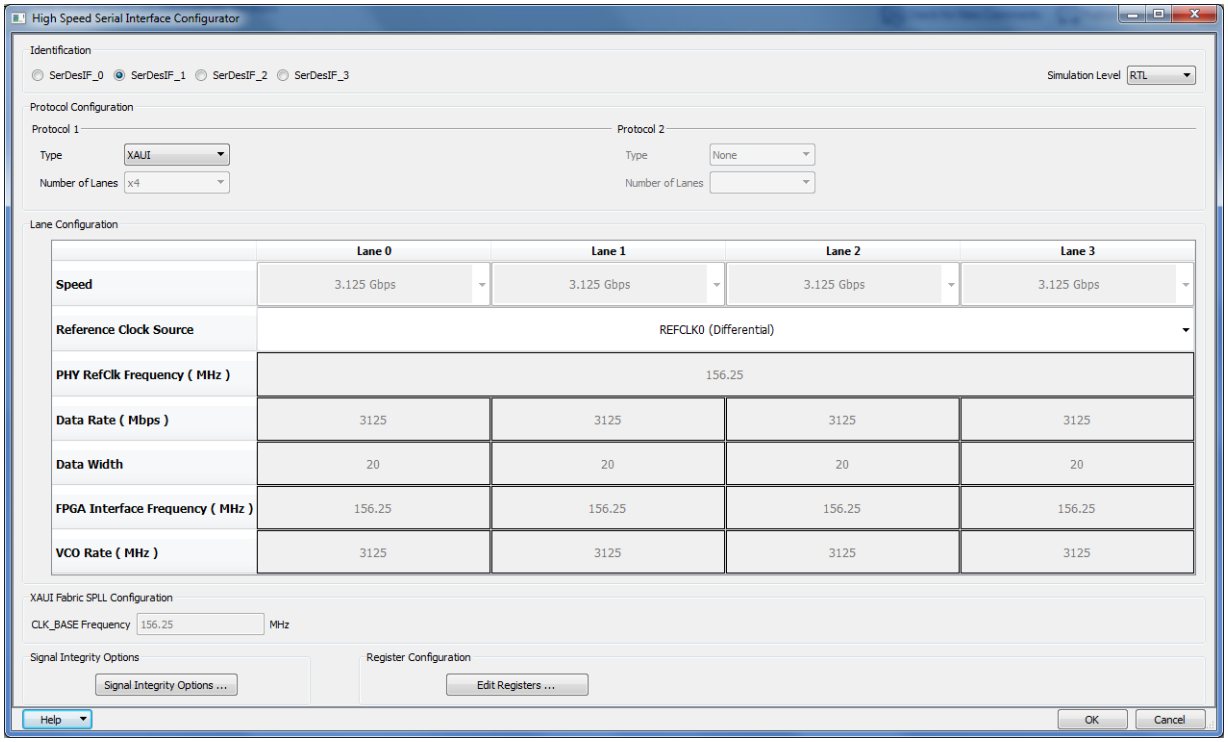
- High-speed serial interface
- Clock conditioning circuitry (CCC)

2.3.2.1 High-Speed Serial Interface

The SmartFusion2 SoC FPGA high-speed SerDes is a hard IP block on chip that supports rates up to 5 Gbps. The SerDes block offers embedded protocol support for PCIe, SRIO, XAUI, SGMII, EPCS, and so on. See the *UG0447: SmartFusion2 and IGLOO2 FPGA High Speed Serial Interfaces User Guide* for more information on the SerDes block.

In this demo, the SERDESIF_1 block is configured for the XAUI mode, with reference clock from REFCLK0 coming from external source.

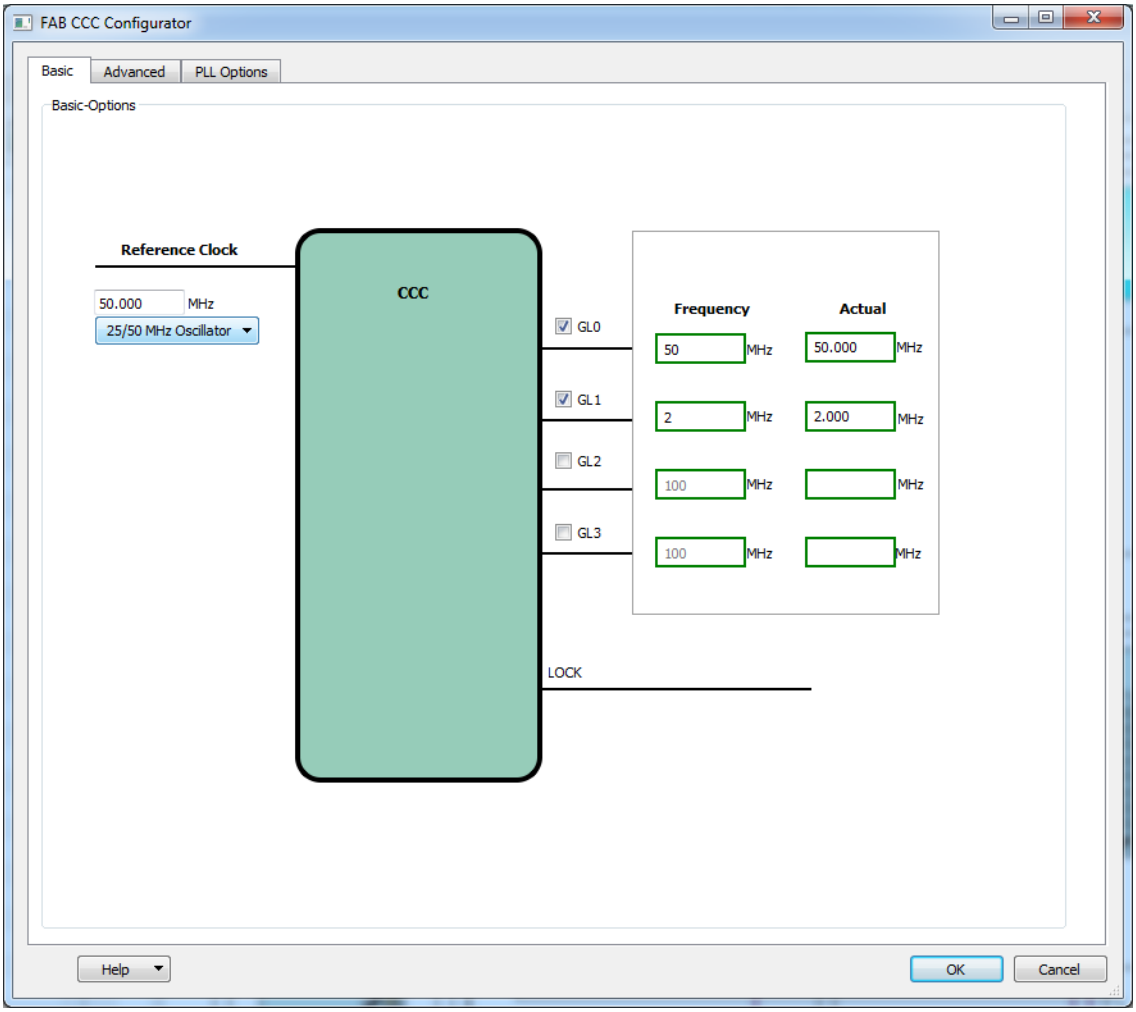
Figure 3 • **High-Speed Serial Interface Configurator**



2.3.2.2 Clock Conditioning Circuitry

CCC provides reference clock needed for clock for the CoreUART, FabUART, and clock for management block in the SerDes XAUI mode. See the *UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide* for more information on CCC blocks.

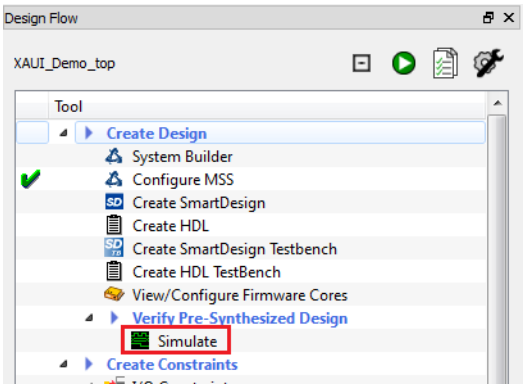
Figure 4 • **CCC Configurator**



2.4 Simulating the Design

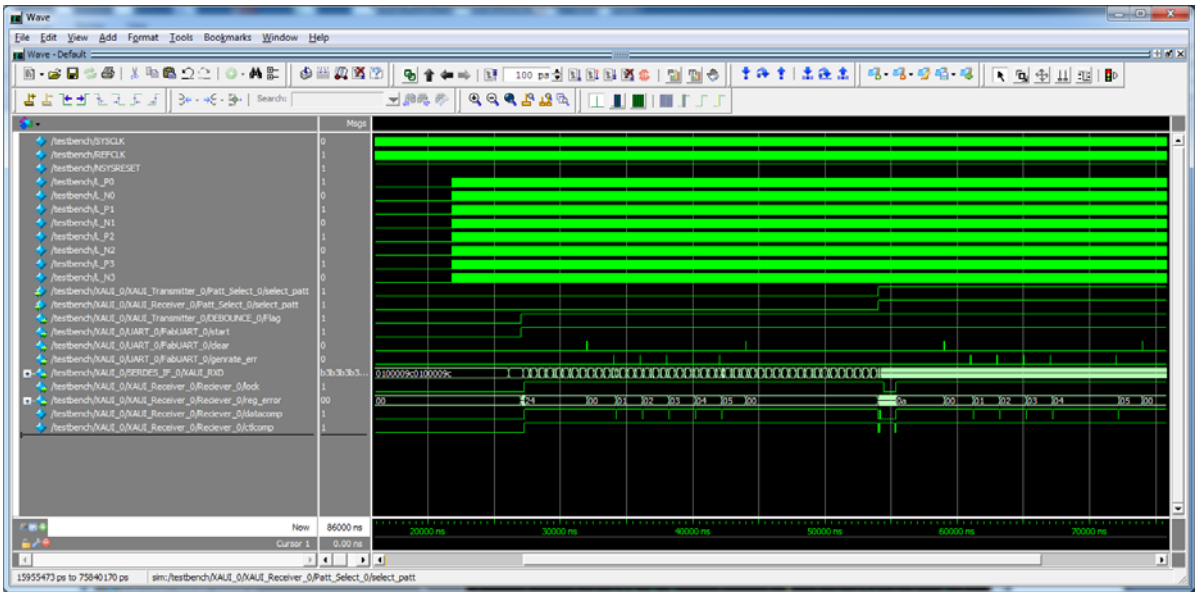
In the **Design Flow** tab, double-click **Simulate** under **Verify Pre-Synthesized Design** to simulate the design, as shown in the following figure. The ModelSim tool takes about 3 to 5 minutes to complete the simulation.

Figure 5 • **Simulating the Design**



When the simulation is successful, the waveform window appears as shown in the following figure.

Figure 6 • **Simulation Waveform Window**



2.5 Conclusion

This demo described how to simulate the SerDes XAUI IP cores and how to implement the Libero design flow using Libero SoC software.