DG0760
Demo Guide
RTG4 SerDes XAUI

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Updated the document for Libero v11.9 SP1 software release.

1.2 Revision 2.0

Updated the document for Libero v11.8 SP2 software release.

1.3 Revision 1.0

Revision 1.0 is the first publication of this document.

2 RTG4 SerDes XAUI

RTG4™ FPGAs have embedded high-speed SerDes blocks that can handle data rates from 1 Gbps to 5 Gbps. The SerDes module integrates several functional blocks to support multiple high-speed serial protocols within the FPGA. XAUI is a standard for extending the 10 Gb media independent interface (XGMII) between the media access control (MAC) and PHY layer of 10 Gb Ethernet (10 GbE). RTG4 high-speed serial block implements hardened XAUI.

This document contains information with respect to the software simulations of XAUI protocol.

2.1 Design Requirements

The following table lists the hardware, software, and IP requirements for this demo design.

Table 1 • **Design Requirements**

Requirement	Version
Operating system	Windows 7/8 (64-bit)
Software	
Libero® System-on-Chip (SoC)	v11.9 SP1
FlashPro Programming	v11.9 SP1
IP	
SerDes Block	1.1.220
RTG4FCCC	1.1.226
COREUART	5.6.102

2.2 Prerequisites

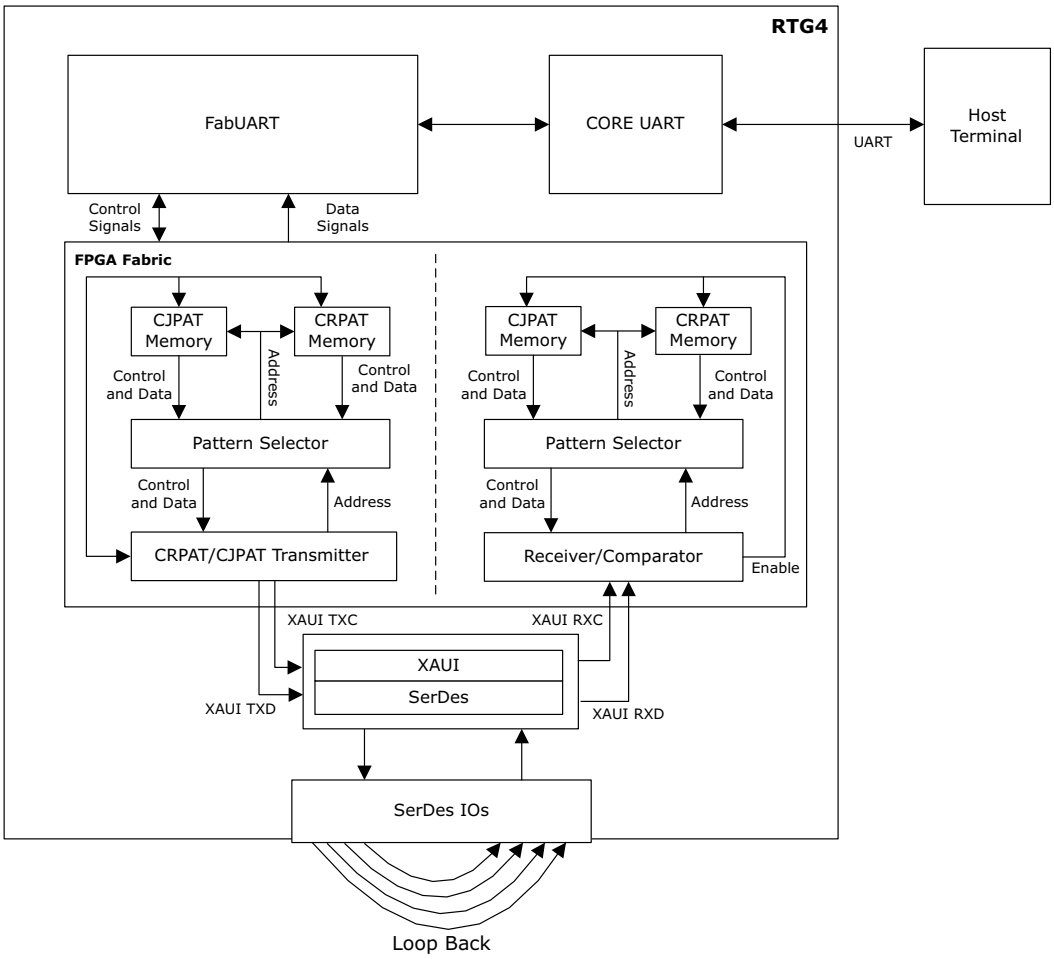
Before you start:

1. Download the design files from the following link:
   http://soc.microsemi.com/portal/default.aspx?r=17&p=f=rtg4_dg0760_liberov11p9sp1_df
2. Download and install Libero SoC software on the host PC.
3. Start Libero SoC software, and in the **Project** menu, click **Open Project**.
4. Browse the RTG4_XAUI Libero project folder and open the `RTG4_XAUI.prjx` file.
   The RTG4 SerDes XAUI project opens.
5. Open the **Design Hierarchy** window and double-click the **RTG4_XAUI** component.
   The SmartDesign page opens on the right pane and displays the high-level design. You can view the design blocks and IP cores instantiated for the SerDes XAUI design.

2.3 Demo Design

This demo design demonstrates transmitting continuous random test pattern (CRPAT) and continuous jitter test pattern (CJPAT) over the RTG4 high-speed SerDes interface. SerDes is configured for 3.125 Gbps operational speed. The system block diagram for the design implemented in a RTG4 device is as shown in the following figure.

Figure 1 • **SerDes XAUI Demo Design Top-Level Block Diagram**



CRPAT_MEM: this block implements the IEEE 802.3ae CRPAT and generates a continuous stream of identical patterns, separated by minimum inter-packet gap (IPG).The CRPAT is intended to provide broad spectral content and minimal peaking used for the measurement of jitter at either a component or system level.

Each packet in the CRPAT consists of eight octets of PREAMBLE/SFD, followed by 1488 data octets (124 repetitions of the 12-octet modified RPAT sequence), plus four CRC octets, followed by a minimum IPG of 12 octets of IDLE.

CJPAT_MEM: this block implements the IEEE 802.3ae CJPAT.The CJPAT is intended to expose a receiver CDR to large instantaneous phase jumps. The pattern alternates repeating low-transition density patterns with repeating high-transition density patterns. The repeating code-group durations should be longer than the time constants in the receiver clock recovery circuit. This assures that the clock phase has followed the systematic pattern jitter and the data sampling circuitry is exposed to large systematic phase jumps. This stresses the timing margins in the received eye.

Pattern selector: this module is used for selection of either CRPAT or CJPAT to be sent onto the transmitter of XAUI. This selection input is driven from the host terminal through the GUI.

Transmitter: sends the pattern along with control signals onto the SerDes interface. The data is fed onto the transmitter from the pattern selector block. The transmitter sends 64 bits of data signals onto the TXD interface and eight bits of control signals onto the TXC interface of the SerDes.

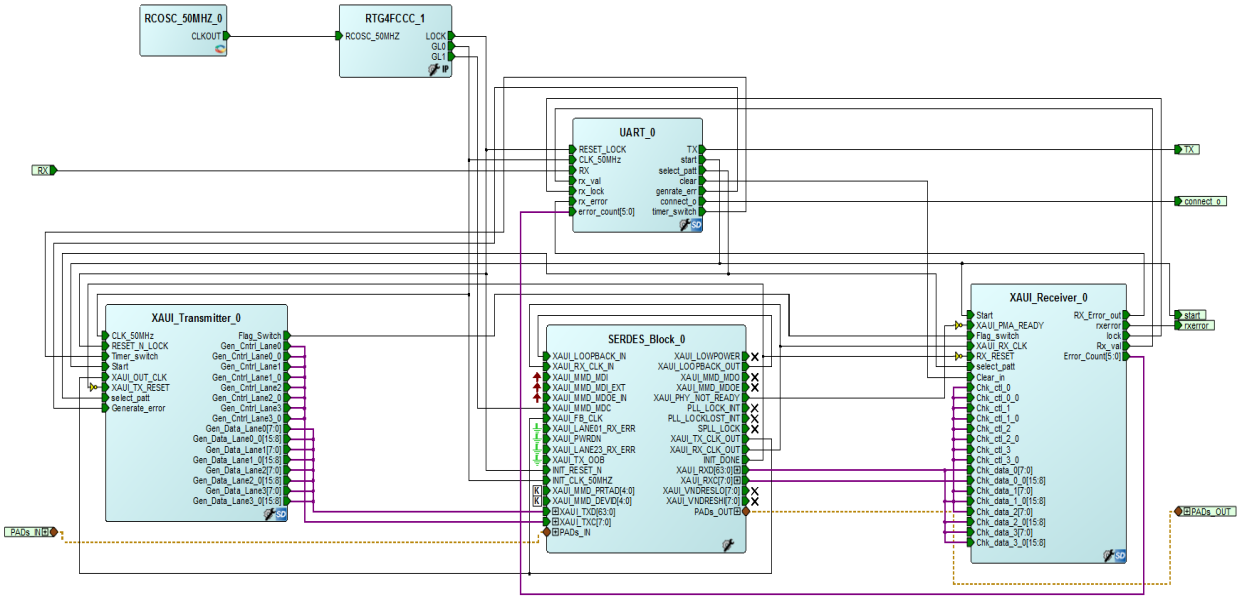
Receiver: this block checks for corresponding CRPAT or CJPAT sequences depending on the pattern selection done and sent over the SerDes interface. If the received sequence does not match with the one transmitted by the transmitter, the receiver indicates an error. The receiver also implements an error counter which is incremented for each error in the received pattern.

Debounce: this logic is written for detecting the stable pulse from GUI. On detecting a stable pulse, the logic raises a flag which is used to initiate the XAUI demo.

2.3.1 Design Implementation

The following figure shows the Libero SoC software design implementation of the SerDes XAUI.

Figure 2 • **SerDes XAUI Design**



2.3.2 IP Configuration

The following IPs and macros need to be configured before simulating the demo design:

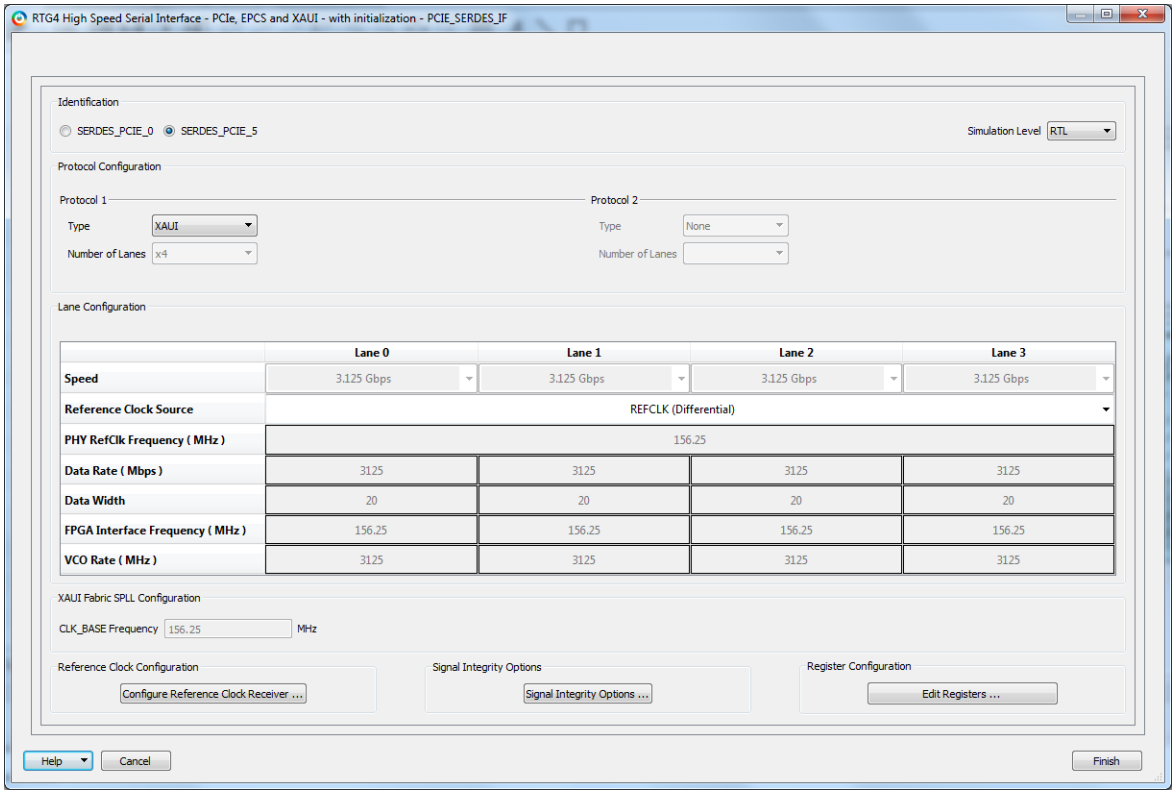
- High-speed serial interface
- Clock conditioning circuitry (CCC)

2.3.2.1 High-Speed Serial Interface

The RTG4 FPGA high-speed SerDes is a hard IP block on chip that supports rates up to 5 Gbps. The SerDes block offers embedded protocol support for PCIe, SRIO, XAUI, SGMII, EPCS, and so on. See the *UG0567: RTG4 FPGA High Speed Serial Interfaces User Guide* for more information on the SerDes block.

In this demo, the SERDESIF_Block block is configured for the XAUI mode, with reference clock from REFCLK0 coming from external source.

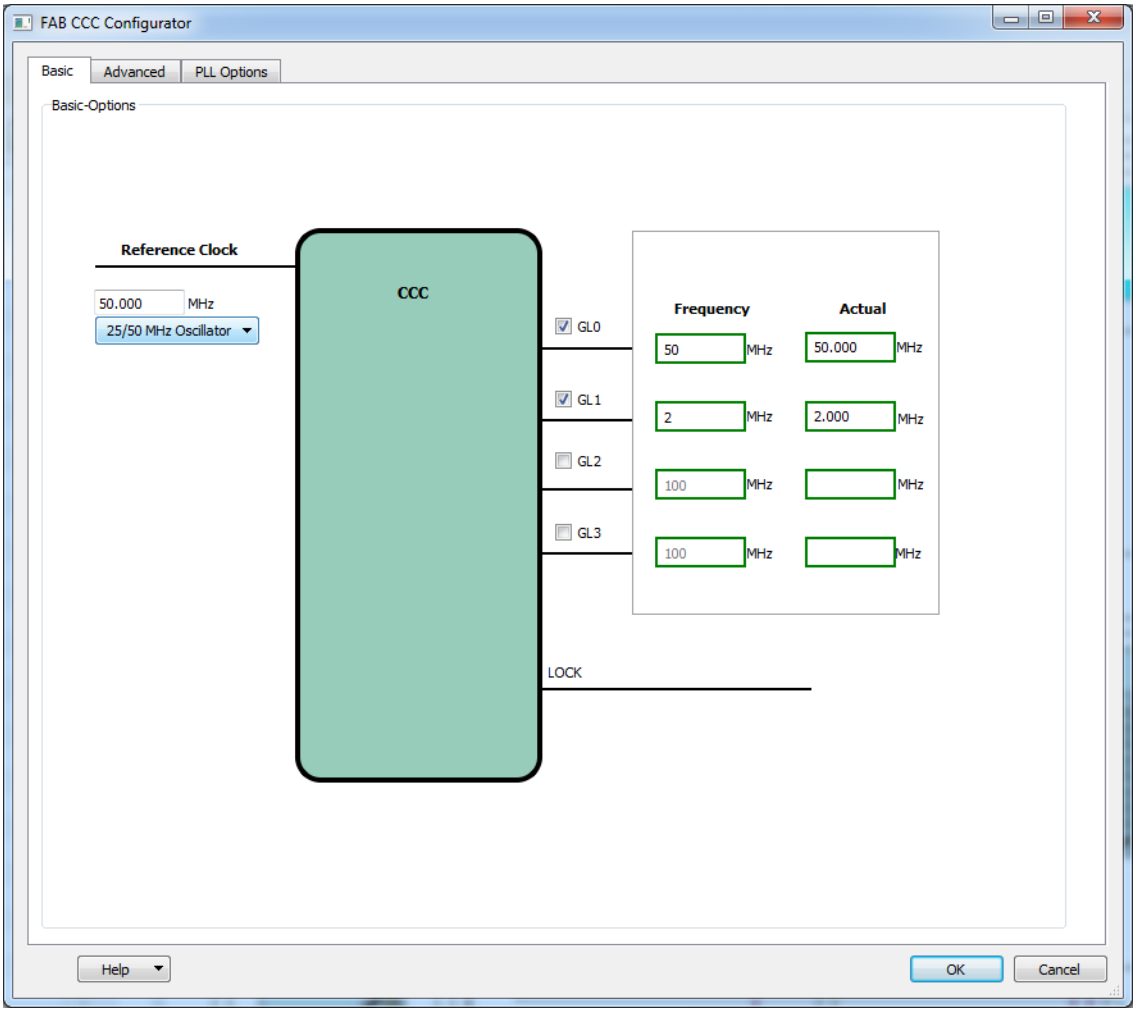
Figure 3 • **High-Speed Serial Interface Configurator**



2.3.2.2 Clock Conditioning Circuitry

CCC provides reference clock needed for clock for the CoreUART, FabUART, and clock for management block in the SerDes XAUI mode. See the *UG0586: RTG4 FPGA Clocking Resources User Guide* for more information on CCC blocks.

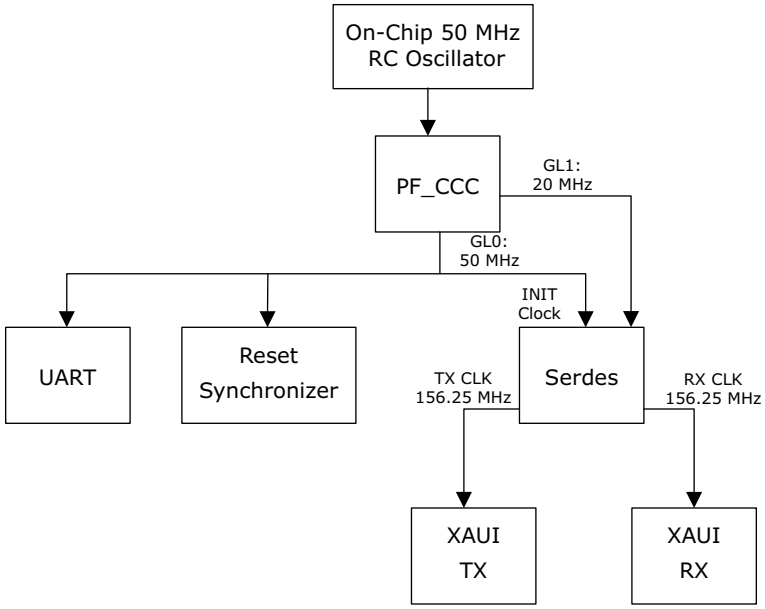
Figure 4 • **CCC Configurator**



2.4 Clocking Structure

The on-chip 50 MHz oscillator provides the reference clock to the FCCC block. The FCCC block provides two clocks, GL0 (50 MHz) and GL1 (20 MHz). The GL0 clock drives the SerDes block, UART, and Reset Synchronizer blocks. The GL1 clock drives the SerDes block. The following figure shows the clocking structure of the design.For more information about FCCC, see *UG0590: RTG4 FPGA Clock Conditioning Circuit with PLL Configuration User Guide from Libero*.

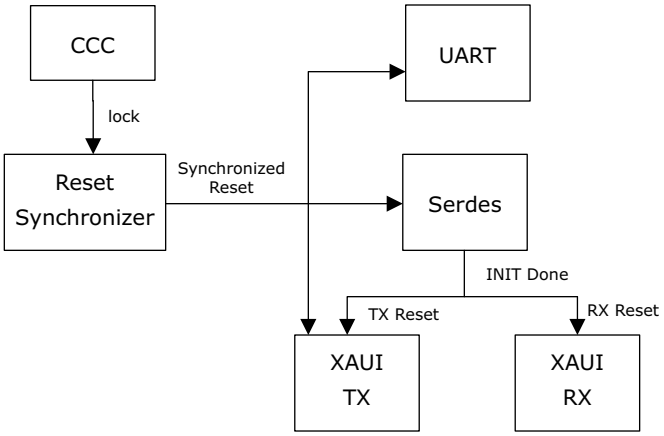
Figure 5 • **Clocking Structure**



2.5 Reset Structure

The LOCK signal from CCC is synchronized by using Reset Synchronizer block. The synchronized LOCK signal is then provided to UART, SerDes and XAUI transmitter. The INIT Done signal from SerDes block is the fed to XAUI TX and XAUI RX.

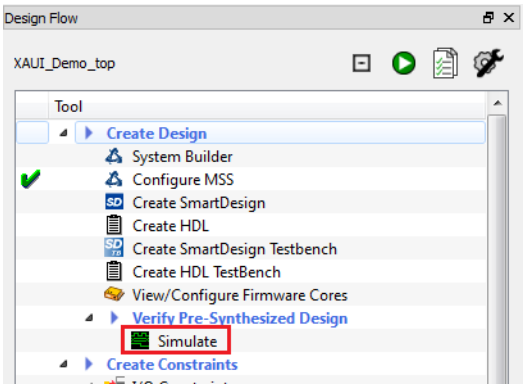
Figure 6 • **Reset Structure**



2.6 Simulating the Design

In the **Design Flow** tab, double-click **Simulate** under **Verify Pre-Synthesized Design** to simulate the design, as shown in the following figure. The ModelSim tool takes about 3 to 5 minutes to complete the simulation.

Figure 7 • **Simulating the Design**

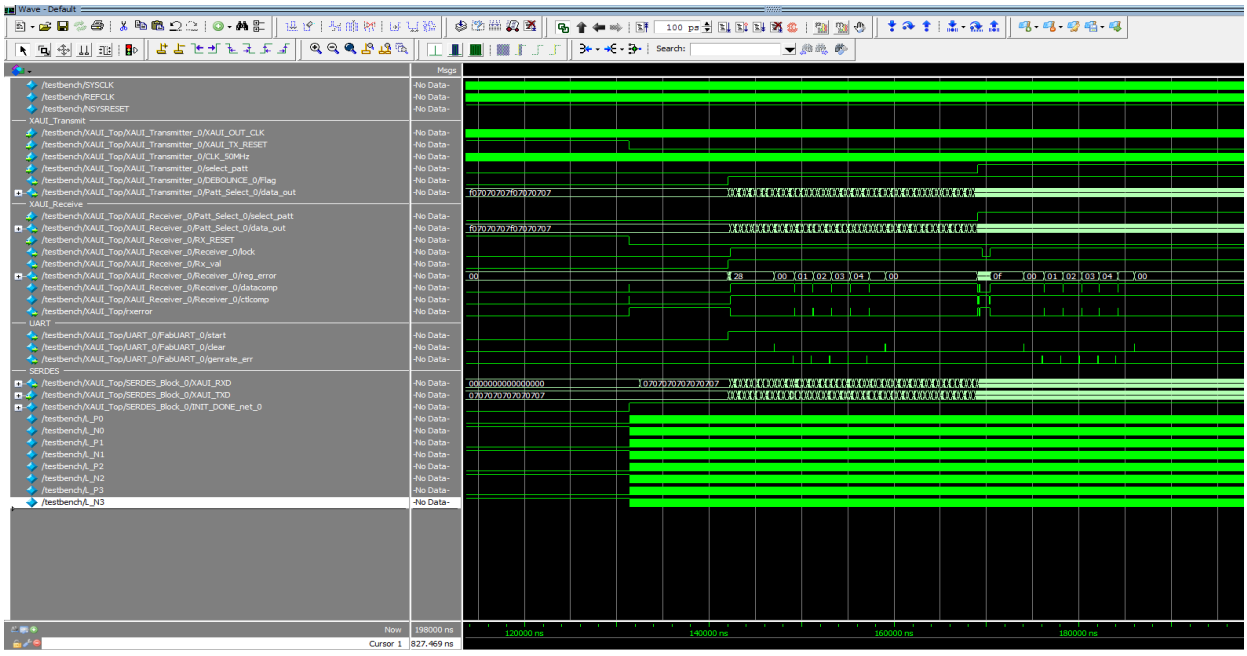


The demo design consists of following signals:

- 50 MHZ and 156.5Mhz clock
- Reset
- XAUI transmitter signal
- XAUI receiver signal
- UART signal
- SerDes signal

When the simulation is successful, the waveform window appears as shown in the following figure.

Figure 8 • **Simulation Waveform Window**



2.7 Conclusion

This demo described how to simulate the SerDes XAUI IP cores and how to implement the Libero design flow using Libero SoC software.